

## 54ACT/74ACT823 9-Bit D Flip-Flop

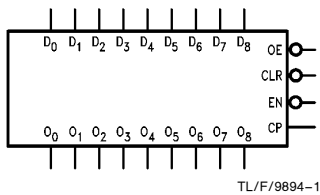
### General Description

The 'ACT823 is a 9-bit buffered register. It features Clock Enable and Clear which are ideal for parity bus interfacing in high performance microprogramming systems. The 'ACT823 offers noninverting outputs and is fully compatible with AMD's Am29823.

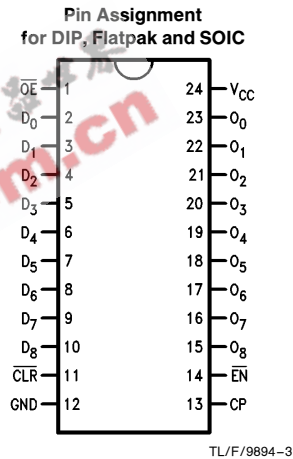
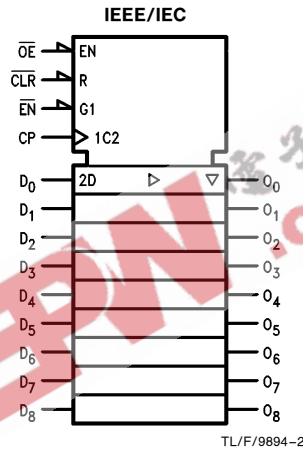
### Features

- Outputs source/sink 24 mA
- TRI-STATE® outputs for bus interfacing
- Inputs and outputs are on opposite sides
- 'ACT823 has TTL-compatible inputs

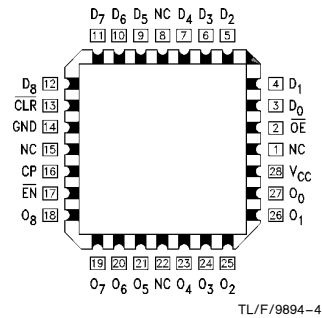
### Logic Symbols



### Connection Diagrams



### Pin Assignment for LCC



Pin Names	Description
D <sub>0</sub> -D <sub>8</sub>	Data Inputs
O <sub>0</sub> -O <sub>8</sub>	Data Outputs
OE	Output Enable
CLR	Clear
CP	Clock Input
EN	Clock Enable

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## Functional Description

The 'ACT823 consists of nine D-type edge-triggered flip-flops. These have TRI-STATE outputs for bus systems organized with inputs and outputs on opposite sides. The buffered clock (CP) and buffered Output Enable ( $\overline{OE}$ ) are common to all flip-flops. The flip-flops will store the state of their individual D inputs that meet the setup and hold time requirements on the LOW-to-HIGH CP transition. With  $\overline{OE}$  LOW, the contents of the flip-flops are available at the outputs. When  $\overline{OE}$  is HIGH, the outputs go to the high impedance state. Operation of the  $\overline{OE}$  input does not affect

the state of the flip-flops. In addition to the Clock and Output Enable pins, there are Clear ( $\overline{CLR}$ ) and Clock Enable ( $\overline{EN}$ ) pins. These devices are ideal for parity bus interfacing in high performance systems.

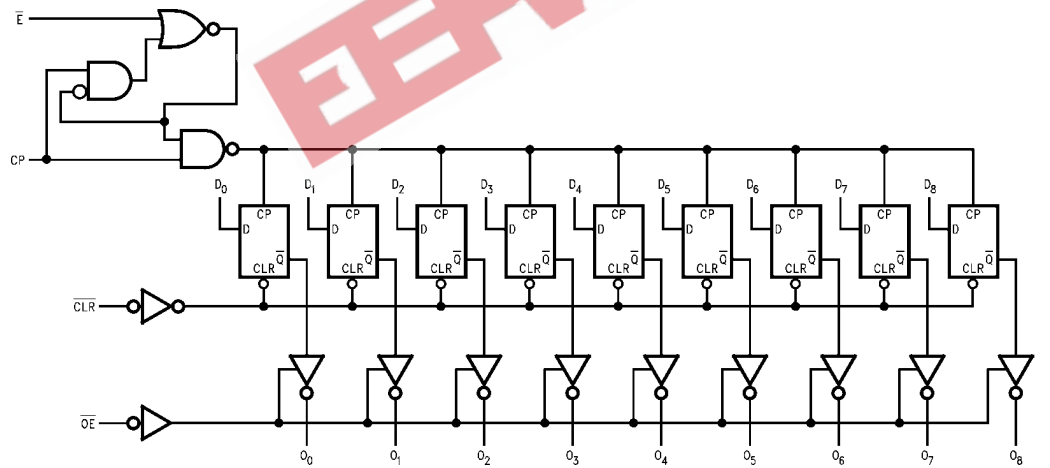
When  $\overline{CLR}$  is LOW and  $\overline{OE}$  is LOW, the outputs are LOW. When  $\overline{CLR}$  is HIGH, data can be entered into the flip-flops. When  $\overline{EN}$  is LOW, data on the inputs is transferred to the outputs on the LOW-to-HIGH clock transition. When the  $\overline{EN}$  is HIGH, the outputs do not change state, regardless of the data or clock input transitions.

Function Table

Inputs					Internal	Output	Function
$\overline{OE}$	$\overline{CLR}$	$\overline{EN}$	CP	D	Q	O	
H	X	L	↗	L	L	Z	High Z
H	X	L	↗	H	H	Z	High Z
H	L	X	X	X	L	Z	Clear
L	L	X	X	X	L	L	Clear
H	H	H	X	X	NC	Z	Hold
L	H	H	X	X	NC	NC	Hold
H	H	L	↗	L	L	Z	Load
H	H	L	↗	H	H	Z	Load
L	H	L	↗	L	L	L	Load
L	H	L	↗	H	H	H	Load

H = HIGH Voltage Level  
 L = LOW Voltage Level  
 X = Immaterial  
 Z = High Impedance  
 ↗ = LOW-to-HIGH Transition  
 NC = No Change

## Logic Diagram



TL/F/9894-5

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

## Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage ( $V_{CC}$ )	-0.5V to 7.0V
DC Input Diode Current ( $I_{IK}$ )	
$V_I = -0.5V$	-20 mA
$V_I = V_{CC} + 0.5V$	+20 mA
DC Input Voltage ( $V_I$ )	-0.5V to $V_{CC} + 0.5V$
DC Output Diode Current ( $I_{OK}$ )	
$V_O = -0.5V$	-20 mA
$V_O = V_{CC} + 0.5V$	+20 mA
DC Output Voltage ( $V_O$ )	-0.5V to $V_{CC} + 0.5V$
DC Output Source or Sink Current ( $I_O$ )	$\pm 50$ mA
DC $V_{CC}$ or Ground Current per Output Pin ( $I_{CC}$ or $I_{GND}$ )	$\pm 50$ mA
Storage Temperature ( $T_{STG}$ )	-65°C to +150°C
Junction Temperature ( $T_J$ )	
CDIP	175°C
PDIP	140°C

**Note 1:** Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT™ circuits outside databook specifications.

## Recommended Operating Conditions

Supply Voltage ( $V_{CC}$ )	4.5V to 5.5V
*ACT	
Input Voltage ( $V_I$ )	0V to $V_{CC}$
Output Voltage ( $V_O$ )	0V to $V_{CC}$
Operating Temperature ( $T_A$ )	
74ACT	-40°C to +85°C
54ACT	-55°C to +125°C
Minimum Input Edge Rate ( $\Delta V/\Delta t$ )	
*ACT Devices	
$V_{IN}$ from 0.8V to 2.0V	
$V_{CC}$ @ 4.5V, 5.5V	125 mV/ns

## DC Electrical Characteristics

Symbol	Parameter	$V_{CC}$ (V)	74ACT		54ACT	74ACT	Units	Conditions
			$T_A = 25^\circ\text{C}$		$T_A = -55^\circ\text{C to } +125^\circ\text{C}$	$T_A = -40^\circ\text{C to } +85^\circ\text{C}$		
			Typ	Guaranteed Limits				
$V_{IH}$	Minimum High Level Input Voltage	4.5	1.5	2.0	2.0	2.0	V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$
		5.5	1.5	2.0	2.0	2.0		
$V_{IL}$	Maximum Low Level Input Voltage	4.5	1.5	0.8	0.8	0.8	V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$
		4.5	1.5	0.8	0.8	0.8		
$V_{OH}$	Minimum High Level	4.5	4.49	4.4	4.4	4.4	V	$I_{OUT} = -50 \mu\text{A}$
			5.49	5.4	5.4	5.4		
		4.5		3.86	3.70	3.76	V	* $V_{IN} = V_{IL}$ or $V_{IH}$ $I_{OH} = -24 \text{ mA}$ $-24 \text{ mA}$
$V_{OL}$	Maximum Low Level Output Voltage	4.5	0.001	0.1	0.1	0.1	V	$I_{OUT} = 50 \mu\text{A}$
		5.5	0.001	0.1	0.1	0.1		
		4.5		0.36	0.50	0.44	V	* $V_{IN} = V_{IL}$ or $V_{IH}$ $I_{OL} = 24 \text{ mA}$ $24 \text{ mA}$
$I_{IN}$	Maximum Input Leakage Current	5.5		$\pm 0.1$	$\pm 1.0$	$\pm 1.0$	$\mu\text{A}$	$V_I = V_{CC}, \text{GND}$
$I_{OZ}$	Maximum TRI-STATE Current	5.5		$\pm 0.5$	$\pm 10.0$	$\pm 5.0$	$\mu\text{A}$	$V_I = V_{IL}, V_{IH}$ $V_O = V_{CC}, \text{GND}$
$I_{CCT}$	Maximum $I_{CC}/\text{Input}$	5.5	0.6		1.6	1.5	mA	$V_I = V_{CC} - 2.1V$
$I_{OLD}$	†Minimum Dynamic Output Current	5.5			50	75	mA	$V_{OLD} = 1.65V \text{ Max}$
$I_{OHD}$		5.5			-50	-75	mA	$V_{OHD} = 3.85V \text{ Min}$
$I_{CC}$	Maximum Quiescent Supply Current	5.5		8.0	160	80	$\mu\text{A}$	$V_{IN} = V_{CC}$ or GND

\*All outputs loaded; thresholds on input associated with output under test.

†Maximum test duration 2.0 ms, one output loaded at a time.

**Note:**  $I_{CC}$  limit for 54ACT @ 25°C is identical to 74ACT @ 25°C.

## AC Electrical Characteristics

Symbol	Parameter	V <sub>CC</sub> * (V)	74ACT			54ACT		74ACT		Units
			T <sub>A</sub> = +25°C C <sub>L</sub> = 50pF			T <sub>A</sub> = -55°C to +125°C C <sub>L</sub> = 50 pF		T <sub>A</sub> = -40°C to +85°C C <sub>L</sub> = 50 pF		
			Min	Typ	Max	Min	Max	Min	Max	
f <sub>max</sub>	Maximum Clock Frequency	5.0	120	158		95		109	MHz	
t <sub>PLH</sub>	Propagation Delay CP to O <sub>n</sub>	5.0	1.5	5.5	9.5	1.5	12.0	1.5	10.5	ns
t <sub>PHL</sub>	Propagation Delay CP to O <sub>n</sub>	5.0	2.0	5.5	9.5	1.5	12.0	1.5	10.5	ns
t <sub>PHL</sub>	Propagation Delay CLR to O <sub>n</sub>	5.0	2.5	8.0	13.5	1.5	18.0	2.0	15.5	ns
t <sub>pZH</sub>	Output Enable Time OE to O <sub>n</sub>	5.0	1.5	6.0	10.5	1.5	11.5	1.5	11.5	ns
t <sub>pZL</sub>	Output Enable Time OE to O <sub>n</sub>	5.0	2.0	6.5	11.0	1.5	12.0	1.5	12.0	ns
t <sub>PHZ</sub>	Output Disable Time OE to O <sub>n</sub>	5.0	1.5	6.5	11.0	1.5	13.5	1.5	12.0	ns
t <sub>PLZ</sub>	Output Disable Time OE to O <sub>n</sub>	5.0	1.5	6.0	10.5	1.5	12.0	1.5	11.5	ns

\*Voltage Range 5.0 is 5.0V ±0.5V

## AC Operating Requirements

Symbol	Parameter	V <sub>CC</sub> * (V)	74ACT		54ACT	74ACT	Units
			T <sub>A</sub> = +25°C C <sub>L</sub> = 50 pF		T <sub>A</sub> = -55°C to +125°C C <sub>L</sub> = 50 pF	T <sub>A</sub> = -40°C to +85°C C <sub>L</sub> = 50 pF	
			Typ	Guaranteed Minimum			
t <sub>s</sub>	Setup Time, HIGH or LOW D to CP	5.0	0.5	2.5	4.0	2.5	ns
t <sub>h</sub>	Hold Time, HIGH or LOW D <sub>n</sub> to CP	5.0	0	2.5	3.0	2.5	ns
t <sub>s</sub>	Setup Time, HIGH or LOW EN to CP	5.0	0	2.0	4.0	2.5	ns
t <sub>h</sub>	Hold Time, HIGH or LOW EN to CP	5.0	0	1.0	3.0	1.0	ns
t <sub>w</sub>	CP Pulse Width HIGH or LOW	5.0	2.5	4.5	6.0	5.5	ns
t <sub>w</sub>	CLR Pulse Width, LOW	5.0	3.0	5.5	7.0	5.5	ns
t <sub>rec</sub>	CLR to CP Recovery Time	5.0	1.5	3.5	4.5	4.0	ns

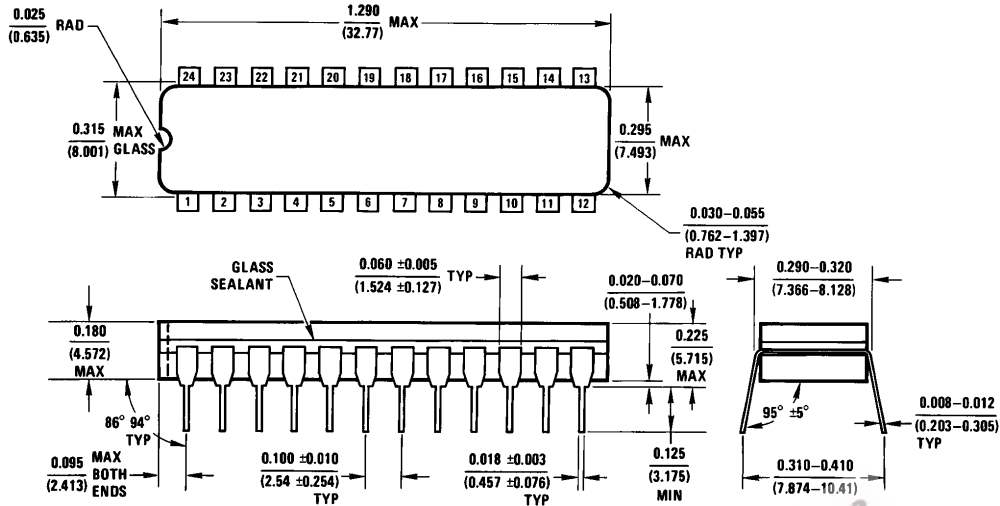
\*Voltage Range 5.0 is 5.0V ±0.5V

## Capacitance

Symbol	Parameter	Typ	Units	Conditions
C <sub>IN</sub>	Input Capacitance	4.5	pF	V <sub>CC</sub> = OPEN
C <sub>PD</sub>	Power Dissipation Capacitance	44	pF	V <sub>CC</sub> = 5.0V

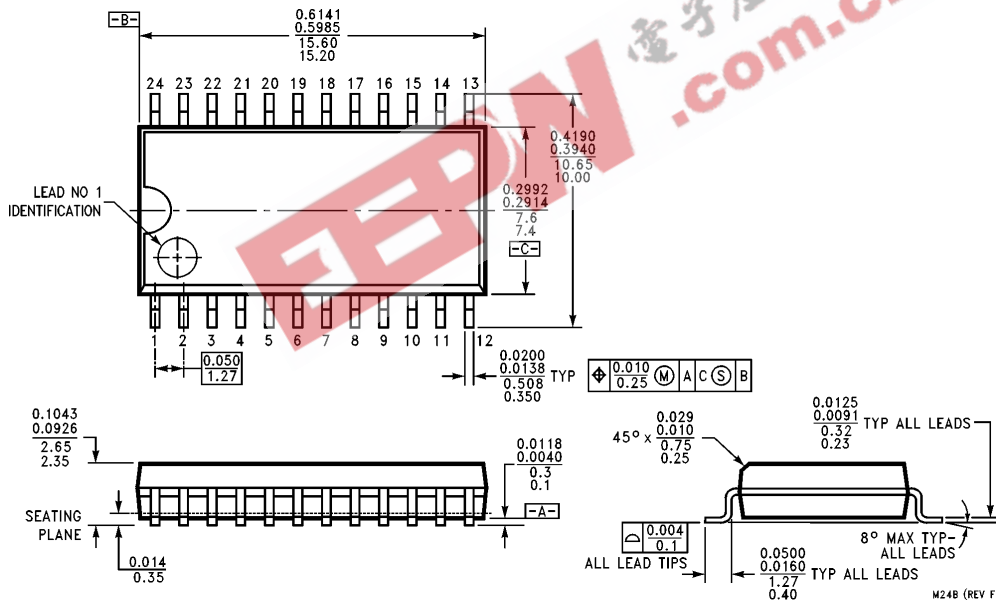


**Physical Dimensions** inches (millimeters) (Continued)



24 Lead Slim (0.300" Wide) Ceramic Dual-In-Line (SD)  
 NS Package Number J24F

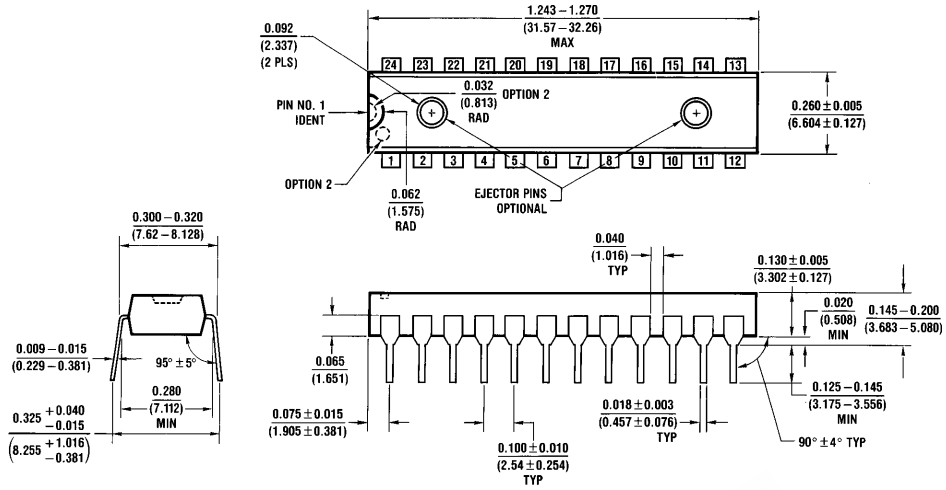
J24F (REV G)



24 Lead Small Outline Integrated Circuit (S)  
 NS Package Number M24B

M24B (REV F)

**Physical Dimensions** inches (millimeters) (Continued)



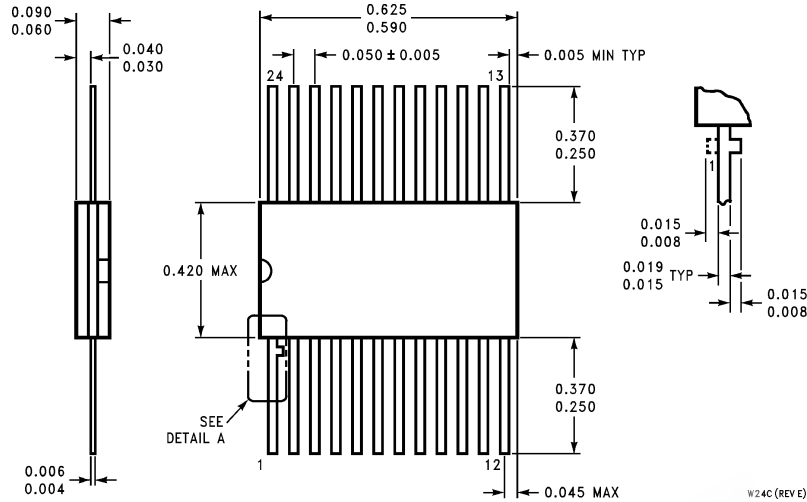
24 Lead Slim (0.300" Wide) Plastic Dual-In-Line (SP)  
NS Package Number N24C

N24C (REV F)

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**Physical Dimensions** inches (millimeters) (Continued)

Lit. # 114635



**24 Lead Ceramic Flatpak (F)  
NS Package Number W24C**



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**National Semiconductor Corporation**  
2900 Semiconductor Drive  
P.O. Box 58090  
Santa Clara, CA 95052-8090  
Tel: 1 (800) 272-9959  
TWX: (910) 339-9240

**National Semiconductor GmbH**  
Livry-Gargan-Str. 10  
D-82256 Fürstenfeldbruck  
Germany  
Tel: (81-41) 35-0  
Telex: 527649  
Fax: (81-41) 35-1

**National Semiconductor Japan Ltd.**  
Sumitomo Chemical  
Engineering Center  
Bldg. 7F  
1-7-1, Nakase, Mihama-Ku  
Chiba-City,  
Chiba Prefecture 261  
Tel: (043) 299-2300  
Fax: (043) 299-2500

**National Semiconductor Hong Kong Ltd.**  
13th Floor, Straight Block,  
Ocean Centre, 5 Canton Rd.  
Tsimshatsui, Kowloon  
Hong Kong  
Tel: (852) 2737-1600  
Fax: (852) 2736-9960

**National Semiconductores Do Brazil Ltda.**  
Rue Deputado Lacorda Franco  
120-3A  
Sao Paulo-SP  
Brazil 05418-000  
Tel: (55-11) 212-5066  
Telex: 391-1131931 NSBR BR  
Fax: (55-11) 212-1181

**National Semiconductor (Australia) Pty, Ltd.**  
Building 16  
Business Park Drive  
Monash Business Park  
Nottingham, Melbourne  
Victoria 3168 Australia  
Tel: (3) 558-9889  
Fax: (3) 558-9998

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