National Semiconductor

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54F/74F2640 • 54F/74F2643 • 54F/74F2645 Octal Bus Transceiver with 25Ω Series Resistors in the Outputs

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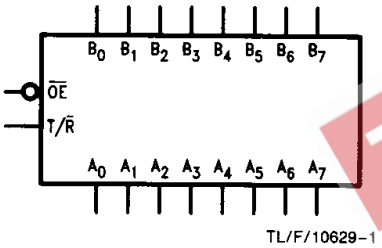
General Description

These devices are octal bus transceivers designed for asynchronous two-way data flow between the A and B busses. These devices are functionally equivalent to the 'F640, 'F643, and 'F645. The 25Ω series resistors in the outputs reduce ringing and eliminate the need for external resistors. Both busses are capable of sinking 12 mA, sourcing 15 mA, have TRI-STATE outputs, and a common output enable pin. The direction of data flow is determined by the transmit/receive ($T/\overline{R}$) input. The 'F2640 is an inverting version of the 'F2645. The 'F2643 has a noninverting A bus and an inverting B bus. The 'F2645 is a low power version of the 'F245 with 25Ω series resistors in the outputs.

Features

- 25Ω series resistors in the outputs eliminates the need for external resistors
- Designed for asynchronous two-way data flow between busses
- Outputs sink 12 mA and source 15 mA
- Transmit/receive ($T/\overline{R}$) input controls the direction of data flow
- Guaranteed 4000V minimum ESD protection
- 'F2645 is a low power version of the 'F245 with 25Ω series resistors in the outputs
- 'F2640 is an inverting option of the 'F2645
- 'F2643 has noninverting A bus and inverting B bus

Logic Symbol



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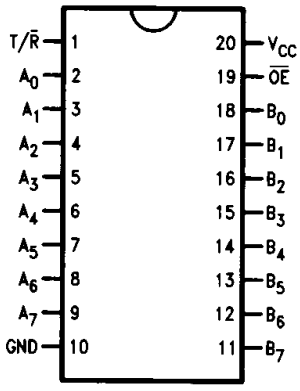
Unit Loading/Fan Out

Pin Names	Description	54F/74F	
		U.L. HIGH/LOW	Input I_{IH}/I_{IL} Output I_{OH}/I_{OL}
$\overline{OE}$	Output Enable Input (Active LOW)	1.0/1.0	20 μA/−0.6 mA
$T/\overline{R}$	Transmit/Receive Input	1.0/1.0	20 μA/−0.6 mA
A_0–A_7	Side A Inputs or	3.5/0.667	70 μA/−0.4 mA
	TRI-STATE Outputs	750/20	−15 mA/12 mA
B_0–B_7	Side B Inputs or	3.5/0.667	70 μA/−0.4 mA
	TRI-STATE Outputs	750/20	−15 mA/12 mA

Connection Diagrams

Pin Assignment for DIP, SOIC and Flatpak



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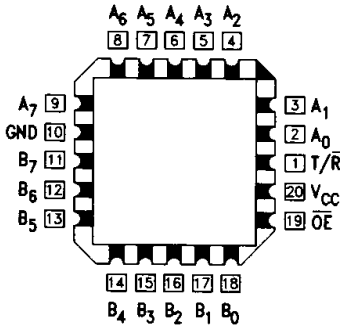
Pin Assignment for LCC and PCC



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Functional Description

The output enable ($\overline{OE}$) is active LOW. If the device is disabled ($\overline{OE}$ HIGH), the outputs are in the high impedance state. The transmit/receive input (T/$\overline{R}$) controls whether data is transmitted from the A bus to the B bus or from the B bus to the A bus. When T/$\overline{R}$ is LOW, B data is sent to the A bus. If T/$\overline{R}$ is HIGH, A data is sent to the B bus.

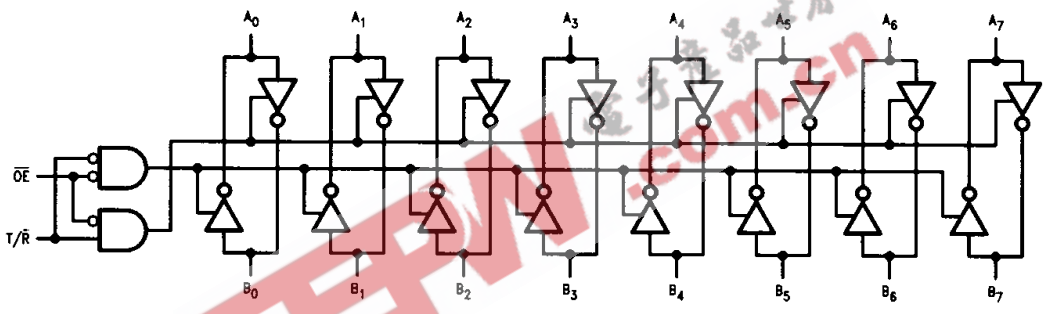
Function Table

Inputs		Outputs		
$\overline{OE}$	T/$\overline{R}$	'F2640	'F2643	'F2645
L	L	Bus $\overline{B}$ data to Bus A	Bus B data to Bus A	Bus B data to Bus A
L	H	Bus $\overline{A}$ data to Bus B	Bus $\overline{A}$ data to Bus B	Bus A data to Bus B
H	X	Z	Z	Z

H = High voltage level
L = Low voltage level
X = Don't care
Z = High-impedance state

Logic Diagrams

'F2640



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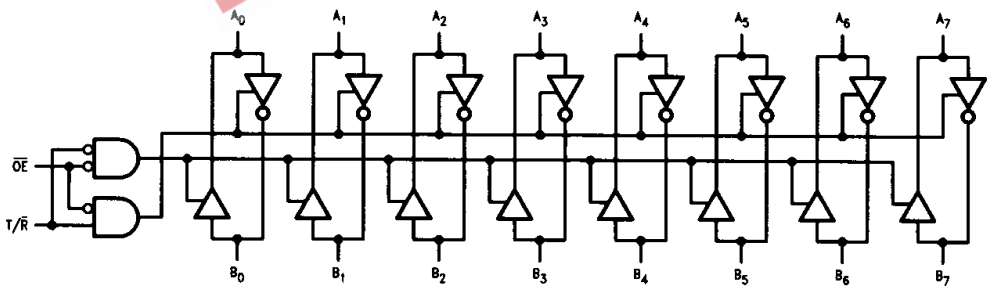
'F2643



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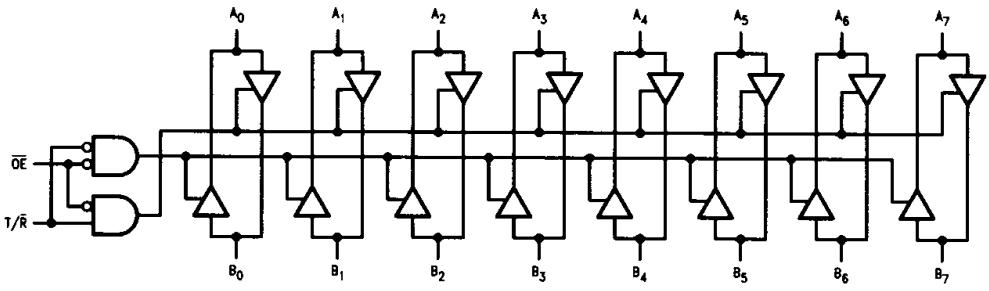
'F2645



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Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	−55°C to +175°C
V_{CC} Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V_{CC} = 0V)	
Standard Output	−0.5V to V_{CC}
TRI-STATE Output	−0.5V to +5.5V
Current Applied to Output in LOW State (Max)	twice the rated I_{OL} (mA)
ESD Last Passing Voltage (Min)	4000V

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

Recommended Operating Conditions

Free Air Ambient Temperature	
Military	−55°C to +125°C
Commercial	0°C to +70°C
Supply Voltage	
Military	+4.5V to +5.5V
Commercial	+4.5V to +5.5V

DC Electrical Characteristics

Symbol	Parameter		54F/74F Min	54F/74F Typ	54F/74F Max	Units	V_{CC}	Conditions
V_{IH}	Input HIGH Voltage		2.0			V		Recognized as a HIGH Signal
V_{IL}	Input LOW Voltage				0.8	V		Recognized as a LOW Signal
V_{CD}	Input Clamp Diode Voltage				−1.2	V	Min	I_{IN} = −18 mA (Non I/O Pins)
V_{OH}	Output HIGH Voltage	54F 10% V_{CC} 74F 10% V_{CC}	2.0 2.0			V	Min	I_{OH} = −12 mA (A_n, B_n) I_{OH} = −15 mA (A_n, B_n)
V_{OL}	Output LOW Voltage	74F 10% V_{CC} 74F 10% V_{CC}			0.50 0.75	V	Min	I_{OL} = 1 mA (A_n, B_n) I_{OL} = 12 mA (A_n, B_n)
I_{IH}	Input HIGH Current	54F 74F			20.0 5.0	μA	Max	V_{IN} = 2.7V (Non I/O Pins)
I_{BVI}	Input HIGH Current Breakdown Test	54F 74F			100 7.0	μA	Max	V_{IN} = 7.0V (Non I/O Pins)
I_{BVIT}	Input HIGH Current Breakdown (I/O)	54F 74F			1.0 0.5	mA	Max	V_{IN} = 5.5V (A_n, B_n)
I_{CEX}	Output HIGH Leakage Current	54F 74F			250 50	μA	Max	V_{OUT} = V_{CC}
V_{ID}	Input Leakage Test	74F	4.75			V	0.0	I_{ID} = 1.9 μA All Other Pins Grounded
I_{OD}	Output Leakage Circuit Current	74F			3.75	μA	0.0	V_{IOD} = 150 mV All Other Pins Grounded
I_{IL}	Input LOW Current				−0.6	mA	Max	V_{IN} = 0.5V (Non I/O Pins)
I_{IH} + I_{OZH}	Output Leakage Current				70	μA	Max	V_{OUT} = 2.7V (A_n, B_n)
I_{IL} + I_{OZL}	Output Leakage Current				−650	μA	Max	V_{OUT} = 0.5V (A_n, B_n)
I_{OS}	Output Short-Circuit Current		−100		−225	mA	Max	V_{OUT} = 0V
I_{ZZ}	Bus Drainage Test				500	μA	0.0V	V_{OUT} = 5.25
I_{CCH}	Power Supply Current ('F2640)				82	mA	Max	V_O = HIGH, V_{IN} = 0.2V
I_{CCL}	Power Supply Current ('F2640)				82	mA	Max	V_O = LOW
I_{CCZ}	Power Supply Current ('F2640)				95	mA	Max	V_O = HIGH Z
I_{CCH}	Power Supply Current ('F2643)				82	mA	Max	V_O = HIGH, V_{IN} = 0.2V (A_n)
I_{CCL}	Power Supply Current ('F2643)				82	mA	Max	V_O = LOW, V_{IN} = 0.2V (B_n)
I_{CCZ}	Power Supply Current ('F2643)				95	mA	Max	V_O = HIGH Z
I_{CCH}	Power Supply Current ('F2645)				82	mA	Max	V_O = HIGH
I_{CCL}	Power Supply Current ('F2645)				82	mA	Max	V_O = LOW, V_{IN} = 0.2V
I_{CCZ}	Power Supply Current ('F2645)				95	mA	Max	V_O = HIGH Z

'F2640 AC Electrical Characteristics:

Symbol	Parameter	74F $T_A = +25°C$, $V_{CC} = +5.0V$, $C_L = 50$ pF			54F T_A, V_{CC} = Mil, $C_L = 50$ pF		74F T_A, V_{CC} = Com, $C_L = 50$ pF		Units
		Min	Typ	Max	Min	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation Delay A Input to B Output	2.5 2.5		7.5 7.5			2.0 2.5	8.0 7.5	ns
t_{PLH} t_{PHL}	Propagation Delay B Input to A Output	2.5 2.5		7.5 7.5			2.0 2.5	8.0 7.5	ns
t_{PZH} t_{PZL}	Enable Time $\overline{OE}$ Input to A Output	2.5 2.5		7.5 8.0			2.0 2.0	9.0 8.5	ns
t_{PHZ} t_{PLZ}	Disable Time $\overline{OE}$ Input to A Output	1.5 1.5		7.0 6.0			1.0 1.5	7.5 6.0	
t_{PZH} t_{PZL}	Enable Time $\overline{OE}$ Input to B Output	2.5 2.5		7.5 8.0			2.0 2.0	9.0 8.5	ns
t_{PHZ} t_{PLZ}	Disable Time $\overline{OE}$ Input to B Output	1.5 1.5		6.5 6.0			1.0 1.5	7.5 6.0	

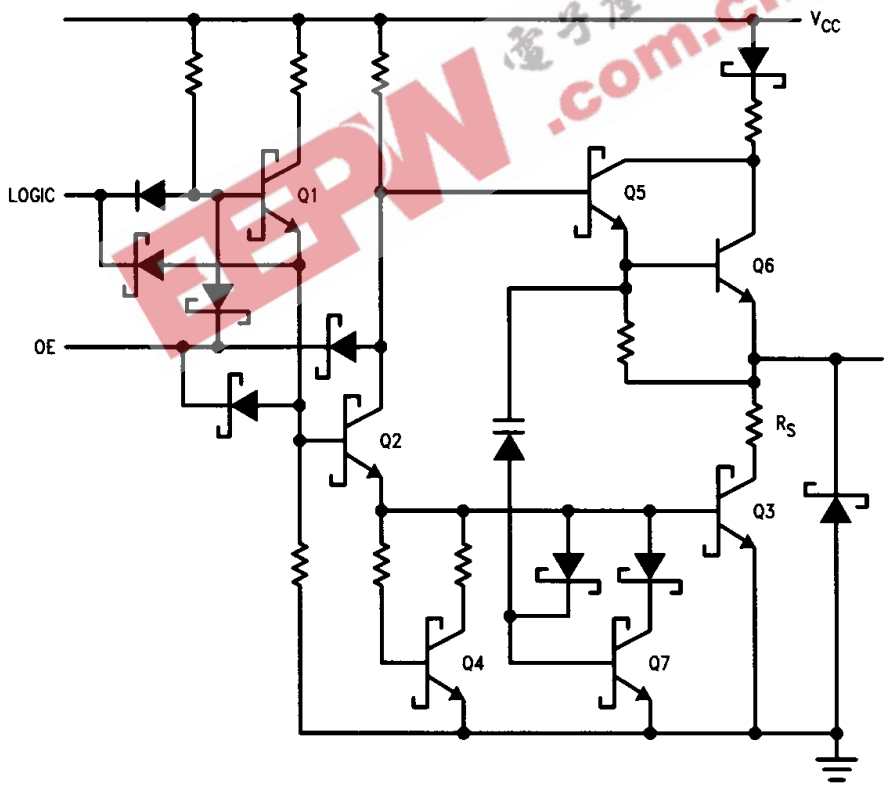
'F2643 AC Electrical Characteristics:

Symbol	Parameter	74F $T_A = +25°C$, $V_{CC} = +5.0V$, $C_L = 50$ pF			54F T_A, V_{CC} = Mil, $C_L = 50$ pF		74F T_A, V_{CC} = Com, $C_L = 50$ pF		Units
		Min	Typ	Max	Min	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation Delay A Input to B Output	2.5 2.5		7.5 7.5			2.0 2.5	8.0 7.5	ns
t_{PLH} t_{PHL}	Propagation Delay B Input to A Output	2.5 2.5		7.0 7.5			2.5 2.5	8.0 8.0	ns
t_{PZH} t_{PZL}	Enable Time $\overline{OE}$ Input to A Output	2.5 2.5		8.0 8.5			2.0 2.0	9.0 8.5	ns
t_{PHZ} t_{PLZ}	Disable Time $\overline{OE}$ Input to A Output	1.5 1.0		7.0 5.5			1.0 1.0	8.0 5.5	
t_{PZH} t_{PZL}	Enable Time $\overline{OE}$ Input to B Output	2.5 2.5		7.5 8.0			2.0 2.0	9.0 8.5	ns
t_{PHZ} t_{PLZ}	Disable Time $\overline{OE}$ Input to B Output	1.5 1.5		6.5 6.0			1.0 1.5	7.5 6.0	

'F2645 AC Electrical Characteristics:

Symbol	Parameter	74F $T_A = +25°C$, $V_{CC} = +5.0V$, $C_L = 50$ pF			54F T_A, V_{CC} = Mil, $C_L = 50$ pF		74F T_A, V_{CC} = Com, $C_L = 50$ pF		Units
		Min	Typ	Max	Min	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation Delay A Input to B Output	1.5 2.5		6.0 7.5			1.5 2.5	7.0 8.0	ns
t_{PLH} t_{PHL}	Propagation Delay B Input to A Output	1.5 2.5		6.0 7.5			1.5 2.5	7.0 8.0	ns
t_{PZH} t_{PZL}	Enable Time $\overline{OE}$ Input to A Output	2.5 2.5		8.0 8.5			2.0 2.0	9.0 8.5	ns
t_{PHZ} t_{PLZ}	Disable Time $\overline{OE}$ Input to A Output	1.5 1.0		7.0 5.5			1.0 1.0	8.0 5.5	
t_{PZH} t_{PZL}	Enable Time $\overline{OE}$ Input to B Output	2.5 2.5		7.5 8.5			2.0 2.5	9.5 9.0	ns
t_{PHZ} t_{PLZ}	Disable Time $\overline{OE}$ Input to B Output	1.5 1.0		6.5 6.5			1.0 1.0	7.5 6.5	

Basic FAST Circuit Showing Series Resistor Placement



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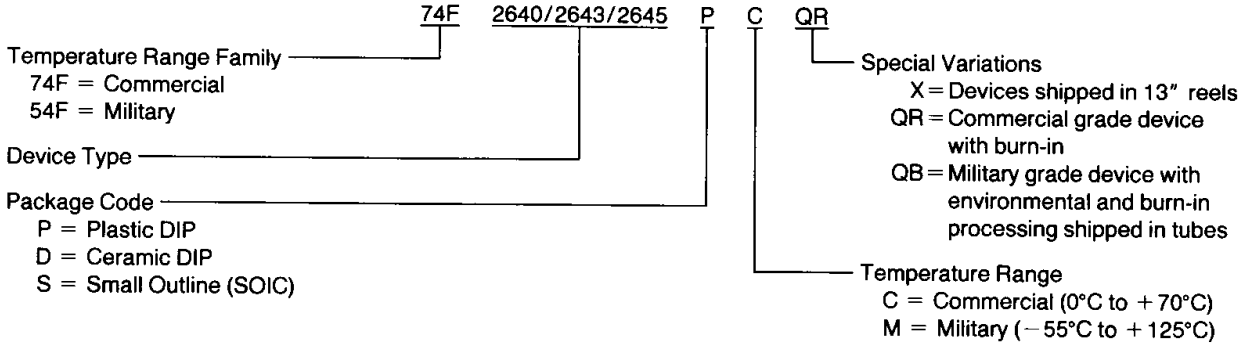
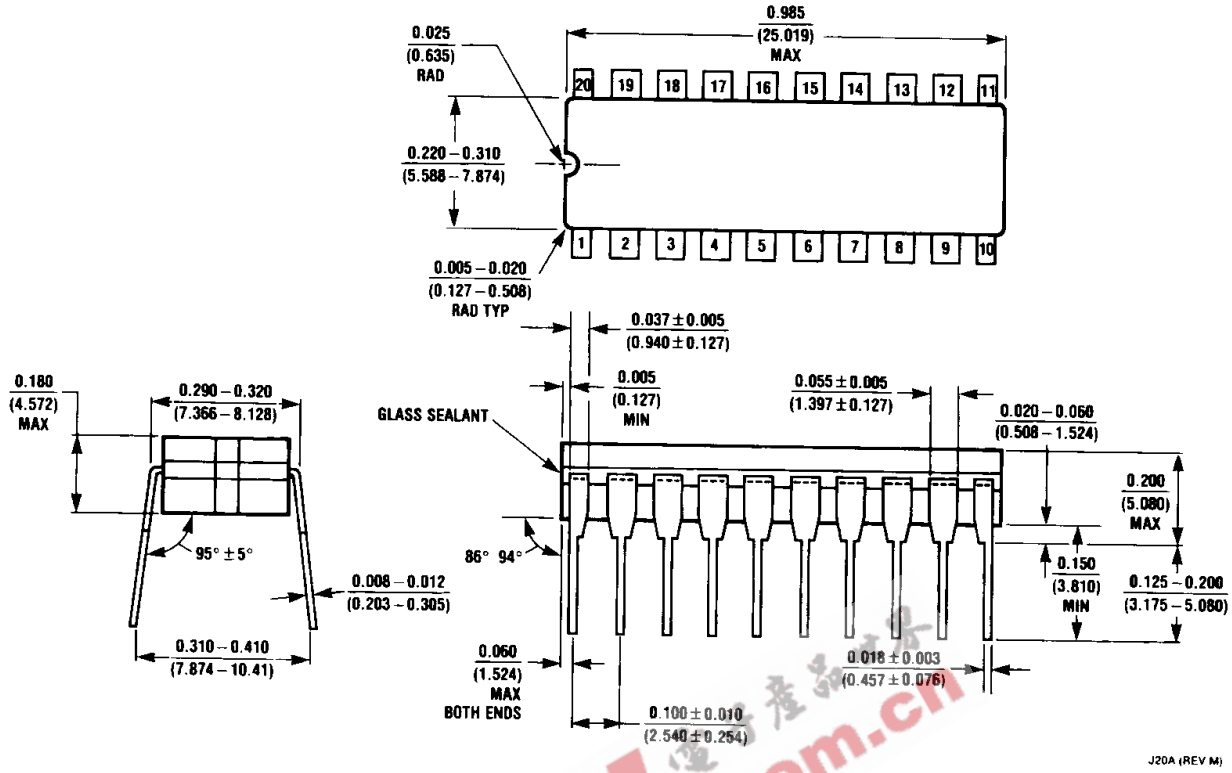
Ordering Information

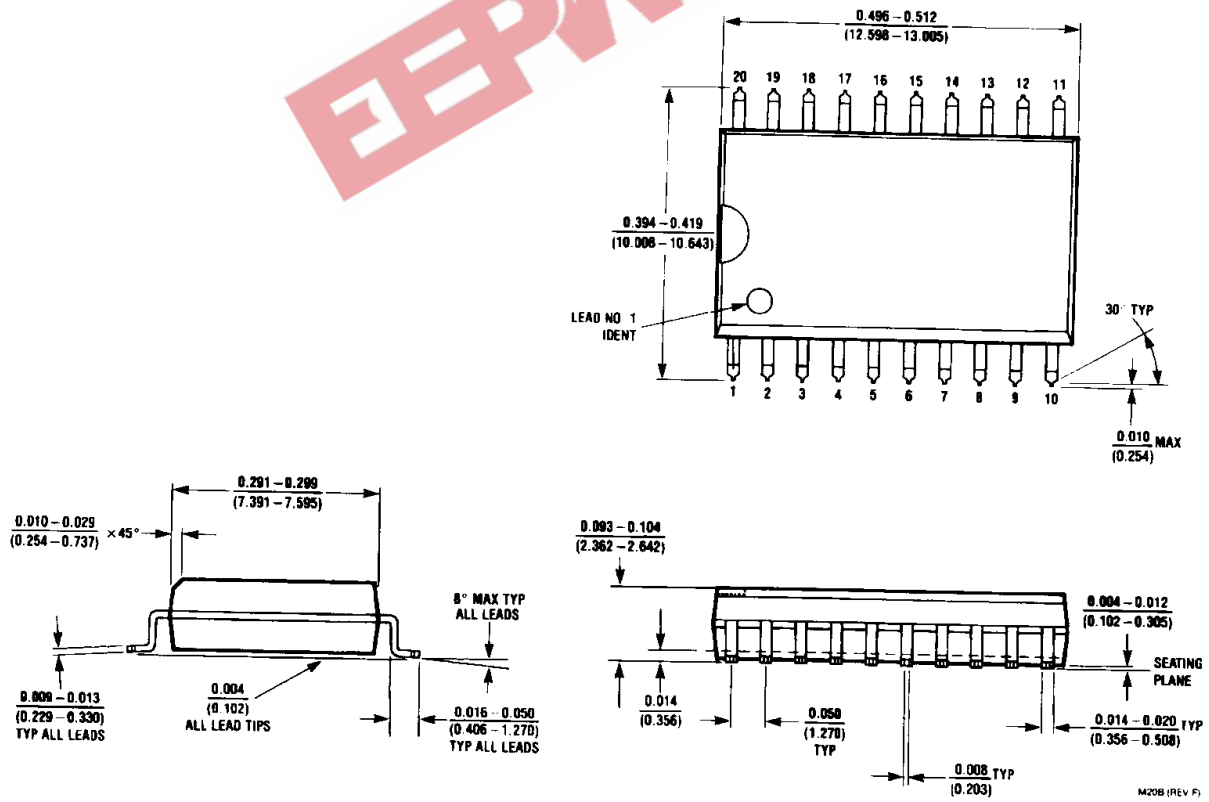
The device number is used to form part of a simplified purchasing code where a package type and temperature range are defined as follows:



Physical Dimensions inches (millimeters)



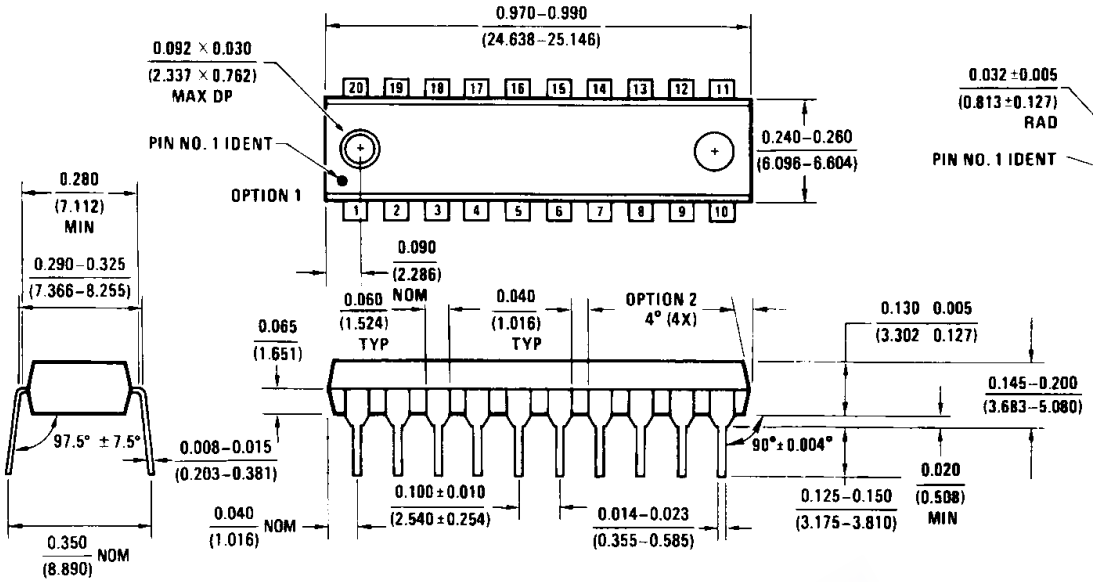
20-Lead Ceramic Dual-In-Line Package (D)
NS Package Number J20A



20-Lead Small Outline Integrated Circuit (S)
NS Package Number M20B

Physical Dimensions inches (millimeters) (Continued)

Lit. # 114659



20-Lead Plastic Dual-In-Line Package (P)
NS Package Number N20B

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