

## 54ACT825 8-Bit D Flip-Flop

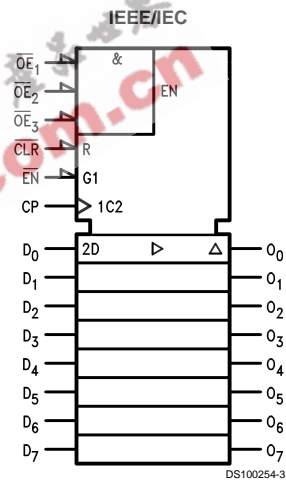
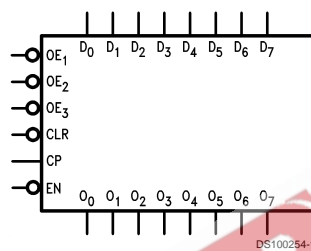
### General Description

The 'ACT825 is an 8-bit buffered register. They have Clock Enable and Clear features which are ideal for parity bus interfacing in high performance microprogramming systems. Also included are multiple enables that allow multi-use control of the interface. The 'ACT825 has noninverting outputs and is fully compatible with AMD's Am29825.

### Features

- Outputs source/sink 24 mA
- Inputs and outputs are on opposite sides
- 'ACT825 has TTL-compatible inputs
- Standard Microcircuit Drawing (SMD)
  - 'ACT825: 5962-91611

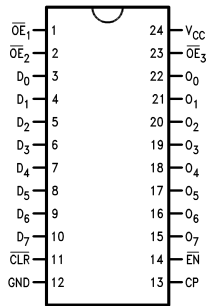
### Logic Symbols



Pin Names	Description
D <sub>0</sub> -D <sub>7</sub>	Data Inputs
O <sub>0</sub> -O <sub>7</sub>	Data Outputs
$\overline{OE}_1, \overline{OE}_2, \overline{OE}_3$	Output Enables
$\overline{EN}$	Clock Enable
$\overline{CLR}$	Clear
CP	Clock Input

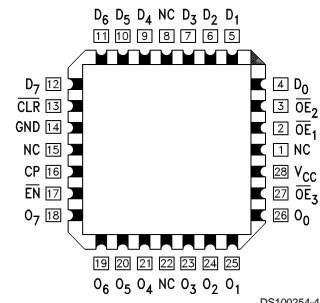
## Connection Diagrams

Pin Assignment  
for DIP and Flatpak



DS100254-2

Pin Assignment for LCC



DS100254-4

## Functional Description

The 'ACT825 consists of eight D-type edge-triggered flip-flops. These devices have TRI-STATE® outputs for bus systems, organized in a broadside pinning. In addition to the clock and output enable pins, the buffered clock (CP) and buffered Output Enable (OE) are common to all flip-flops. The flip-flops will store the state of their individual D inputs that meet the setup and hold time requirements on the LOW-to-HIGH CP transition. With OE<sub>1</sub>, OE<sub>2</sub> and OE<sub>3</sub> LOW, the contents of the flip-flops are available at the outputs. When one of OE<sub>1</sub>, OE<sub>2</sub> or OE<sub>3</sub> is HIGH, the outputs go to the high impedance state.

Operation of the OE input does not affect the state of the flip-flops. The 'ACT825 has Clear (CLR) and Clock Enable (EN) pins. These pins are ideal for parity bus interfacing in high performance systems.

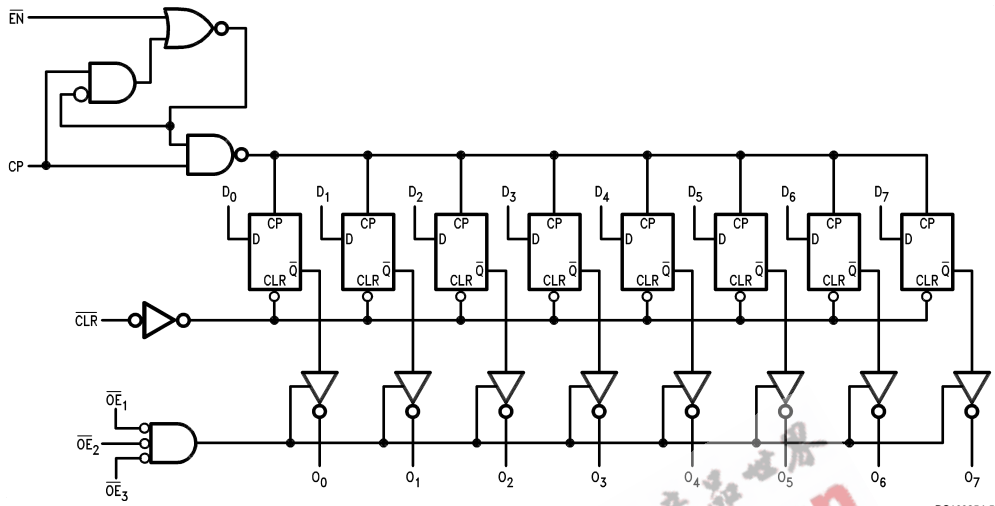
When CLR is LOW and OE is LOW, the outputs are LOW. When CLR is HIGH, data can be entered into the flip-flops. When EN is LOW, data on the inputs is transferred to the outputs on the LOW-to-HIGH clock transition. When EN is HIGH, the outputs do not change state, regardless of the data or clock input transitions.

## Function Table

Inputs					Internal	Output	Function
OE	CLR	EN	CP	D <sub>n</sub>	Q	O	
H	X	L	↗	L	L	Z	High-Z
H	X	L	↗	H	H	Z	High-Z
H	L	X	X	X	L	Z	Clear
L	L	X	X	X	L	L	Clear
H	H	H	X	X	NC	Z	Hold
L	H	H	X	X	NC	NC	Hold
H	H	L	↗	L	L	Z	Load
H	H	L	↗	H	H	Z	Load
L	H	L	↗	L	L	L	Load
L	H	L	↗	H	H	H	Load

H = HIGH Voltage Level  
 L = LOW Voltage Level  
 X = Immaterial  
 Z = High Impedance  
 ↗ = LOW-to-HIGH Transition  
 NC = No Change

## Logic Diagram



DS100254-5

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

EEPW.com.cn

## Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage ( $V_{CC}$ )	-0.5V to 7.0V
DC Input Diode Current ( $I_{IK}$ )	
$V_I = -0.5V$	-20 mA
$V_I = V_{CC} + 0.5V$	+20 mA
DC Input Voltage ( $V_I$ )	-0.5V to $V_{CC} + 0.5V$
DC Output Diode Current ( $I_{OK}$ )	
$V_O = -0.5V$	-20 mA
$V_O = V_{CC} + 0.5V$	+20 mA
DC Output Voltage ( $V_O$ )	+0.5V
DC Output Source or Sink Current ( $I_O$ )	±50 mA
DC $V_{CC}$ or Ground Current	
Per Output Pin ( $I_{CC}$ or $I_{GND}$ )	±50 mA
Storage Temperature ( $T_{STG}$ )	-65°C to +150°C

Junction Temperature ( $T_J$ )

CDIP

175°C

## Recommended Operating Conditions

Supply Voltage ( $V_{CC}$ )	
'ACT	4.5V to 5.5V
Input Voltage ( $V_I$ )	0V to $V_{CC}$
Output Voltage ( $V_O$ )	0V to $V_{CC}$
Operating Temperature ( $T_A$ )	
54ACT	-55°C to +125°C
Minimum Input Edge Rate ( $\Delta V/\Delta t$ )	
'ACT Devices	
$V_{IN}$ from 0.8V to 2.0V	
$V_{CC}$ @ 4.5V, 5.5V	125 mV/ns

**Note 1:** Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT™ circuits outside databook specifications.

## DC Electrical Characteristics

Symbol	Parameter	$V_{CC}$ (V)	54ACT	Units	Conditions
			$T_A =$ -55°C to +125°C		
			Guaranteed Limits		
$V_{IH}$	Minimum High Level Input Voltage	4.5	2.0	V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$
		5.5	2.0		
$V_{IL}$	Maximum Low Level Input Voltage	4.5	0.8		$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$
		5.5	0.8		
$V_{OH}$	Minimum High Level	4.5	4.4	V	$I_{OUT} = -50 \mu A$
		5.5	5.4		
		4.5	3.70	V	(Note 2) $V_{IN} = V_{IL}$ or $V_{IH}$ $I_{OH} = -24 mA$ $I_{OH} = -24 mA$
		5.5	4.70		
$V_{OL}$	Maximum Low Level Output Voltage	4.5	0.1	V	$I_{OUT} = 50 \mu A$
		5.5	0.1		
		4.5	0.50	V	(Note 2) $V_{IN} = V_{IL}$ or $V_{IH}$ $I_{OL} = 24 mA$ $I_{OL} = 24 mA$
		5.5	0.50		
$I_{IN}$	Maximum Input Leakage Current	5.5	±1.0	μA	$V_I = V_{CC}, GND$
$I_{OZ}$	Maximum TRI-STATE Current	5.5	±10.0	μA	$V_I = V_{IL}, V_{IH}$ $V_O = V_{CC}, GND$
$I_{CCT}$	Maximum $I_{CC}$ /Input	5.5	1.6	mA	$V_I = V_{CC} - 2.1V$
$I_{OLD}$	(Note 3) Minimum Dynamic	5.5	50	mA	$V_{OLD} = 1.65V$ Max
$I_{OHD}$	Output Current	5.5	-50	mA	$V_{OHD} = 3.85V$ Min
$I_{CC}$	Maximum Quiescent Supply Current	5.5	160	μA	$V_{IN} = V_{CC}$ or GND

**Note 2:** All outputs loaded; thresholds on input associated with output under test.

**Note 3:** Maximum test duration 2.0 ms, one output loaded at a time.

## DC Electrical Characteristics (Continued)

Note 4:  $I_{CC}$  limit for 54ACT @ 25°C is identical to 74ACT @ 25°C.

## AC Electrical Characteristics

Symbol	Parameter	$V_{CC}$ (V) (Note 5)	54ACT		Units	Fig. No.
			$T_A = -55^\circ\text{C}$ to $+125^\circ\text{C}$ $C_L = 50\text{ pF}$			
			Min	Max		
$f_{max}$	Maximum Clock Frequency	5.0	95		MHz	
$t_{PLH}$	Propagation Delay CP to $O_n$	5.0	1.5	11.5	ns	
$t_{PHL}$	Propagation Delay CP to $O_n$	5.0	1.5	11.5	ns	
$t_{PHL}$	Propagation Delay $\overline{\text{CLR}}$ to $O_n$	5.0	1.5	18.0	ns	
$t_{PZH}$	Output Enable Time $\overline{\text{OE}}$ to $O_n$	5.0	1.5	11.5	ns	
$t_{PZL}$	Output Enable Time $\overline{\text{OE}}$ to $O_n$	5.0	1.5	12.5	ns	
$t_{PHZ}$	Output Disable Time $\overline{\text{OE}}$ to $O_n$	5.0	1.5	13.5	ns	
$t_{PLZ}$	Output Disable Time $\overline{\text{OE}}$ to $O_n$	5.0	1.5	13.0	ns	

Note 5: Voltage Range 5.0 is 5.0V  $\pm 0.5V$

## AC Operating Requirements

Symbol	Parameter	$V_{CC}$ (V) (Note 6)	54ACT		Units	Fig. No.
			$T_A = -55^\circ\text{C}$ to $+125^\circ\text{C}$ $C_L = 50\text{ pF}$			
			Guaranteed Minimum			
$t_s$	Setup Time, HIGH or LOW $D_n$ to CP	5.0	4.0		ns	
$t_h$	Hold Time, HIGH or LOW $D_n$ to CP	5.0	2.5		ns	
$t_s$	Setup Time, HIGH or LOW $\overline{\text{EN}}$ to CP	5.0	4.0		ns	
$t_h$	Hold Time, HIGH or LOW $\overline{\text{EN}}$ to CP	5.0	2.0		ns	
$t_w$	CP Pulse Width HIGH or LOW	5.0	6.0		ns	
$t_w$	$\overline{\text{CLR}}$ Pulse Width, LOW	5.0	7.0		ns	
$t_{rec}$	$\overline{\text{CLR}}$ to CP Recovery Time	5.0	4.5		ns	

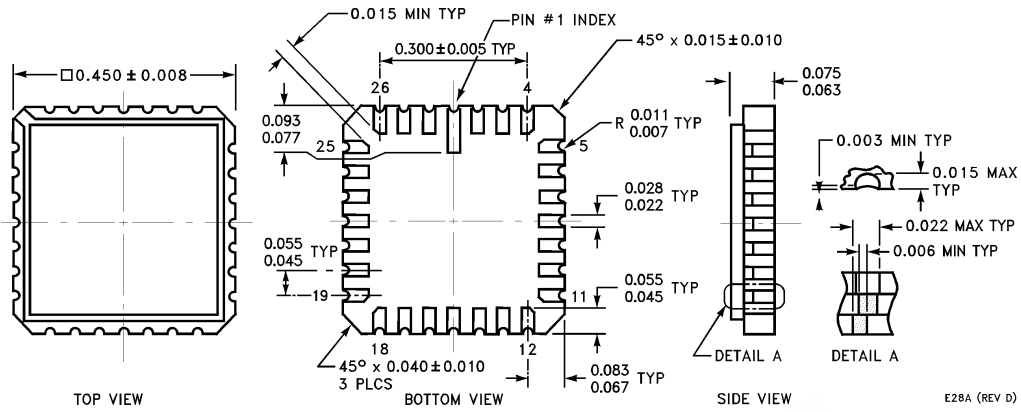
Note 6: Voltage Range 5.0 is 5.0V  $\pm 0.5V$

## Capacitance

Symbol	Parameter	Typ	Units	Conditions
$C_{IN}$	Input Capacitance	4.5	pF	$V_{CC} = OPEN$
$C_{PD}$	Power Dissipation Capacitance	44	pF	$V_{CC} = 5.0V$

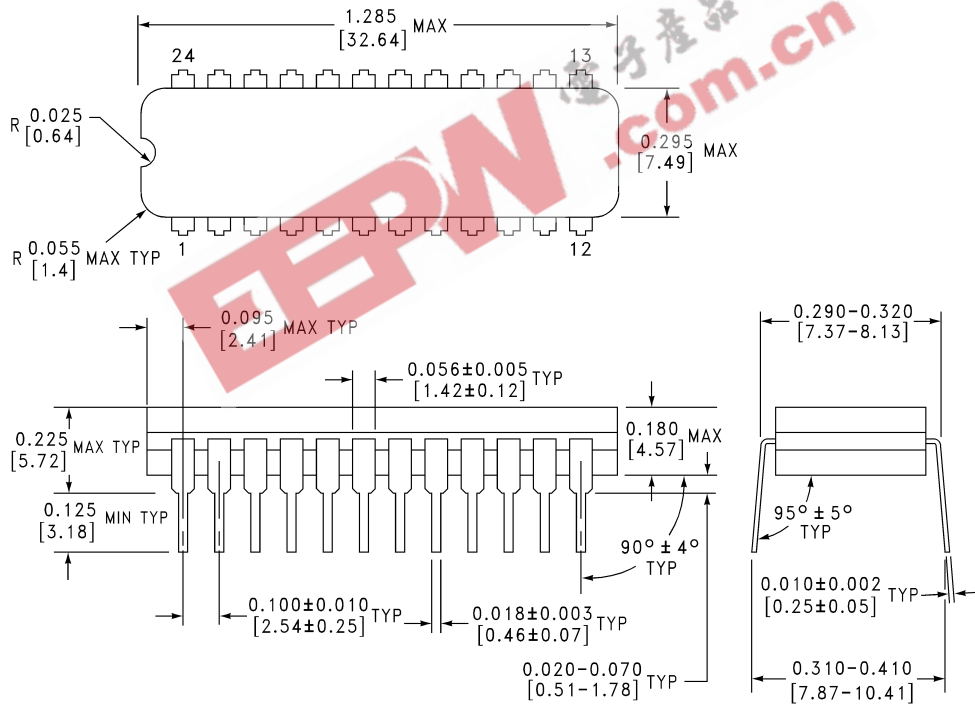
EEPW 电子产品世界  
.com.cn

**Physical Dimensions** inches (millimeters) unless otherwise noted



**28-Terminal Ceramic Leadless Chip Carrier (L)**  
NS Package Number E28A

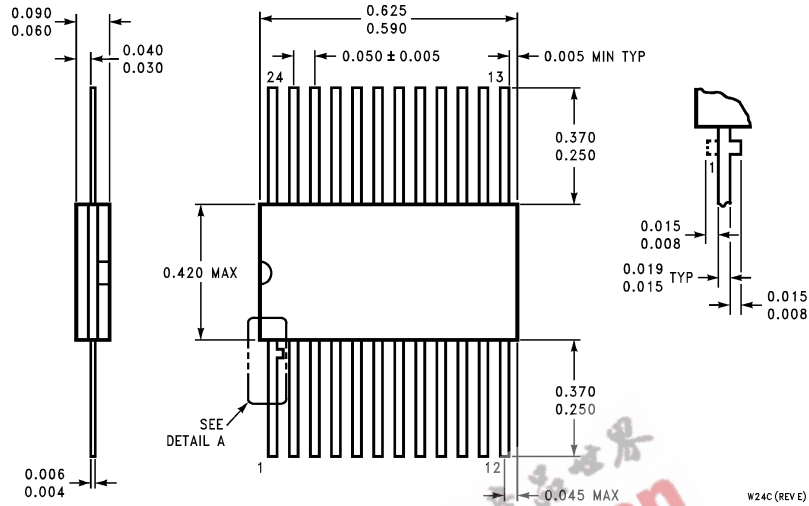
E28A (REV D)



**24 Lead Slim (0.300" Wide) Ceramic Dual-In-Line (SD)**  
NS Package Number J24F

J24F (REV. H)

**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



**24 Lead Ceramic Flatpak (F)**  
NS Package Number W24C

W24C (REV E)

**LIFE SUPPORT POLICY**

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.



**National Semiconductor Corporation**  
Americas  
Tel: 1-800-272-9959  
Fax: 1-800-737-7018  
Email: support@nsc.com

**National Semiconductor Europe**  
Fax: +49 (0) 1 80-530 85 86  
Email: europe.support@nsc.com  
Deutsch Tel: +49 (0) 1 80-530 85 85  
English Tel: +49 (0) 1 80-532 78 32  
Français Tel: +49 (0) 1 80-532 93 58  
Italiano Tel: +49 (0) 1 80-534 16 80

**National Semiconductor Asia Pacific Customer Response Group**  
Tel: 65-2544466  
Fax: 65-2504466  
Email: sea.support@nsc.com

**National Semiconductor Japan Ltd.**  
Tel: 81-3-5639-7560  
Fax: 81-3-5639-7507

www.national.com