National Semiconductor

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54ACTQ544
Quiet Series Octal Registered Transceiver with TRI-STATE® Outputs

General Description

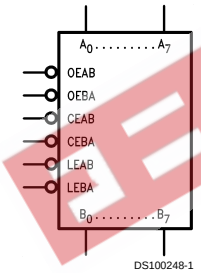
The ACTQ544 is an inverting octal transceiver containing two sets of D-type registers for temporary storage of data flowing in either direction. Separate Latch Enable and Output Enable inputs are provided for each register to permit independent input and output control in either direction of data flow. The '544 inverts data in both directions.

The ACTQ utilizes NSC Quiet Series technology to guarantee quiet output switching and improved dynamic threshold performance. FACT Quiet Series™ features GTO™ output control and undershoot corrector in addition to a split ground bus for superior performance.

Features

- Guaranteed simultaneous switching noise level and dynamic threshold performance
- 8-bit inverting octal latched transceiver
- Separate controls for data flow in each direction
- Back-to-back registers for storage
- Outputs source/sink 24 mA
- 4 kV minimum ESD immunity

Logic Symbols



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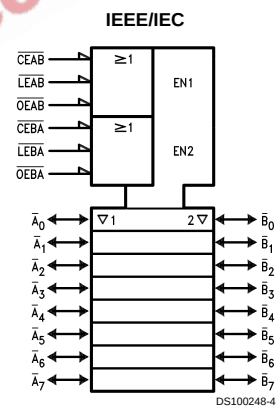

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Pin Names	Description
$\overline{OEAB}$	A-to-B Output Enable Input (Active LOW)
$\overline{OEBA}$	B-to-A Output Enable Input (Active LOW)
$\overline{CEAB}$	A-to-B Enable Input (Active LOW)
$\overline{CEBA}$	B-to-A Enable Input (Active LOW)
$\overline{LEAB}$	A-to-B Latch Enable Input (Active LOW)
$\overline{LEBA}$	B-to-A Latch Enable Input (Active LOW)
$\overline{A_0}$ –$\overline{A_7}$	A-to-B Data Inputs or B-to-A TRI-STATE Outputs
$\overline{B_0}$ –$\overline{B_7}$	B-to-A Data Inputs or A-to-B TRI-STATE Outputs

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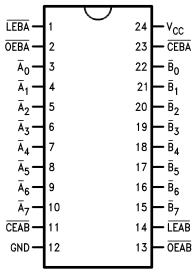
FACT® is a registered trademark of Fairchild Semiconductor Corporation.
FACT Quiet Series™ is a trademark of Fairchild Semiconductor Corporation.

Connection Diagrams

Pin Assignment for DIP and Flatpak



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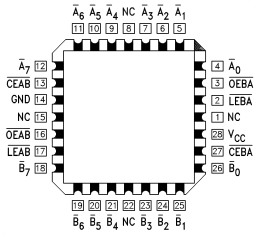
Pin Assignment for LCC



DS100248-3

Functional Description

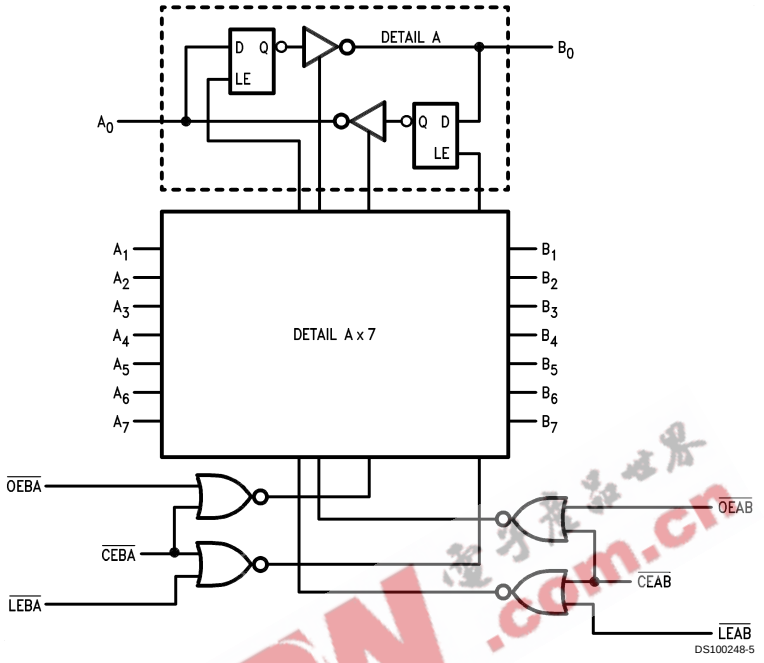
The ACTQ544 contains two sets of eight D-type latches, with separate input and output controls for each set. For data flow from A to B, for example, the A-to-B Enable ($\overline{CEAB}$) input must be LOW in order to enter data from $\overline{A_0}$–$\overline{A_7}$ or take data from $\overline{B_0}$–$\overline{B_7}$, as indicated in the Data I/O Control Table. With $\overline{CEAB}$ LOW, a LOW signal on the A-to-B Latch Enable ($\overline{LEAB}$) input makes the A-to-B latches transparent; a subsequent LOW-to-HIGH transition of the $\overline{LEAB}$ signal puts the A latches in the storage mode and their outputs no longer change with the A inputs. With $\overline{CEAB}$ and $\overline{OEAB}$ both LOW, the TRI-STATE B output buffers are active and reflect the data present at the output of the A latches. Control of data flow from B to A is similar, but using the $\overline{CEBA}$, $\overline{LEBA}$ and $\overline{OEBA}$ inputs.

Data I/O Control Table

Inputs			Latch	Output
$\overline{CEAB}$	$\overline{LEAB}$	$\overline{OEAB}$	Status	Buffers
H	X	X	Latched	High Z
X	H	X	Latched	—
L	L	X	Transparent	—
X	X	H	—	High Z
L	X	L	—	Driving

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
A-to-B data flow shown; B-to-A flow control is the same, except using $\overline{CEBA}$, $\overline{LEBA}$ and $\overline{OEBA}$

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
V_I = V_{CC} + 0.5V	+20 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} + 0.5V
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} + 0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to V_{CC} + 0.5V
DC Output Source or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND})	±50 mA
Storage Temperature (T_{STG})	−65˚C to +150˚C
DC Latch-up Source or Sink Current	±300 mA
Junction Temperature (T_J)	
CDIP	175˚C

Recommended Operating Conditions

Supply Voltage V_{CC}	
'ACTQ	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A) (Note 2)	
54ACTQ	−55˚C to +125˚C
Minimum Input Edge Rate ΔV/Δt	
'ACTQ Devices	
V_{IN} from 0.8V to 2.0V	
V_{CC} @ 4.5V, 5.5V	125 mV/ns

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT® circuits outside databook specifications.

Note 2: Surface mount and plastic dip packaging is not recommended for applications requiring greater than 2000 temperature cycles from −40˚C to +125˚C.

DC Characteristics for 'ACTQ Family Devices

Symbol	Parameter	V_{CC} (V)	54ACTQ T_A = −55˚C to +125˚C Guaranteed Limits	Units	Conditions
V_{IH}	Minimum High Level Input Voltage	4.5	2.0	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		5.5	2.0		
V_{IL}	Maximum Low Level Input Voltage	4.5	0.8	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		5.5	0.8		
V_{OH}	Minimum High Level Output Voltage	4.5	4.4	V	I_{OUT} = −50 μA
		5.5	5.4		
					(Note 3) V_{IN} = V_{IL} or V_{IH}
		4.5	3.70	V	I_{OH} = −24 mA
		5.5	4.70		I_{OH} = −24 mA
V_{OL}	Maximum Low Level Output Voltage	4.5	0.1	V	I_{OUT} = 50 μA
		5.5	0.1		
					(Note 3) V_{IN} = V_{IL} or V_{IH}
		4.5	0.50	V	I_{OL} = 24 mA
		5.5	0.50		I_{OL} = 24 mA
I_{IN}	Maximum Input Leakage Current	5.5	±1.0	μA	V_I = V_{CC}, GND
I_{OZT}	Maximum I/O Leakage Current	5.5	±10.0	μA	V_I, (OE) = V_{IL}, V_{IH} V_O = V_{CC}, GND
I_{CCT}	Maximum I_{CC}/Input	5.5	1.6	mA	V_I = V_{CC} − 2.1V

DC Characteristics for 'ACTQ Family Devices (Continued)

Symbol	Parameter	V_{CC} (V)	54ACTQ T_A = −55°C to +125°C Guaranteed Limits	Units	Conditions
I_{OLD}	Minimum Dynamic Output Current (Note 4)	5.5	50	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5	−50	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5	160.0	µA	V_{IN} = V_{CC} or GND (Note 5)
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	5.0	1.6	V	2–12, 13 (Notes 6, 7)
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	5.0	−1.2	V	2–12, 13 (Notes 6, 7)

Note 3: All outputs loaded; thresholds on input associated with output under test.

Note 4: Maximum test duration 2.0 ms, one output loaded at a time.

Note 5: I_{CC} for 54ACTQ @ 25°C is identical to 74ACTQ@ 25°C.

Note 6: Plastic DIP package.

Note 7: Max number of outputs defined as (n-1). Data Inputs are driven 0V to 3V, one output @ GND.

Note 8: Max number of Data Inputs (n) switching (n-1) inputs switching 0V to 3V ('ACTQ). Input-under-test switching: 3V to threshold (V_{ILD}), 0V to threshold (V_{IHD}), f = 1 MHz.

AC Electrical Characteristics

Symbol	Parameter	V_{CC} (V) (Note 9)	54ACTQ T_A = −55°C to +125°C C_L = 50 pF Min	54ACTQ Max	Units	Fig. No.
t_{PLH} t_{PHL}	Propagation Delay Transparent Mode A_n to B_n or B_n to A_n	5.0	2.0	9.5	ns	
t_{PLH} t_{PHL}	Propagation Delay $\overline{LEBA}$, $\overline{LEAB}$ to A_n, B_n	5.0	2.0	11.0	ns	
t_{PZH} t_{PZL}	Output Enable Time $\overline{OEBA}$ or $\overline{OEAB}$ to A_n or B_n $\overline{CEBA}$ or $\overline{CEAB}$ to A_n or B_n	5.0	1.5	13.0	ns	
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OEBA}$ or $\overline{OEAB}$ to A_n or B_n $\overline{CEBA}$ or $\overline{CEAB}$ to A_n or B_n	5.0	1.5	9.0	ns	

Note 9: Voltage Range 5.0 is 5.0V ±0.5V

Note 10: Skew is defined as the absolute value of the difference between the actual propagation delay for any two outputs within the same packaged device. The specification applies to any outputs switching in the same direction, either HIGH to LOW (t_{OSHL}) or LOW to HIGH (t_{OSLH}). Parameter guaranteed by design. Not tested.

AC Operating Requirements

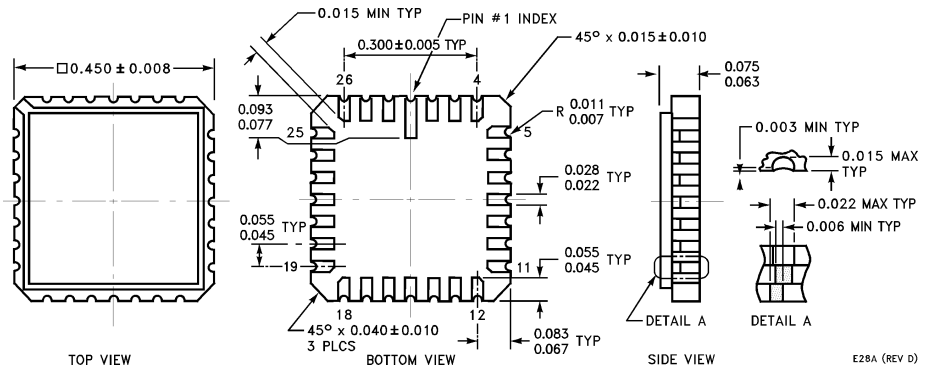
Symbol	Parameter	V_{CC} (V) (Note 11)	54ACTQ $T_A = -55^\circ C$ to $+125^\circ C$ $C_L = 50$ pF Guaranteed Minimum	Units	Fig. No.
t_s	Setup Time, HIGH or LOW A_n or B_n to $\overline{LEBA}$ or $\overline{LEAB}$	5.0	3.0	ns	
t_h	Hold Time, HIGH or LOW A_n or B_n to $\overline{LEBA}$ or $\overline{LEAB}$	5.0	1.5	ns	
t_w	Latch Enable, B to A Pulse Width, LOW	5.0	4.0	ns	

Note 11: Voltage Range 5.0 is 5.0V ±0.5V

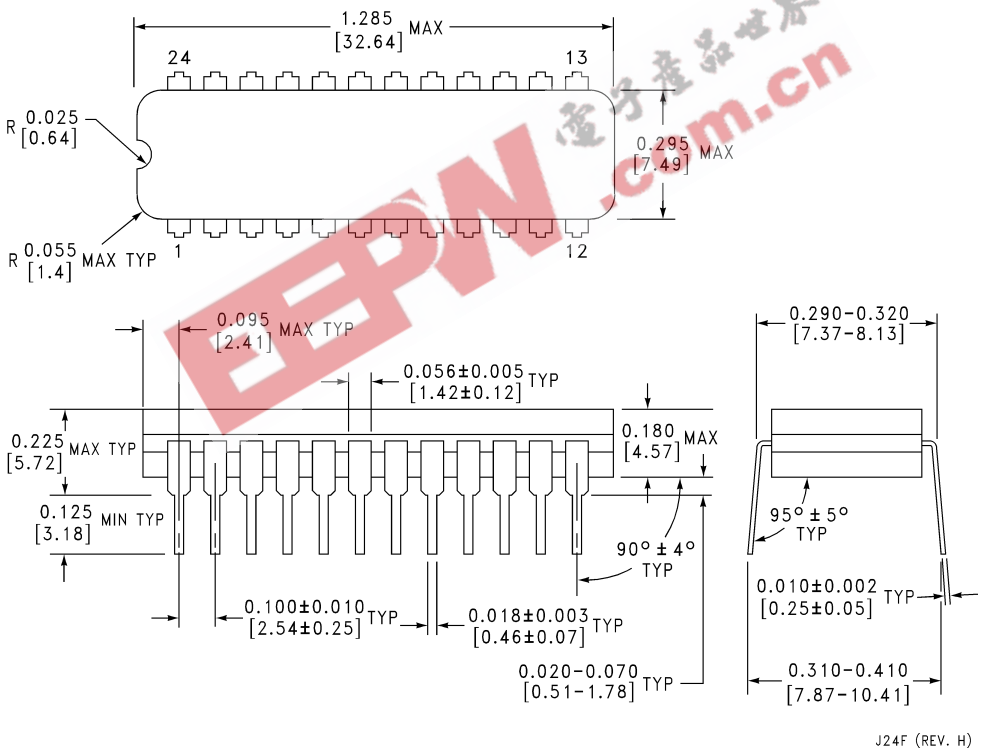
Capacitance

Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = 5.0V
C_{PD}	Power Dissipation Capacitance	80.0	pF	V_{CC} = 5.0V

Physical Dimensions inches (millimeters) unless otherwise noted

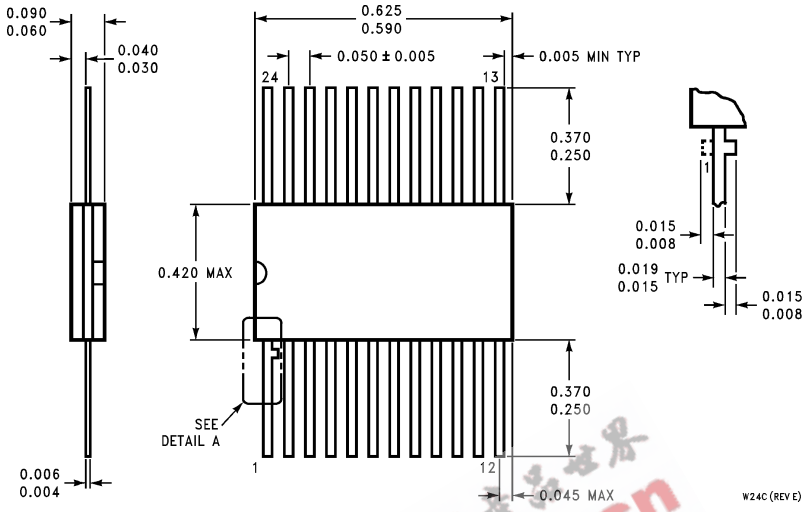


28-Terminal Ceramic Leadless Chip Carrier (L)
NS Package Number E28A



24-Lead Ceramic Dual-In-Line Package (D)
NS Package Number J24F

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



24-Lead Ceramic Flatpak (F)
NS Package Number W24C

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