National Semiconductor

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54ACT573
Octal Latch with TRI-STATE® Outputs

General Description

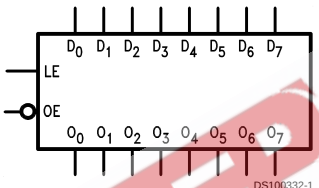
The 'ACT573 is a high-speed octal latch with buffered common Latch Enable (LE) and buffered common Output Enable ($\overline{OE}$) inputs.

The 'ACT573 is functionally identical to the 'ACT373 but has inputs and outputs on opposite sides.

Features

- I_{CC} and I_{OZ} reduced by 50%
- Inputs and outputs on opposite sides of package allowing easy interface with microprocessors
- Useful as input or output port for microprocessors
- Functionally identical to 'ACT373
- TRI-STATE outputs for bus interfacing
- Outputs source/sink 24 mA
- 'ACT573 has TTL-compatible inputs
- Standard Military Drawing (SMD)
  — 'ACT573: 5962-87664

Logic Symbols



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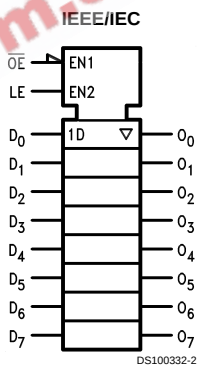

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Pin Names	Description
D_0–D_7	Data Inputs
LE	Latch Enable Input
$\overline{OE}$	TRI-STATE Output Enable Input
O_0–O_7	TRI-STATE Latch Outputs

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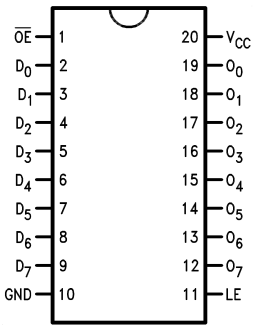
FACT® is a registered trademark of Fairchild Semiconductor Corporation.

Connection Diagrams

Pin Assignment for DIP and Flatpak



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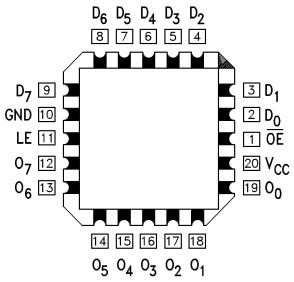
Pin Assignment for LCC



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Functional Description

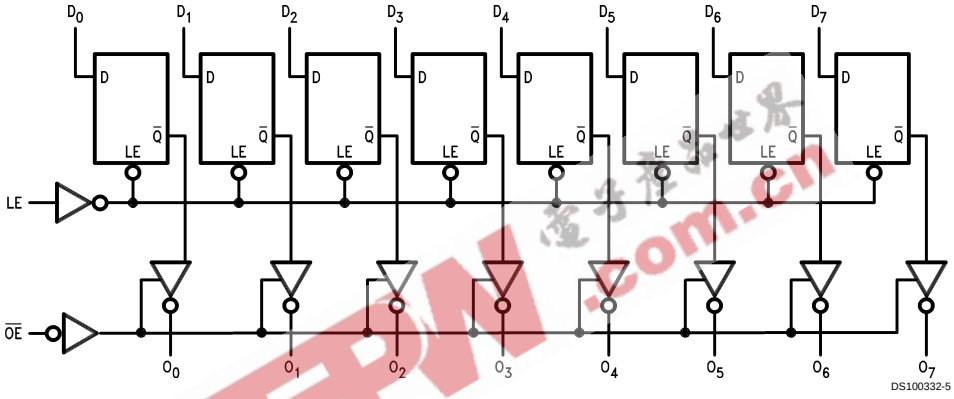
The 'ACT573 contains eight D-type latches with TRI-STATE output buffers. When the Latch Enable (LE) input is HIGH, data on the D_n inputs enters the latches. In this condition the latches are transparent, i.e., a latch output will change state each time its D input changes. When LE is LOW the latches store the information that was present on the D inputs a setup time preceding the HIGH-to-LOW transition of LE. The TRI-STATE buffers are controlled by the Output Enable ($\overline{OE}$) input. When $\overline{OE}$ is LOW, the buffers are enabled. When $\overline{OE}$ is HIGH the buffers are in the high impedance mode but this does not interfere with entering new data into the latches.

Truth Table

Inputs			Outputs
$\overline{OE}$	LE	D	O_n
L	H	H	H
L	H	L	L
L	L	X	O_0
H	X	X	Z

H = HIGH Voltage
L = LOW Voltage
Z = High Impedance
X = Immaterial
O_0 = Previous O_0 before HIGH-to-LOW transition of Latch Enable

Logic Diagram



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Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
V_I = V_{CC} + 0.5V	+20 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} + 0.5V
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} + 0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to V_{CC} + 0.5V
DC Output Source or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current per Output Pin (I_{CC} or I_{GND})	±50 mA
Storage Temperature (T_{STG})	−65˚C to +150˚C
Junction Temperature (T_J)	
CDIP	175˚C

Recommended Operating Conditions

Supply Voltage (V_{CC})	
'ACT	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
54ACT	−55˚C to +125˚C
Minimum Input Edge Rate (ΔV/Δt)	
'ACT Devices	
V_{IN} from 0.8V to 2.0V	
V_{CC} @ 4.5V, 5.5V	125 mV/ns

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT® circuits outside databook specifications.

DC Characteristics for 'ACT Family Devices

Symbol	Parameter	V_{CC} (V)	54ACT T_A = −55˚C to +125˚C Guaranteed Limits	Units	Conditions
V_{IH}	Minimum High Level Input Voltage	4.5	2.0	V	V_{OUT} = 0.1V
		5.5	2.0		or V_{CC} − 0.1V
V_{IL}	Maximum Low Level Input Voltage	4.5	0.8	V	V_{OUT} = 0.1V
		5.5	0.8	or V_{CC} − 0.1V	
V_{OH}	Minimum High Level Output Voltage	4.5	4.4	V	I_{OUT} = −50 µA
		5.5	5.4		
					(Note 2) V_{IN} = V_{IL} or V_{IH}
		4.5	3.70	V	I_{OH} −24 mA
		5.5	4.70		−24 mA
V_{OL}	Maximum Low Level Output Voltage	4.5	0.1	V	I_{OUT} = 50 µA
		5.5	0.1		
					(Note 2) V_{IN} = V_{IL} or V_{IH}
		4.5	0.50	V	I_{OL} 24 mA
		5.5	0.50		24 mA
I_{IN}	Maximum Input Leakage Current	5.5	±1.0	µA	V_I = V_{CC}, GND
I_{OZ}	Maximum TRI-STATE Leakage Current	5.5	±5.0	µA	V_I = V_{IL}, V_{IH} V_O = V_{CC}, GND
I_{CCT}	Maximum I_{CC}/Input	5.5	1.6	mA	V_I = V_{CC} − 2.1V
I_{OLD}	(Note 3) Minimum Dynamic Output Current	5.5	50	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5	−50	mA	V_{OHD} = 3.85V Min

DC Characteristics for 'ACT Family Devices (Continued)

Symbol	Parameter	V_{CC} (V)	54ACT T_A = −55°C to +125°C Guaranteed Limits	Units	Conditions
I_{CC}	Maximum Quiescent Supply Current	5.5	80.0	µA	V_{IN} = V_{CC} or GND

Note 2: All outputs loaded; thresholds on input associated with output under test.

Note 3: Maximum test duration 2.0 ms, one output loaded at a time.

Note 4: I_{CC} for 54ACT @ 25°C is identical to 74ACT @ 25°C.

AC Electrical Characteristics

Symbol	Parameter	V_{CC} (V) (Note 5)	54ACT T_A = −55°C to +125°C C_L = 50 pF Min	54ACT T_A = −55°C to +125°C C_L = 50 pF Max	Units	Fig. No.
t_{PLH}	Propagation Delay D_m to O_n	5.0	1.5	13.5	ns	
t_{PHL}	Propagation Delay D_n to O_n	5.0	1.5	13.5	ns	
t_{PLH}	Propagation Delay LE to O_n	5.0	1.5	13.0	ns	
t_{PHL}	Propagation Delay LE to O_n	5.0	1.5	12.0	ns	
t_{PZH}	Output Enable Time	5.0	1.5	11.5	ns	
t_{PZL}	Output Enable Time	5.0	1.5	11.0	ns	
t_{PHZ}	Output Disable Time	5.0	1.5	13.5	ns	
t_{PLZ}	Output Disable Time	5.0	1.5	10.5	ns	

Note 5: Voltage Range 5.0 is 5.0V ±0.5V

AC Operating Requirements

Symbol	Parameter	V_{CC} (V) (Note 6)	54ACT T_A = −55°C to +125°C C_L = 50 pF Guaranteed Minimum	Units	Fig. No.
t_s	Setup Time, HIGH or LOW D_n to LE	5.0	4.5	ns	
t_h	Hold Time, HIGH or LOW D_n to LE	5.0	1.0	ns	
t_w	LE Pulse Width, HIGH	5.0	5.0	ns	

Note 6: Voltage Range 5.0 is 5.0V ±0.5V

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Capacitance	5.0	pF	V_{CC} = OPEN
C_{PD}	Power Dissipation Capacitance	25.0	pF	V_{CC} = 5.0V


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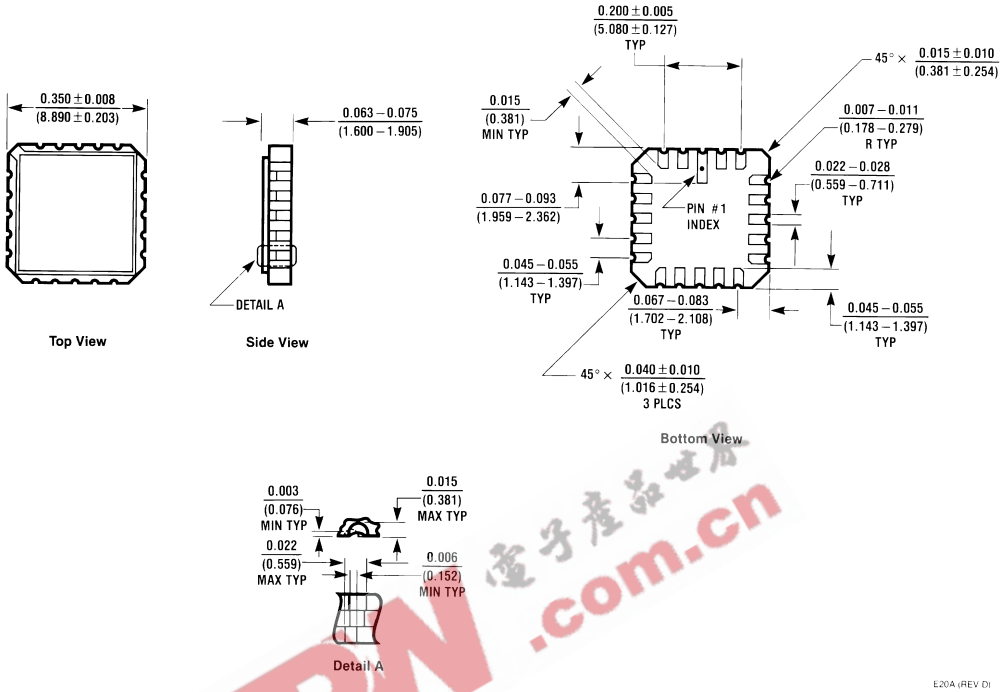
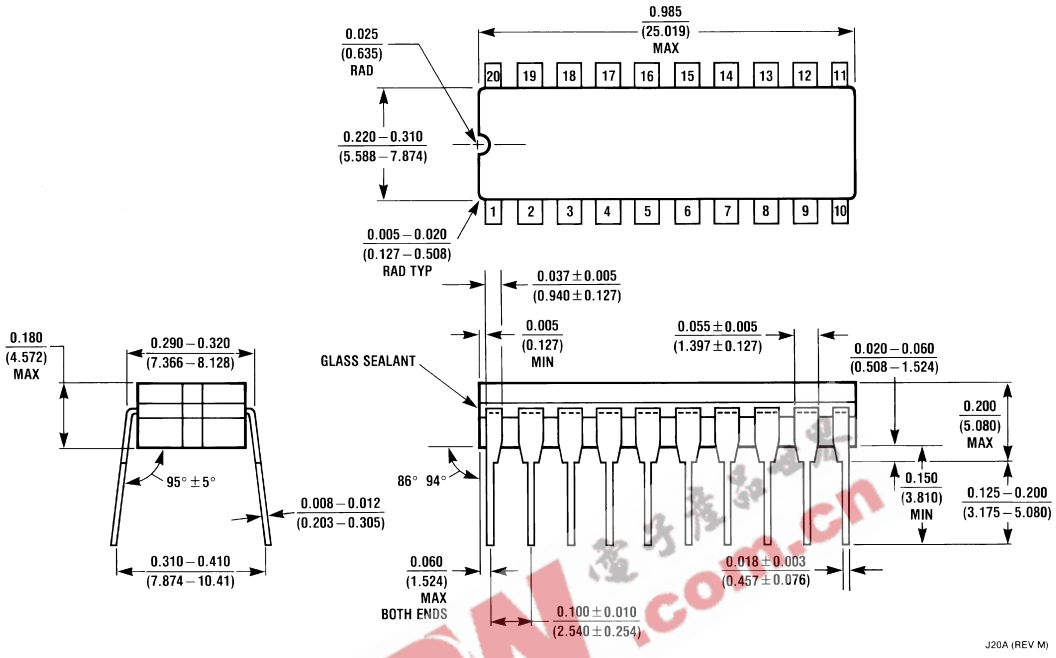
Physical Dimensions inches (millimeters) unless otherwise noted

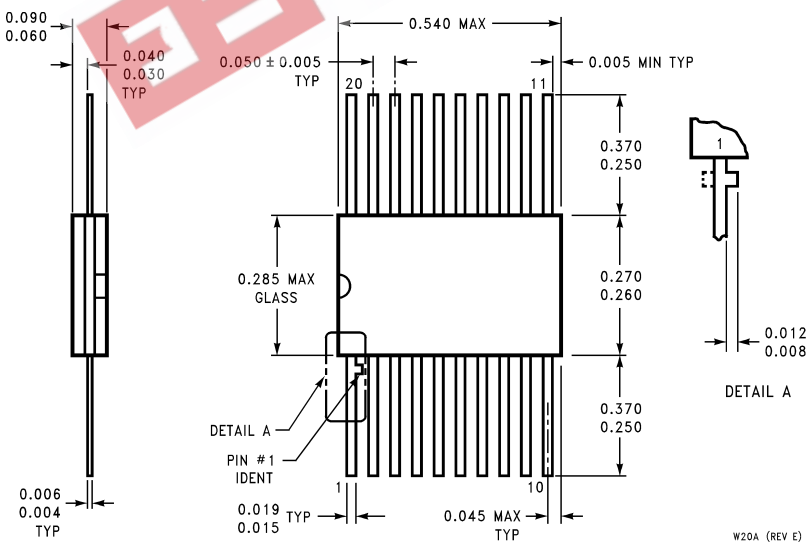


20 Terminal Ceramic Leadless Chip Carrier (L)
NS Package Number E20A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



20-Lead Ceramic Dual-In-Line Package (D)
NS Package Number J20A



20-Lead Ceramic Flatpak (F)
NS Package Number W20A

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