National Semiconductor

August 1995

54F/74F573
Octal D-Type Latch with TRI-STATE® Outputs

General Description

The ’F573 is a high speed octal latch with buffered common Latch Enable (LE) and buffered common Output Enable ($\overline{\text{OE}}$) inputs.

This device is functionally identical to the ’F373 but has different pinouts.

Features

- Inputs and outputs on opposite sides of package allowing easy interface with microprocessors
- Useful as input or output port for microprocessors
- Functionally identical to ’F373
- TRI-STATE outputs for bus interfacing
- Guaranteed 4000V minimum ESD protection

Commercial	Military	Package Number	Package Description
74F573PC		N20A	20-Lead (0.300″ Wide) Molded Dual-In-Line
	54F573DM (Note 2)	J20A	20-Lead Ceramic Dual-In-Line
74F573SC (Note 1)		M20B	20-Lead (0.300″ Wide) Molded Small Outline, JEDEC
74F573SJ (Note 1)		M20D	20-Lead (0.300″ Wide) Molded Small Outline, EIAJ
	54F573FM (Note 2)	W20A	20-Lead Cerpak
	54F573LM (Note 2)	E20A	20-Lead Ceramic Leadless Chip Carrier, Type C

Note 1: Devices also available in 13″ reel. Use suffix = SCX and SJX.

Note 2: Military grade device with environmental and burn-in processing. Use suffix = DMQB, FMQB and LMQB.

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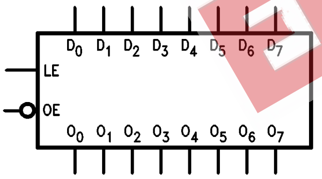
Logic Symbols



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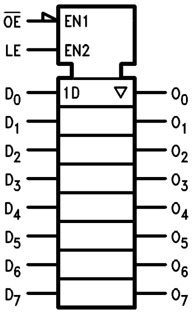
IEEE/IEC



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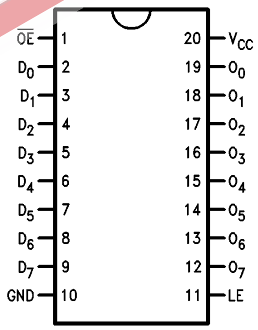
Connection Diagrams

Pin Assignment for DIP, SOIC and Flatpak



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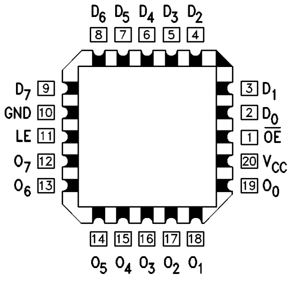
Pin Assignment for LCC



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Unit Loading/Fan Out

Pin Names	Description	54F/74F	
		U.L. HIGH/LOW	Input I_{IH}/I_{IL} Output I_{OH}/I_{OL}
D_0–D_7	Data Inputs	1.0/1.0	20 μA/−0.6 mA
LE	Latch Enable Input (Active HIGH)	1.0/1.0	20 μA/−0.6 mA
$\overline{OE}$	TRI-STATE Output Enable Input (Active LOW)	1.0/1.0	20 μA/−0.6 mA
O_0–O_7	TRI-STATE Latch Outputs	150/40(33.3)	−3 mA/24 mA (20 mA)

Functional Description

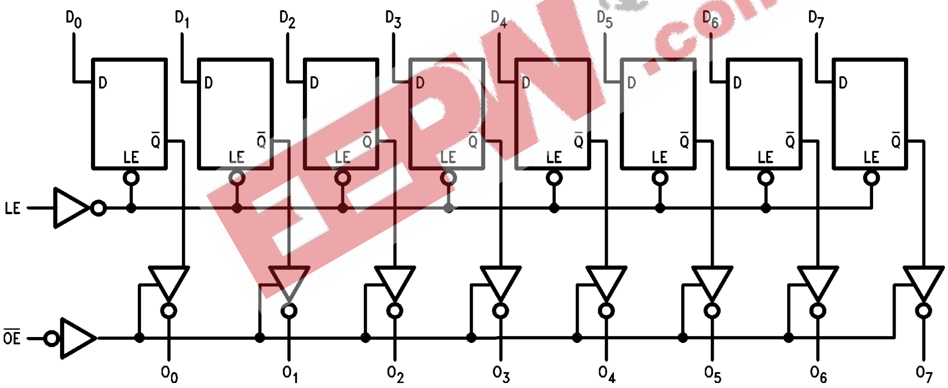
The ’F573 contains eight D-type latches with 3-state output buffers. When the Latch Enable (LE) input is HIGH, data on the D_n inputs enters the latches. In this condition the latches are transparent, i.e., a latch output will change state each time its D input changes. When LE is LOW the latches store the information that was present on the D inputs a setup time preceding the HIGH-to-LOW transition of LE. The 3-state buffers are controlled by the Output Enable ($\overline{OE}$) input. When $\overline{OE}$ is LOW, the buffers are in the bi-state mode. When $\overline{OE}$ is HIGH the buffers are in the high impedance mode but this does not interfer with entering new data into the latches.

Function Table

Inputs			Outputs
$\overline{OE}$	LE	D	O
L	H	H	H
L	H	L	L
L	L	X	O_0
H	X	X	Z

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
O_0 = Value stored from previous clock cycle

Logic Diagram



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Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	−55°C to +175°C
Plastic	−55°C to +150°C
V_{CC} Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V_{CC} = 0V)	
Standard Output	−0.5V to V_{CC}
TRI-STATE Output	−0.5V to +5.5V
Current Applied to Output in LOW State (Max)	twice the rated I_{OL} (mA)
ESD Last Passing Voltage (Min)	4000V

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

Recommended Operating Conditions

Free Air Ambient Temperature	
Military	−55°C to +125°C
Commercial	0°C to +70°C
Supply Voltage	
Military	+4.5V to +5.5V
Commercial	+4.5V to +5.5V

DC Electrical Characteristics

Symbol	Parameter		54F/74F			Units	V_{CC}	Conditions
			Min	Typ	Max			
V_{IH}	Input HIGH Voltage		2.0			V		Recognized as a HIGH Signal
V_{IL}	Input LOW Voltage				0.8	V		Recognized as a LOW Signal
V_{CD}	Input Clamp Diode Voltage				−1.2	V	Min	I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	54F 10% V_{CC}	2.5			V	Min	I_{OH} = −1 mA
		54F 10% V_{CC}	2.4					I_{OH} = −3 mA
		74F 10% V_{CC}	2.5					I_{OH} = −1 mA
		74F 10% V_{CC}	2.4					I_{OH} = −3 mA
		74F 5% V_{CC}	2.7					I_{OH} = −1 mA
		74F 5% V_{CC}	2.7					I_{OH} = −3 mA
V_{OL}	Output LOW Voltage	54F 10% V_{CC}			0.5	V	Min	I_{OL} = 20 mA
		74F 10% V_{CC}			0.5			I_{OL} = 24 mA
I_{IH}	Input HIGH Current	54F			20.0	μA	Max	V_{IN} = 2.7V
		74F			5.0			
I_{BVI}	Input HIGH Current Breakdown Test	54F			100	μA	Max	V_{IN} = 7.0V
		74F			7.0			
I_{CEX}	Output HIGH Leakage Current	54F			250	μA	Max	V_{OUT} = V_{CC}
		74F			50			
V_{ID}	Input Leakage Test	74F	4.75			V	0.0	I_{ID} = 1.9 μA All Other Pins Grounded
I_{OD}	Output Leakage Circuit Current	74F			3.75	μA	0.0	V_{IOD} = 150 mV All Other Pins Grounded
I_{IL}	Input LOW Current				−0.6	mA	Max	V_{IN} = 0.5V
I_{OZH}	Output Leakage Current				50	μA	Max	V_{OUT} = 2.7V
I_{OZL}	Output Leakage Current				−50	μA	Max	V_{OUT} = 0.5V
I_{OS}	Output Short-Circuit Current		−60		−150	mA	Max	V_{OUT} = 0V
I_{ZZ}	Bus Drainage Test				500	μA	0.0V	V_{OUT} = 5.25V
I_{CCL}	Power Supply Current			35	55	mA	Max	V_O = LOW
I_{CCZ}	Power Supply Current			35	55	mA	Max	V_O = HIGH Z

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AC Electrical Characteristics

Symbol	Parameter	74F			54F		74F		Units
		$T_A = +25^\circ C$ $V_{CC} = +5.0V$ $C_L = 50\ pF$			$T_A, V_{CC} =$ Mil $C_L = 50\ pF$		$T_A, V_{CC} =$ Com $C_L = 50\ pF$		
		Min	Typ	Max	Min	Max	Min	Max	
t_{PLH}	Propagation Delay D_n to O_n	3.0	5.3	7.0	3.0	9.0	3.0	8.0	ns
t_{PHL}		2.0	3.7	6.0	2.0	7.0	2.0	6.5	
t_{PLH}	Propagation Delay LE to O_n	5.0	9.0	11.0	5.0	13.5	5.0	12.0	ns
t_{PHL}		3.0	5.2	7.0	3.0	7.5	3.0	7.0	
t_{PZH}	Output Enable Time	2.0	5.0	8.0	2.0	10.0	2.0	9.0	ns
t_{PZL}		2.0	5.6	8.5	2.0	10.0	2.0	9.5	
t_{PHZ}	Output Disable Time	1.5	4.5	5.5	1.5	7.0	1.5	6.5	
t_{PLZ}		1.5	3.8	5.5	1.5	5.5	1.5	5.5	

AC Operating Requirements

Symbol	Parameter	74F		54F		74F		Units
		$T_A = +25^\circ C$ $V_{CC} = +5.0V$		$T_A, V_{CC} =$ Mil		$T_A, V_{CC} =$ Com		
		Min	Max	Min	Max	Min	Max	
$t_s(H)$	Setup Time, HIGH or LOW D_n to LE	2.0		2.0		2.0		ns
$t_s(L)$		2.0		2.0		2.0		
$t_h(H)$	Hold Time, HIGH or LOW D_n to LE	3.0		3.0		3.0		
$t_h(L)$		3.5		4.0		3.5		
$t_w(H)$	LE Pulse Width, HIGH	4.0		4.0		4.0		ns

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Ordering Information

The device number is used to form part of a simplified purchasing code where the package type and temperature range are defined as follows:

74F 573 S C X

Temperature Range Family
74F = Commercial
54F = Military

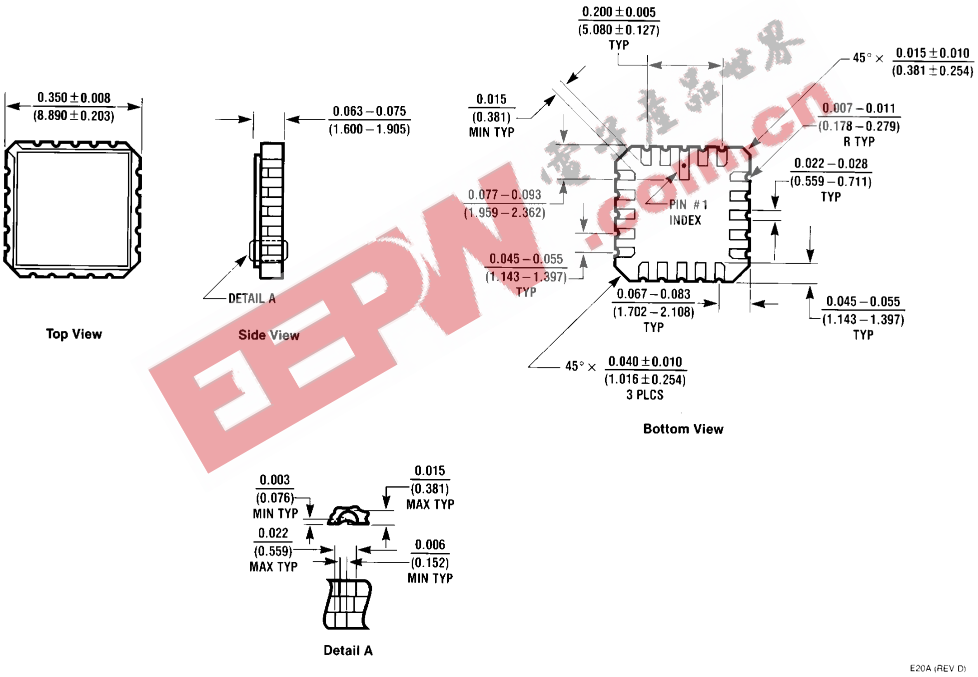
Device Type

Package Code
P = Plastic DIP
D = Ceramic DIP
F = Flatpak
L = Leadless Chip Carrier (LCC)
S = Small Outline SOIC JEDEC
SJ = Small Outline SOIC EIAJ

Special Variations
QB = Military grade device with environmental and burn-in processing
X = Devices shipped in 13″ reels

Temperature Range
C = Commercial (0°C to +70°C)
M = Military (−55°C to +125°C)

Physical Dimensions inches (millimeters)



20-Lead Ceramic Leadless Chip Carrier (L)
NS Package Number E20A

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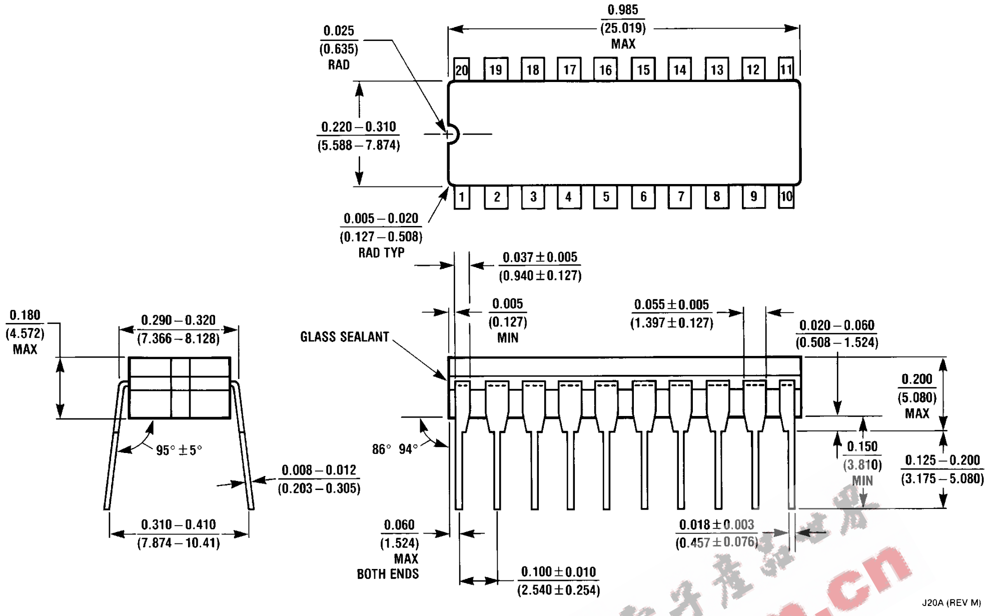
Physical Dimensions inches (millimeters) (Continued)



20-Lead Ceramic Dual-In-Line Package (D)
NS Package Number J20A

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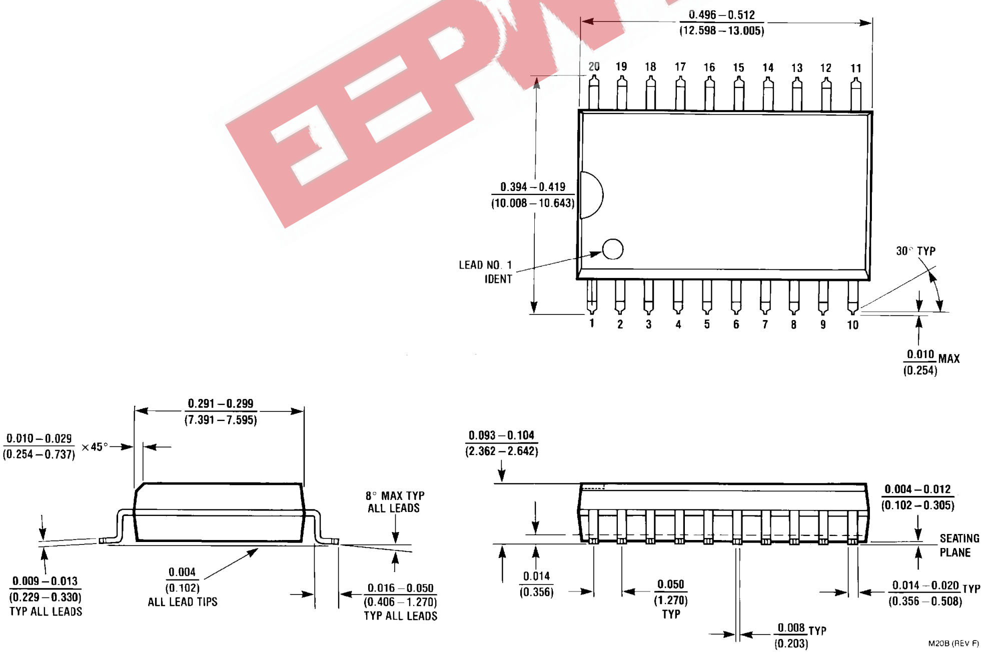
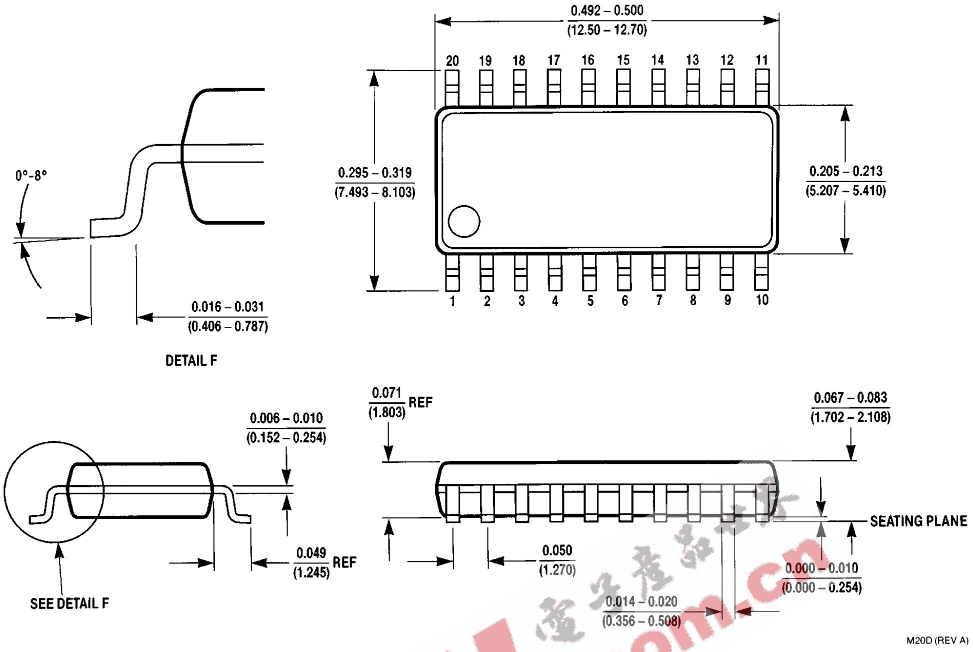
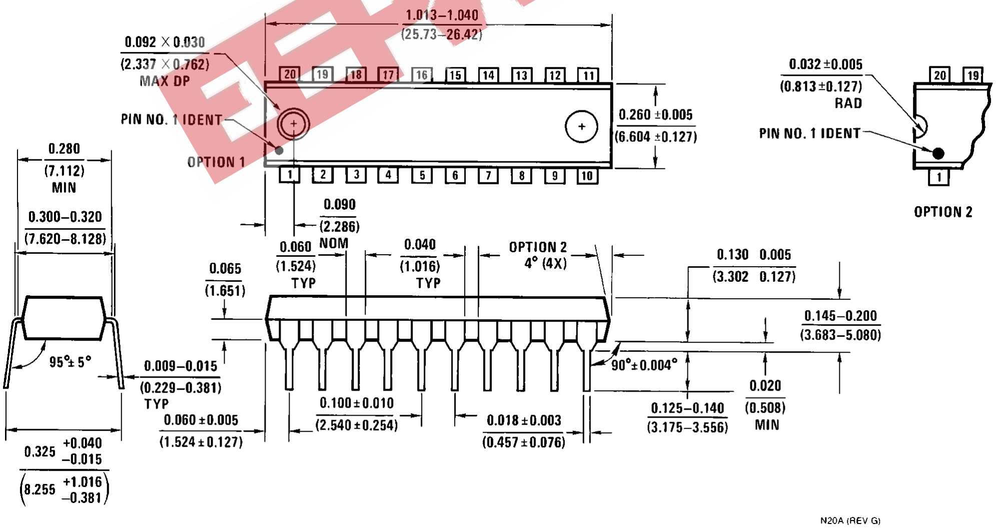


20-Lead (0.300″ Wide) Molded Small Outline Package, JEDEC (S)
NS Package Number M20B

Physical Dimensions inches (millimeters) (Continued)

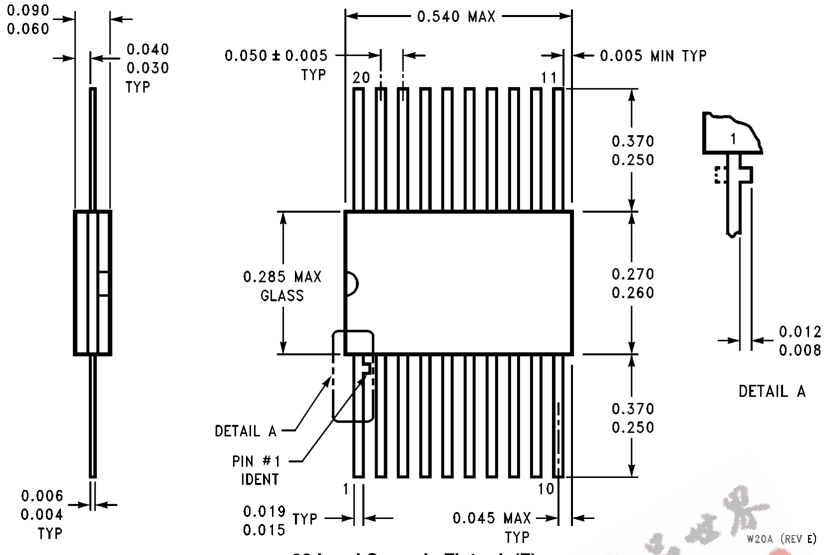


20-Lead (0.300″ Wide) Small Outline Package, EIAJ (SJ)
NS Package Number M20D



20-Lead (0.300″ Wide) Molded Dual-In-Line Package (P)
NS Package Number N20A

Physical Dimensions inches (millimeters) (Continued)



20 Lead Ceramic Flatpak (F)
NS Package Number W20A

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