July 1998

National **S**emiconductor

54ACT534
Octal D Flip-Flop with TRI-STATE® Outputs

General Description

The 'ACT534 is a high-speed, low-power octal D-type flip-flop featuring separate D-type inputs for each flip-flop and TRI-STATE outputs for bus-oriented applications. A buffered Clock (CP) and Output Enable ($\overline{OE}$) are common to all flip-flops. The 'ACT534 is the same as the 'ACT374 except that the outputs are inverted.

- Edge-triggered D-type inputs
- Buffered positive edge-triggered clock
- TRI-STATE outputs for bus-oriented applications
- Outputs source/sink 24 mA
- 'ACT534 has TTL-compatible inputs
- Inverted output version of 'ACT374
- Standard Microcircuit Drawing (SMD) 5962-8965801

Features

- I_{CC} and I_{OZ} reduced by 50%

Logic Symbols

DS100292-1

IEEE/IEC

DS100292-2
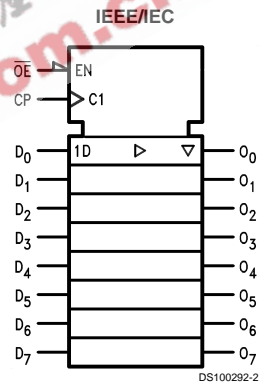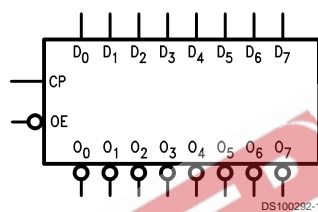
Pin Names	Description
D_0–D_7	Data Inputs
CP	Clock Pulse Input
$\overline{OE}$	TRI-STATE Output Enable Input
$\overline{O}_0$–$\overline{O}_7$	Complementary TRI-STATE Outputs

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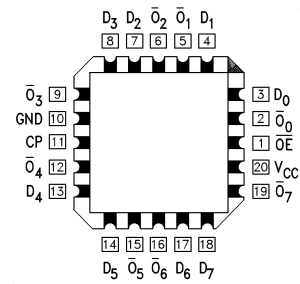FACT™ is a trademark of Fairchild Semiconductor Corporation.

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Connection Diagrams

**Pin Assignment
for DIP and Flatpak**

$\overline{OE}$	1	20	V_{CC}
$\overline{O}_0$	2	19	$\overline{O}_7$
D_0	3	18	D_7
D_1	4	17	D_6
$\overline{O}_1$	5	16	$\overline{O}_6$
$\overline{O}_2$	6	15	$\overline{O}_5$
D_2	7	14	D_5
D_3	8	13	D_4
$\overline{O}_3$	9	12	$\overline{O}_4$
GND	10	11	CP
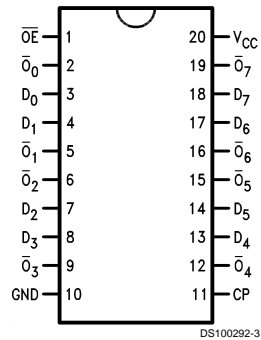
DS100292-3

**Pin Assignment
for LCC**

Top row: D_3 [8], D_2 [7], $\overline{O}_2$ [6], $\overline{O}_1$ [5], D_1 [4]

Left side: $\overline{O}_3$ [9], GND [10], CP [11], $\overline{O}_4$ [12], D_4 [13]

Right side: [3] D_0, [2] $\overline{O}_0$, [1] $\overline{OE}$, [20] V_{CC}, [19] $\overline{O}_7$

Bottom row: [14] [15] [16] [17] [18] — D_5, $\overline{O}_5$, $\overline{O}_6$, D_6, D_7
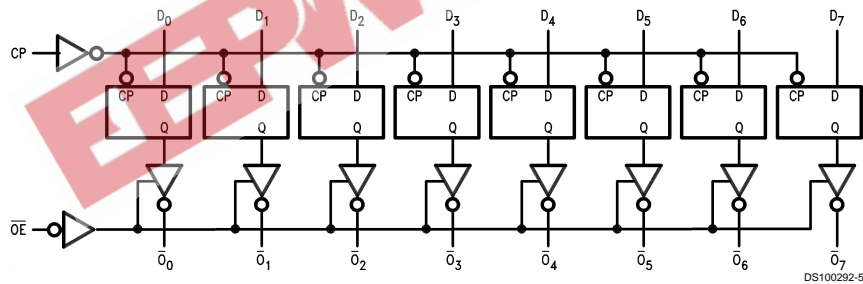
DS100292-4

Functional Description

The 'ACT534 consists of eight edge-triggered flip-flops with individual D-type inputs and TRI-STATE complementary outputs. The buffered clock and buffered Output Enable are common to all flip-flops. The eight flip-flops will store the state of their individual D inputs that meet the setup and hold times requirements on the LOW-to-HIGH Clock (CP) transition. With the Output Enable ($\overline{OE}$) LOW, the contents of the eight flip-flops are available at the outputs. When the $\overline{OE}$ is HIGH, the outputs go to the high impedance state. Operation of the $\overline{OE}$ input does not affect the state of the flip-flops.

Logic Diagram

DS100292-5

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Function Table

Inputs			Output
CP	OE	D	$\overline{O}$
⌐	L	H	L
⌐	L	L	H
L	L	X	$\overline{O}_0$
X	H	X	Z

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
⌐ = LOW-to-HIGH Clock Transition
Z = High Impedance
$\overline{O}_0$ = Value stored from previous clock cycle

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
$V_I = -0.5V$	−20 mA
$V_I = V_{CC} + 0.5V$	+20 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} + 0.5V
DC Output Diode Current (I_{OK})	
$V_O = -0.5V$	−20 mA
$V_O = V_{CC} + 0.5V$	+20 mA
DC Output Voltage (V_O)	−0.5V to V_{CC} + 0.5V
DC Output Source	
or Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current	
per Output Pin (I_{CC} or I_{GND})	±50 mA
Storage Temperature (T_{STG})	−65°C to +150°C

Junction Temperature (T_J)	
CDIP	175°C

Recommended Operating Conditions

Supply Voltage (V_{CC})	
'ACT	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	
54ACT	−55°C to +125°C
Minimum Input Edge Rate (ΔV/Δt)	
'ACT Devices	
V_{IN} from 0.8V to 2.0V	
V_{CC} @ 4.5V, 5.5V	125 mV/ns

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. National does not recommend operation of FACT™ circuits outside databook specifications.

DC Characteristics for 'ACT Family Devices

Symbol	Parameter	V_{CC} (V)	54ACT $T_A =$ −55°C to +125°C Guaranteed Limits	Units	Conditions
V_{IH}	Minimum High Level Input Voltage	4.5	2.0	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		5.5	2.0		
V_{IL}	Maximum Low Level Input Voltage	4.5	0.8	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		5.5	0.8		
V_{OH}	Minimum High Level Output Voltage	4.5	4.4	V	I_{OUT} = −50 µA
		5.5	5.4		
		4.5	3.70	V	(Note 2) $V_{IN} = V_{IL}$ or V_{IH} I_{OH} = −24 mA
		5.5	4.70		I_{OH} = −24 mA
V_{OL}	Maximum Low Level Output Voltage	4.5	0.1	V	I_{OUT} = 50 µA
		5.5	0.1		
		4.5	0.50	V	(Note 2) $V_{IN} = V_{IL}$ or V_{IH} I_{OL} = 24 mA
		5.5	0.50		I_{OL} = 24 mA
I_{IN}	Maximum Input Leakage Current	5.5	±1.0	µA	$V_I = V_{CC}$, GND
I_{OZ}	Maximum TRI-STATE Current	5.5	±5.0	µA	$V_I = V_{IL}, V_{IH}$ $V_O = V_{CC}$, GND
I_{CCT}	Maximum I_{CC}/Input	5.5	1.6	mA	$V_I = V_{CC}$ − 2.1V
I_{OLD}	Minimum Dynamic	5.5	50	mA	V_{OLD} = 1.65V Max
I_{OHD}	Output Current (Note 3)	5.5	−50	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5	80.0	µA	$V_{IN} = V_{CC}$ or GND

Note 2: All outputs loaded; thresholds on input associated with output under test.

Note 3: Maximum test duration 2.0 ms, one output loaded at a time.

Note 4: I_{CC} for 54ACT @ 25°C is identical to 74ACT @ 25°C.

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AC Electrical Characteristics

Symbol	Parameter	V_CC (V) (Note 5)	54ACT T_A = −55°C to +125°C C_L = 50 pF		Units	Fig. No.
			Min	Max		
f_{max}	Maximum Clock Frequency	5.0	85		MHz	
t_{PLH}	Propagation Delay CP to $\overline{Q}_n$	5.0	1.5	14.0	ns	
t_{PHL}	Propagation Delay CP to $\overline{Q}_n$	5.0	1.5	13.0	ns	
t_{PZH}	Output Enable Time	5.0	1.5	14.0	ns	
t_{PZL}	Output Enable Time	5.0	1.5	13.0	ns	
t_{PHZ}	Output Disable Time	5.0	1.5	14.5	ns	
t_{PLZ}	Output Disable Time	5.0	1.5	11.5	ns	

Note 5: Voltage Range 5.0 is 5.0V ±0.5V

AC Operating Requirements

Symbol	Parameter	V_CC (V) (Note 6)	54ACT T_A = −55°C to +125°C C_L = 50 pF Guaranteed Minimum	Units	Fig. No.
t_s	Setup Time, HIGH or LOW D_n to CP	5.0	5.0	ns	
t_h	Hold Time, HIGH or LOW D_n to CP	5.0	3.0	ns	
t_w	CP Pulse Width HIGH or LOW	5.0	5.0	ns	

Note 6: Voltage Range 5.0 is 5.0V ±0.5V

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = OPEN
C_{PD}	Power Dissipation Capacitance	40.0	pF	V_{CC} = 5.0V

Physical Dimensions inches (millimeters) unless otherwise noted

0.350 ± 0.008
(8.890 ± 0.203)

Top View

0.063 − 0.075
(1.600 − 1.905)

DETAIL A

Side View

0.200 ± 0.005
(5.080 ± 0.127)
TYP

0.015
(0.381)
MIN TYP

45° × 0.015 ± 0.010
(0.381 ± 0.254)

0.007 − 0.011
(0.178 − 0.279)
R TYP

0.022 − 0.028
(0.559 − 0.711)
TYP

0.077 − 0.093
(1.959 − 2.362)

PIN #1
INDEX

0.045 − 0.055
(1.143 − 1.397)
TYP

0.067 − 0.083
(1.702 − 2.108)
TYP

0.045 − 0.055
(1.143 − 1.397)
TYP

45° × 0.040 ± 0.010
(1.016 ± 0.254)
3 PLCS

Bottom View

0.003
(0.076)
MIN TYP

0.015
(0.381)
MAX TYP

0.022
(0.559)
MAX TYP

0.006
(0.152)
MIN TYP

Detail A
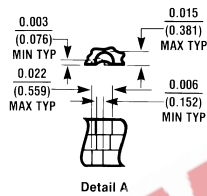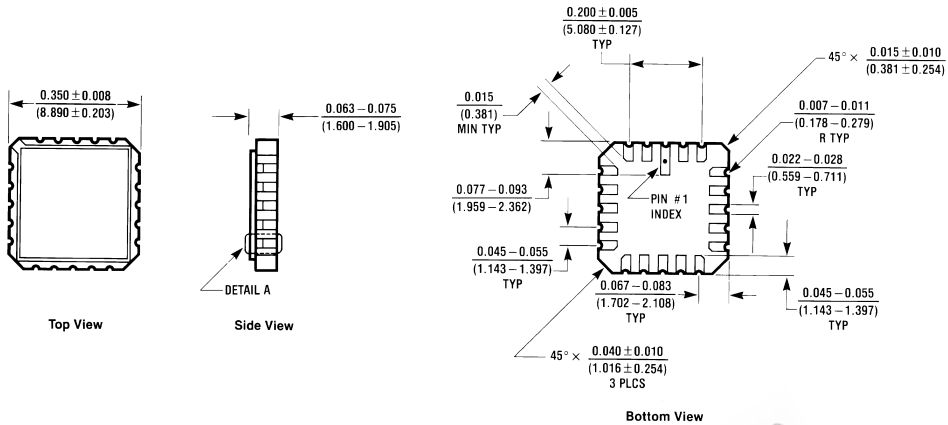
E20A (REV D)

20 Terminal Ceramic Leadless Chip Carrier (L)
NS Package Number E20A

0.785
[19.94] MAX

16   9

0.220−0.310
[5.59−7.87]

R 0.025
[0.64]

1   8

R 0.005−0.020
[0.13−0.51] TYP

0.037 ± 0.005
[0.94 ± 0.13] TYP

0.005
[0.13]
MIN TYP

0.055 ± 0.005
[1.40 ± 0.13] TYP

0.290−0.320
[7.37−8.13]

GLASS SEALANT

0.020−0.060
[0.51−1.52] TYP

0.200
[5.08]
MAX TYP

0.180
[4.57] MAX

0.010 ± 0.002
[0.25 ± 0.05] TYP

0.150
[3.81] MIN TYP

0.125−0.200
[3.18−5.08] TYP

90° ± 4°
TYP

95° ± 5°
TYP

0.080
[2.03] MAX
BOTH ENDS

0.018 ± 0.003
[0.46 ± 0.08] TYP

0.310−0.410
[7.87−10.41]

0.100 ± 0.010
[2.54 ± 0.25] TYP
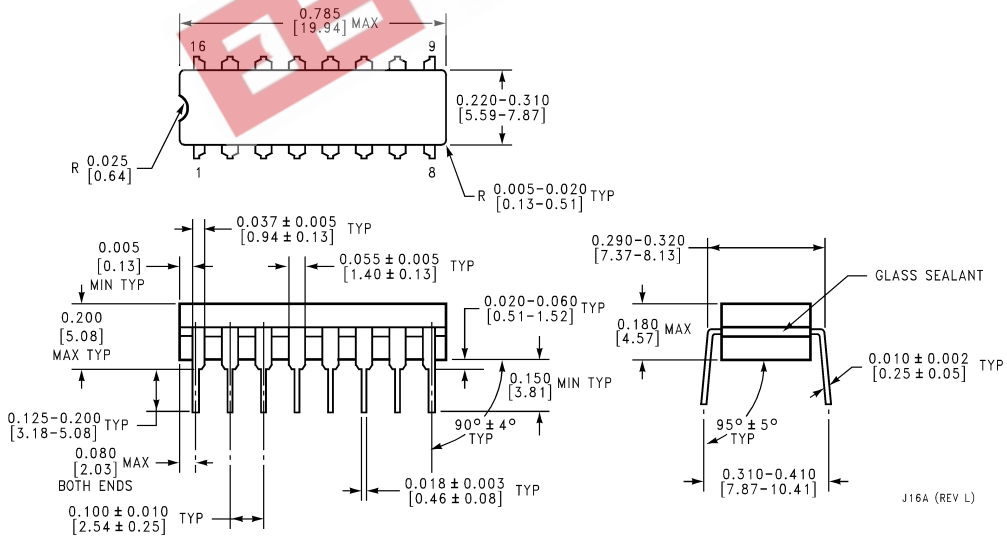
J16A (REV L)

16 Lead Ceramic Dual-In-Line Package (D)
NS Package Number J16A

54ACT534 Octal D Flip-Flop with TRI-STATE Outputs

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

$$\frac{0.050-0.080}{(1.270-2.032)}$$

$$\frac{0.004-0.006}{(0.102-0.152)}\ TYP$$

$$\frac{0.371-0.390}{(9.423-9.906)}$$

$$\frac{0.007-0.018}{(0.178-0.457)}\ TYP$$

$$\frac{0.050\pm0.005}{(1.270\pm0.127)}\ TYP$$

0.000 MIN TYP

$$\frac{0.250-0.370}{(6.350-9.398)}$$

$$\frac{0.300}{(7.620)}\ MAX\ GLASS$$

16 15 14 13 12 11 10 9

$$\frac{0.245-0.275}{(6.223-6.985)}$$

2 3 4 5 6 7 8

DETAIL A

PIN NO. 1 IDENT

$$\frac{0.250-0.370}{(6.350-9.398)}$$

$$\frac{0.026-0.040}{(0.660-1.016)}\ TYP$$

$$\frac{0.015-0.019}{(0.381-0.482)}\ TYP$$

$$\frac{0.008-0.012}{(0.203-0.305)}$$

DETAIL A

W16A (REV H)
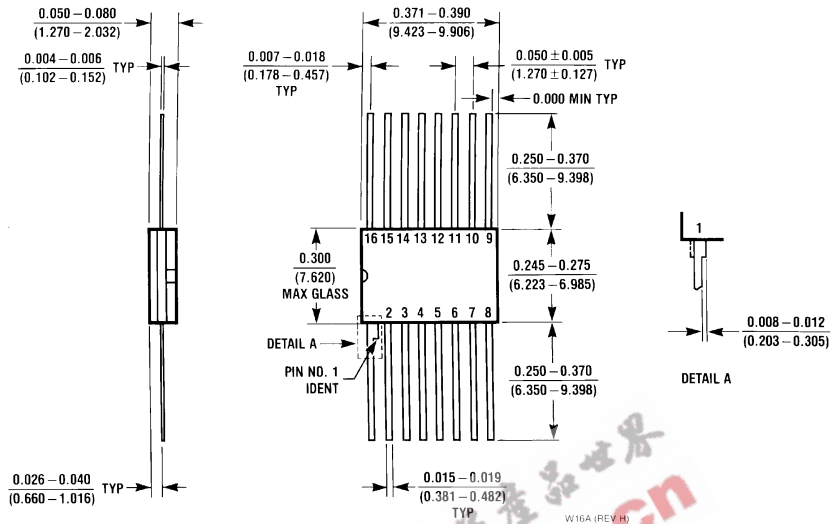
16 Lead Ceramic Flatpak (F)
NS Package Number W16A

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