

54F/74F821 10-Bit D-Type Flip-Flop

General Description

The 'F821 is a 10-bit D-type flip-flop with TRI-STATE® true outputs arranged in a broadside pinout. The 'F821 is functionally and pin compatible with the AMD's Am29821.

Features

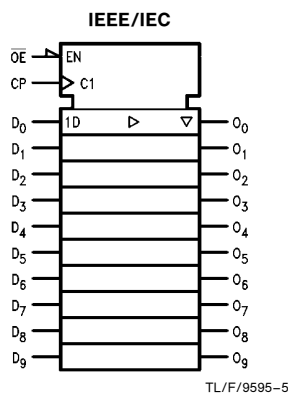
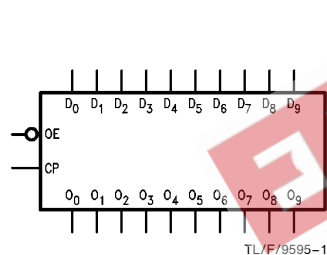
- TRI-STATE Outputs
- Direct replacement for AMD's Am29821

Commercial	Military	Package Number	Package Description
74F821SPC		N24C	24-Lead (0.300" Wide) Molded Dual-In-Line
	54F821SDM (Note 2)	J24F	24-Lead (0.300" Wide) Ceramic Dual-In-Line
74F821SC (Note 1)		M24B	24-Lead (0.300" Wide) Molded Small Outline, JEDEC
	54F821FM (Note 2)	W24C	24-Lead Cerpack
	54F821LM (Note 2)	E28A	24-Lead Ceramic Leadless Chip Carrier, Type C

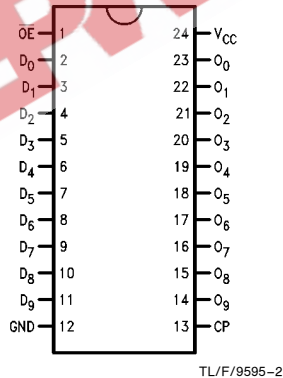
Note 1: Devices also available in 13" reel. Use suffix = SCX.

Note 2: Military grade device with environmental and burn-in processing. Use suffix = SDMQB, FMQB and LMQB.

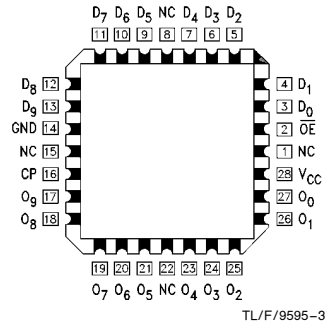
Logic Symbols



Pin Assignment
for DIP, SOIC and Flatpak



Pin Assignment
for LCC



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Unit Loading/Fan Out

Pin Names	Description	54F/74F	
		U.L. HIGH/LOW	Input I _{IH} /I _{IL} Output I _{OH} /I _{OL}
D ₀ –D ₉	Data Inputs	1.0/1.0	20 μA/ –0.6 mA
OE	Output Enable	1.0/1.0	20 μA/ –0.6 mA
CP	TRI-STATE Input	1.0/1.0	20 μA/ –0.6 mA
O ₀ –O ₉	Clock Input	150/40 (33.3)	–3.0 mA/24 mA (20 mA)

Functional Description

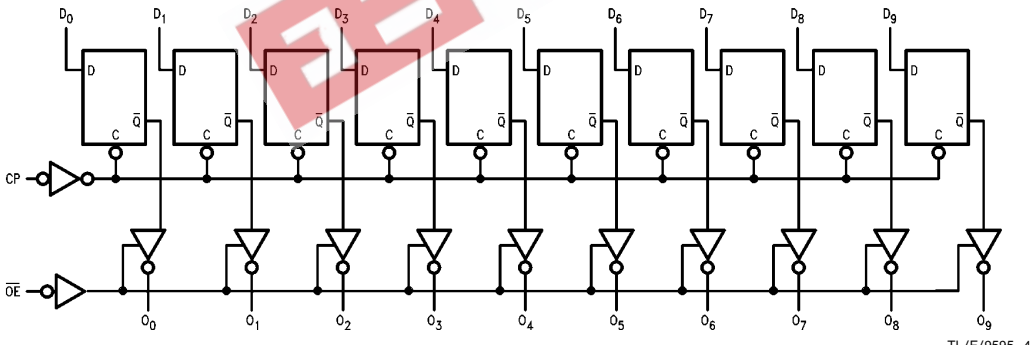
The 'F821 consists of ten D-type edge-triggered flip-flops. This device has TRI-STATE true outputs for bus systems organized in a broadside pinning. The buffered Clock (CP) and buffered Output Enable (OE) are common to all flip-flops. The flip-flops will store the state of their individual D inputs that meet the setup and hold times requirements on the LOW-to-HIGH CP transition. With the OE LOW the content of the flip-flops are available at the outputs. When the OE is HIGH, the outputs go to the high impedance state. Operation of the OE input does not affect the state of the flip-flops.

Function Table

Inputs			Internal	Output	Function
OE	CP	D	Q	O	
H	H	X	NC	Z	Hold
H	L	X	NC	Z	Hold
H		L	H	Z	Load
H		H	L	Z	Load
L		L	H	L	Data Available
L		H	L	H	Data Available
L	H	X	NC	NC	No Change in Data
L	L	X	NC	NC	No Change in Data

L = LOW Voltage Level
H = HIGH Voltage Level
X = Immaterial
Z = High Impedance
 = LOW-to-HIGH Transition
NC = No Change

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	−55°C to +175°C
Plastic	−55°C to +150°C
V _{CC} Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V _{CC} = 0V)	
Standard Output	−0.5V to V _{CC}
TRI-STATE Output	−0.5V to +5.5V
Current Applied to Output in LOW State (Max)	twice the rated I _{OL} (mA)

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

Recommended Operating Conditions

Free Air Ambient Temperature	
Military	−55°C to +125°C
Commercial	0°C to +70°C
Supply Voltage	
Military	+4.5V to +5.5V
Commercial	+4.5V to +5.5V

DC Electrical Characteristics

Symbol	Parameter	54F/74F			Units	V _{CC}	Conditions
		Min	Typ	Max			
V _{IH}	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V _{IL}	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V _{CD}	Input Clamp Diode Voltage			−1.2	V	Min	I _{IN} = −18 mA
V _{OH}	Output HIGH Voltage	54F 10% V _{CC} 54F 10% V _{CC} 74F 10% V _{CC} 74F 10% V _{CC} 74F 5% V _{CC} 74F 5% V _{CC}	2.5 2.4 2.5 2.4 2.7 2.7		V	Min	I _{OH} = −1 mA I _{OH} = −3 mA I _{OH} = −1 mA I _{OH} = −3 mA I _{OH} = −1 mA I _{OH} = −3 mA
V _{OL}	Output LOW Voltage	54F 10% V _{CC} 74F 10% V _{CC}		0.5 0.5	V	Min	I _{OL} = 20 mA I _{OL} = 24 mA
I _{IH}	Input HIGH Current	54F 74F		20.0 5.0	μA	Max	V _{IN} = 2.7V
I _{BVI}	Input HIGH Current Breakdown Test	54F 74F		100 7.0	μA	Max	V _{IN} = 7.0V
I _{CEX}	Output HIGH Leakage Current	54F 74F		250 50	μA	Max	V _{OUT} = V _{CC}
V _{ID}	Input Leakage Test	74F	4.75		V	0.0	I _{ID} = 1.9 μA, All Other Pins Grounded
I _{OD}	Output Leakage Circuit Current	74F		3.75	μA	0.0	V _{IOD} = 150 mV All Other Pins Grounded
I _{IL}	Input LOW Current			−0.6	mA	Max	V _{IN} = 0.5V
I _{OZH}	Output Leakage Current			50	μA	Max	V _{OUT} = 2.7V
I _{OZL}	Output Leakage Current			−50	μA	Max	V _{OUT} = 0.5V
I _{OS}	Output Short-Circuit Current		−60	−150	mA	Max	V _{OUT} = 0V
I _{CCZ}	Power Supply Current		78	100	mA	Max	V _O = HIGH Z

AC Electrical Characteristics

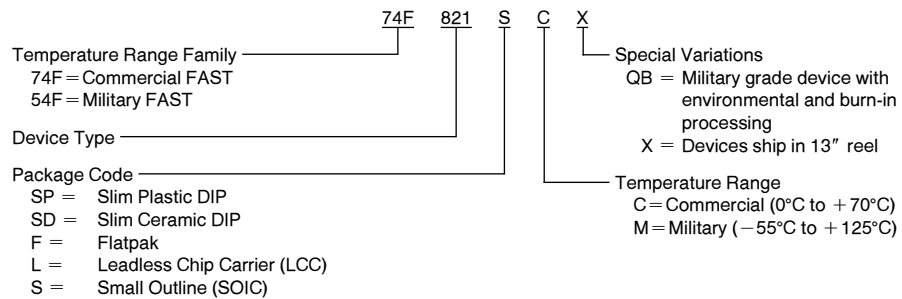
Symbol	Parameter	74F			54F		74F		Units
		$T_A = +25^{\circ}\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{ pF}$			$T_A, V_{CC} = \text{Mil}$ $C_L = 50\text{ pF}$		$T_A, V_{CC} = \text{Com}$ $C_L = 50\text{ pF}$		
		Min	Typ	Max	Min	Max	Min	Max	
f _{max}	Maximum Clock Frequency	100	150		60		70		MHz
t _{PLH}	Propagation Delay	2.0	6.4	9.5	2.0	10.5	2.0	10.5	ns
t _{PHL}	CP to O _n	2.0	6.2	9.5	2.0	10.5	2.0	10.5	
t _{PZH}	Output Enable Time	2.0	5.8	10.5	2.0	13.0	2.0	11.5	ns
t _{PZL}	$\overline{OE}$ to O _n	2.0	6.3	10.5	2.0	13.0	2.0	11.5	
t _{PHZ}	Output Disable Time	1.5	3.4	7.0	1.0	7.5	1.5	7.5	
t _{PLZ}	$\overline{OE}$ to O _n	1.5	3.5	7.0	1.0	7.5	1.5	7.5	

AC Operating Requirements

Symbol	Parameter	74F		54F		74F		Units
		$T_A = +25^{\circ}\text{C}$ $V_{CC} = +5.0\text{V}$		$T_A, V_{CC} = \text{Mil}$		$T_A, V_{CC} = \text{Com}$		
		Min	Max	Min	Max	Min	Max	
$t_s(\text{H})$	Setup Time, HIGH or LOW	2.5		4.0		3.0		ns
$t_s(\text{L})$	D_n to CP	2.5		4.0		3.0		
$t_h(\text{H})$	Hold Time, HIGH or LOW	2.5		2.5		2.5		ns
$t_h(\text{L})$	D_n to CP	2.5		2.5		2.5		
$t_w(\text{H})$	CP Pulse Width	5.0		6.0		6.0		ns
$t_w(\text{L})$	HIGH or LOW	5.0		6.0		6.0		

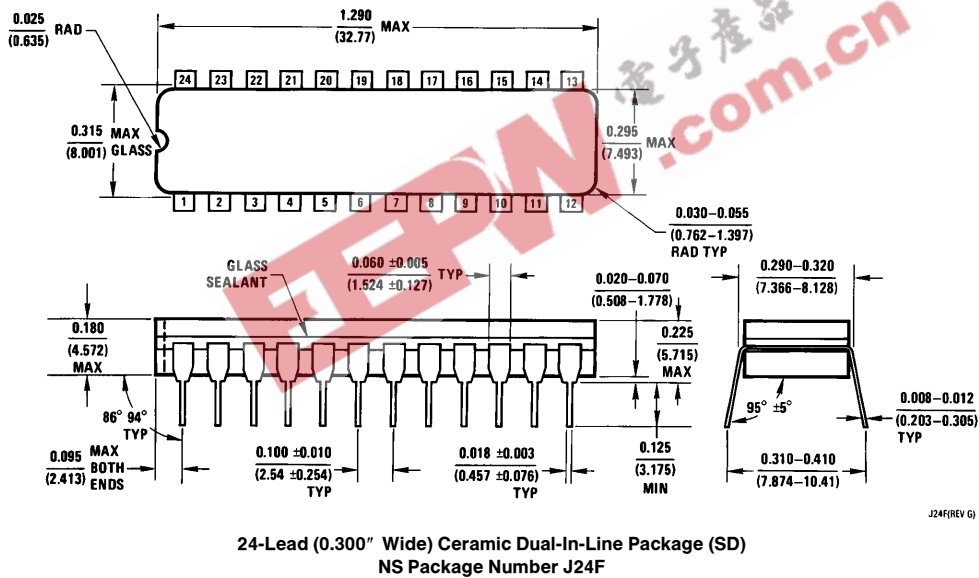
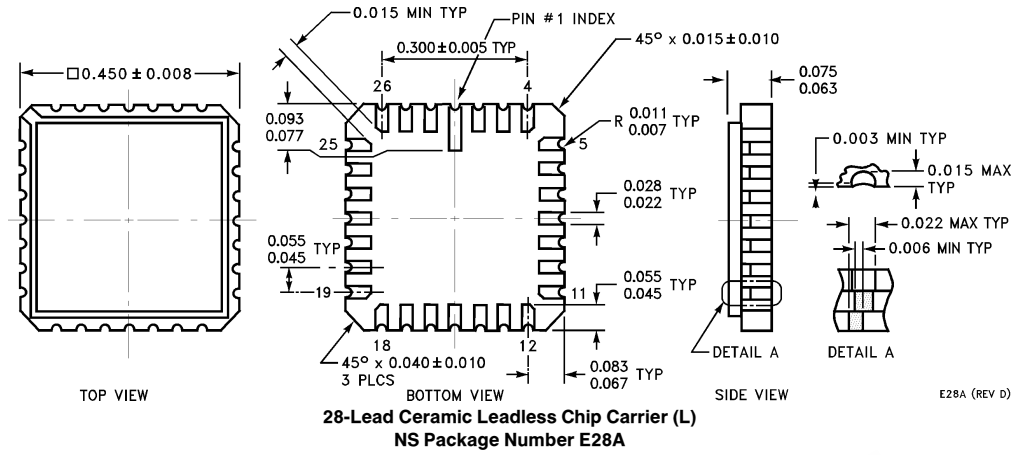
Ordering Information

The device number is used to form part of a simplified purchasing code where the package type and temperature range are defined as follows:

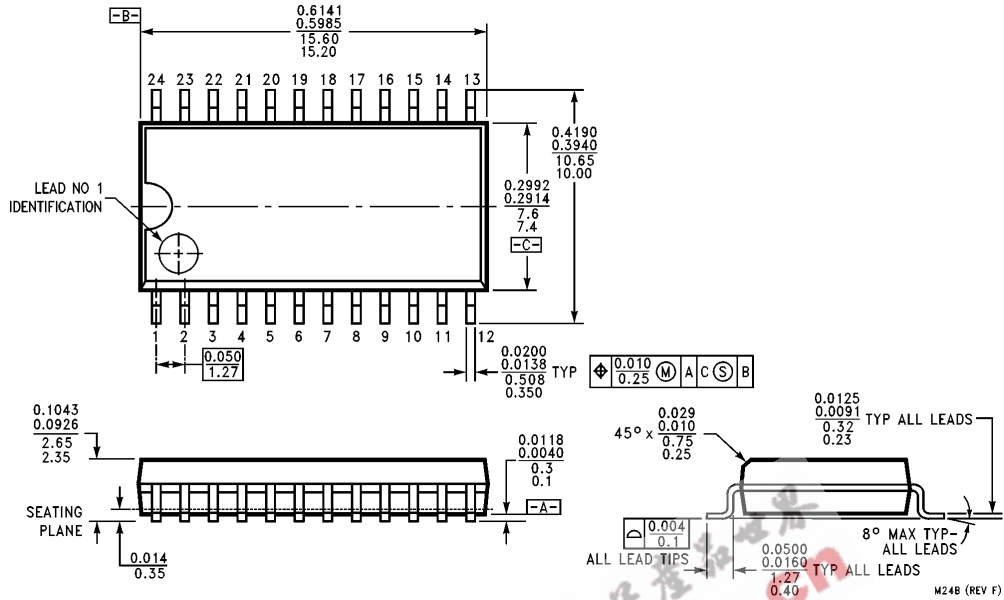


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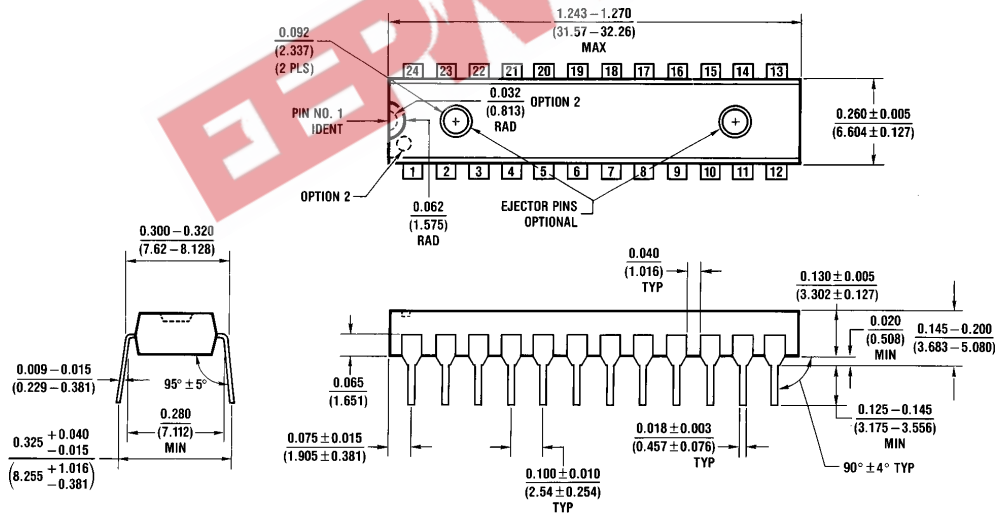
Physical Dimensions inches (millimeters)



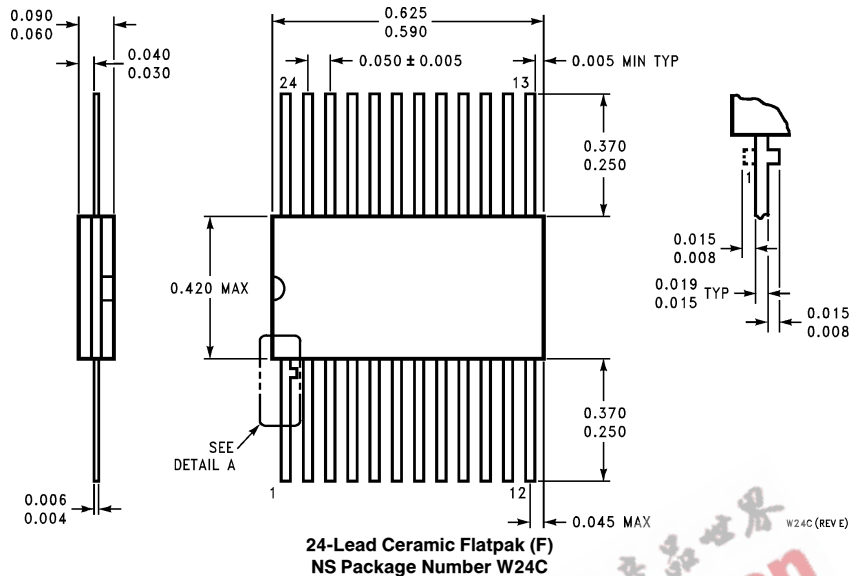
Physical Dimensions inches (millimeters) (Continued)



**24-Lead (0.300" Wide) Molded Small Outline Package, JEDEC (S)
NS Package Number M24B**



24-Lead (0.300" Wide) Molded Dual-In-Line Package (SP)
NS Package Number N24C

Physical Dimensions inches (millimeters) (Continued)**LIFE SUPPORT POLICY**

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National Semiconductor Corporation
2900 Semiconductor Drive
P.O. Box 58090
Santa Clara, CA 95052-8090
Tel: (800) 272-9959
TWX: (910) 339-9240

National Semiconductor GmbH
Livry-Gargan-Str. 10
D-82256 Fürstentfeldbruck
Germany
Tel: (81-41) 35-0
Telex: 527649
Fax: (81-41) 35-1

National Semiconductor Japan Ltd.
Sumitomo Chemical
Engineering Center
Bldg. 7F
1-7-1, Nakase, Mihama-Ku
Chiba-City,
Chiba Prefecture 261
Tel: (043) 299-2300
Fax: (043) 299-2500

National Semiconductor Hong Kong Ltd.
13th Floor, Straight Block,
Ocean Centre, 5 Canton Rd.
Tsimshatsui, Kowloon
Hong Kong
Tel: (852) 2737-1600
Fax: (852) 2736-9960

National Semicondutores Do Brazil Ltda.
Rue Deputado Lacorda Franco
120-3A
Sao Paulo-SP
Brazil 05418-000
Tel: (55-11) 212-5066
Telex: 391-1131931 NSBR BR
Fax: (55-11) 212-1181

National Semiconductor (Australia) Pty, Ltd.
Building 16
Business Park Drive
Monash Business Park
Nottingham, Melbourne
Victoria 3168 Australia
Tel: (3) 558-9888
Fax: (3) 558-9898

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