DATA SHEET

74LVC2G14
Dual inverting Schmitt-trigger with 5 V tolerant input

Product specification
Supersedes data of 2003 Jul 31

2004 Sep 08

Philips Semiconductors

PHILIPS

Dual inverting Schmitt-trigger with 5 V tolerant input

74LVC2G14

FEATURES

- Wide supply voltage range from 1.65 V to 5.5 V
- 5 V tolerant input/output for interfacing with 5 V logic
- High noise immunity
- Complies with JEDEC standard:
  - JESD8-7 (1.65 V to 1.95 V)
  - JESD8-5 (2.3 V to 2.7 V)
  - JESD8B/JESD36 (2.7 V to 3.6 V).
- ±24 mA output drive (V_{CC} = 3.0 V)
- CMOS low power consumption
- Latch-up performance exceeds 250 mA
- Direct interface with TTL levels
- Mulltiple package options
- ESD protection:
  - HBM EIA/JESD22-A114-B exceeds 2000 V
  - MM EIA/JESD22-A115-A exceeds 200 V.
- Specified from –40 °C to +85 °C and –40 °C to +125 °C.

APPLICATIONS

- Wave and pulse shapers for highly noisy environments
- Astable multivibrators
- Monostable multivibrators.

DESCRIPTION

The 74LVC2G14 is a high-performance, low-power, low-voltage, Si-gate CMOS device and superior to most advanced CMOS compatible TTL families.

Inputs can be driven from either 3.3 V or 5 V devices. This feature allows the use of this device as translator in a mixed 3.3 V and 5 V environment.

This device is fully specified for partial power-down applications using I_{off}. The I_{off} circuitry disables the output, preventing the damaging backflow current through the device when it is powered down.

The 74LVC2G14A provides two inverting buffers with Schmitt-trigger action. It is capable of transforming slowly changing input signals into sharply defined, jitter-free output signals.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	propagation delay input nA to output nY	V_{CC} = 1.8 V; C_L = 30 pF; R_L = 1 kΩ	5.6	ns
		V_{CC} = 2.5 V; C_L = 30 pF; R_L = 500 Ω	3.7	ns
		V_{CC} = 2.7 V; C_L = 50 pF; R_L = 500 Ω	4.1	ns
		V_{CC} = 3.3 V; C_L = 50 pF; R_L = 500 Ω	3.9	ns
		V_{CC} = 5.0 V; C_L = 50 pF; R_L = 500 Ω	2.7	ns
C_I	input capacitance		3.5	pF
C_{PD}	power dissipation capacitance per buffer	V_{CC} = 3.3 V; notes 1 and 2	18.1	pF

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW).
   $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum(C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz;
   f_o = output frequency in MHz;
   C_L = output load capacitance in pF;
   V_{CC} = supply voltage in Volts;
   N = total switching outputs;
   $\sum(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.
2. The condition is V_I = GND to V_{CC}.

FUNCTION TABLE

See note 1.

INPUT	OUTPUT
nA	**nY**
L	H
H	L

Note

1. H = HIGH voltage level;
   L = LOW voltage level.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE					
	TEMPERATURE RANGE	PINS	PACKAGE	MATERIAL	CODE	MARKING
74LVC2G14GW	–40 °C to +125 °C	6	SC-88	plastic	SOT363	VK
74LVC2G14GV	–40 °C to +125 °C	6	SC-74	plastic	SOT457	V14
74LVC2G14GM	–40 °C to +125 °C	6	XSON6	plastic	SOT886	VK

PINNING

PIN	SYMBOL	DESCRIPTION
1	1A	data input
2	GND	ground (0 V)
3	2A	data input
4	2Y	data output
5	V_{CC}	supply voltage
6	1Y	data output

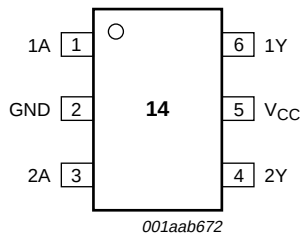
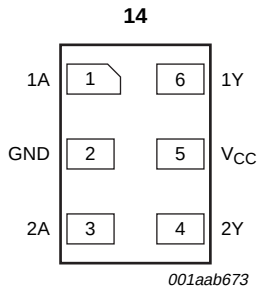


Fig.1 Pin configuration SC-88 and SC-74.



Transparent top view

Fig.2 Pin configuration XSON6.

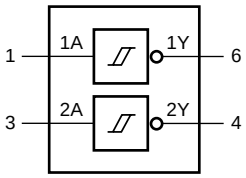


Fig.3 Logic symbol.

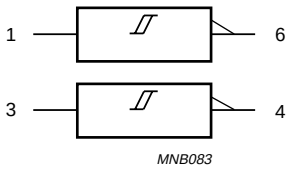


Fig.4 IEEE/IEC logic symbol.

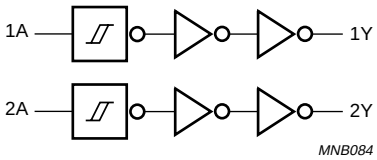


Fig.5 Logic diagram.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	supply voltage		1.65	5.5	V
V_I	input voltage		0	5.5	V
V_O	output voltage		0	V_{CC}	V
T_{amb}	operating ambient temperature		–40	+125	°C

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134); voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CC}	supply voltage		–0.5	+6.5	V
I_{IK}	input diode current	$V_I < 0$ V	–	–50	mA
V_I	input voltage	note 1	–0.5	+6.5	V
I_{OK}	output diode current	$V_O > V_{CC}$ or $V_O < 0$ V	–	±50	mA
V_O	output voltage	enable mode; notes 1 and 2	–0.5	V_{CC} + 0.5	V
		Power-down mode; notes 1 and 2	–0.5	+6.5	V
I_O	output source or sink current	V_O = 0 V to V_{CC}	–	±50	mA
I_{CC}, I_{GND}	V_{CC} or GND current		–	±100	mA
T_{stg}	storage temperature		–65	+150	°C
P_D	power dissipation	T_{amb} = –40 °C to +125 °C	–	300	mW

Notes

1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. When V_{CC} = 0 V (Power-down mode), the output voltage can be 5.5 V in normal operation.

DC CHARACTERISTICS

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		OTHER	V_{CC} (V)				
T_{amb} = –40 °C to +85 °C; note 1							
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}					
		I_O = 100 µA	1.65 to 5.5	–	–	0.1	V
		I_O = 4 mA	1.65	–	–	0.45	V
		I_O = 8 mA	2.3	–	–	0.3	V
		I_O = 12 mA	2.7	–	–	0.4	V
		I_O = 24 mA	3.0	–	–	0.55	V
		I_O = 32 mA	4.5	–	–	0.55	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}					
		I_O = –100 µA	1.65 to 5.5	V_{CC} – 0.1	–	–	V
		I_O = –4 mA	1.65	1.2	–	–	V
		I_O = –8 mA	2.3	1.9	–	–	V
		I_O = –12 mA	2.7	2.2	–	–	V
		I_O = –24 mA	3.0	2.3	–	–	V
		I_O = –32 mA	4.5	3.8	–	–	V
I_{LI}	input leakage current	V_I = 5.5 V or GND	5.5	–	±0.1	±5	µA
I_{off}	power OFF leakage current	V_I or V_O = 5.5 V	0	–	±0.1	±10	µA
I_{CC}	quiescent supply current	$V_I = V_{CC}$ or GND; I_O = 0 A	5.5	–	0.1	10	µA
ΔI_{CC}	additional quiescent supply current per pin	$V_I = V_{CC}$ – 0.6 V; I_O = 0 A	2.3 to 5.5	–	5	500	µA

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		OTHER	V_{CC} (V)				
T_{amb} = −40 °C to +125 °C							
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}					
		I_O = 100 µA	1.65 to 5.5	–	–	0.1	V
		I_O = 4 mA	1.65	–	–	0.70	V
		I_O = 8 mA	2.3	–	–	0.45	V
		I_O = 12 mA	2.7	–	–	0.60	V
		I_O = 24 mA	3.0	–	–	0.80	V
		I_O = 32 mA	4.5	–	–	0.80	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}					
		I_O = −100 µA	1.65 to 5.5	V_{CC} − 0.1	–	–	V
		I_O = −4 mA	1.65	0.95	–	–	V
		I_O = −8 mA	2.3	1.7	–	–	V
		I_O = −12 mA	2.7	1.9	–	–	V
		I_O = −24 mA	3.0	2.0	–	–	V
		I_O = −32 mA	4.5	3.4	–	–	V
I_{LI}	input leakage current	V_I = 5.5 V or GND	5.5	–	–	±20	µA
I_{off}	power OFF leakage current	V_I or V_O = 5.5 V	0	–	–	±20	µA
I_{CC}	quiescent supply current	$V_I = V_{CC}$ or GND; I_O = 0 A	5.5	–	–	40	µA
ΔI_{CC}	additional quiescent supply current per pin	$V_I = V_{CC}$ − 0.6 V; I_O = 0 A	2.3 to 5.5	–	–	5000	µA

Note

1. All typical values are measured at V_{CC} = 3.3 V and T_{amb} = 25 °C.

TRANSFER CHARACTERISTICS

Voltage are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		WAVEFORMS	V_{CC} (V)				
T_{amb} = −40 °C to +85 °C; note 1							
V_{T+}	positive-going threshold	see Figs 6 and 7	1.8	0.70	1.10	1.50	V
			2.3	1.00	1.40	1.80	V
			3.0	1.30	1.76	2.20	V
			4.5	1.90	2.47	3.10	V
			5.5	2.20	2.91	3.60	V
V_{T-}	negative-going threshold	see Figs 6 and 7	1.8	0.25	0.61	0.90	V
			2.3	0.40	0.80	1.15	V
			3.0	0.60	1.04	1.50	V
			4.5	1.00	1.55	2.00	V
			5.5	1.20	1.86	2.30	V
V_H	hysteresis ($V_{T+} - V_{T-}$)	see Figs 6, 7 and 8	1.8	0.15	0.49	1.00	V
			2.3	0.25	0.60	1.10	V
			3.0	0.40	0.73	1.20	V
			4.5	0.60	0.92	1.50	V
			5.5	0.70	1.02	1.70	V
T_{amb} = −40 °C to +125 °C							
V_{T+}	positive-going threshold	see Figs 6 and 7	1.8	0.70	–	1.70	V
			2.3	1.00	–	2.00	V
			3.0	1.30	–	2.40	V
			4.5	1.90	–	3.30	V
			5.5	2.20	–	3.80	V
V_{T-}	negative-going threshold	see Figs 6 and 7	1.8	0.25	–	1.10	V
			2.3	0.40	–	1.35	V
			3.0	0.60	–	1.70	V
			4.5	1.00	–	2.20	V
			5.5	1.20	–	2.50	V
V_H	hysteresis ($V_{T+} - V_{T-}$)	see Figs 6, 7 and 8	1.8	0.15	–	1.20	V
			2.3	0.25	–	1.30	V
			3.0	0.40	–	1.40	V
			4.5	0.60	–	1.70	V
			5.5	0.70	–	1.90	V

Note

1. All typical values are measured at T_{amb} = 25 °C.

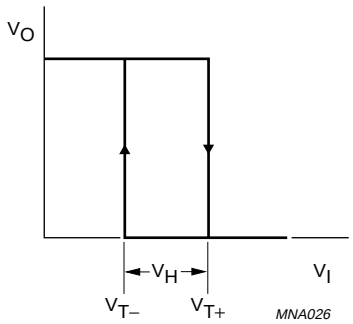
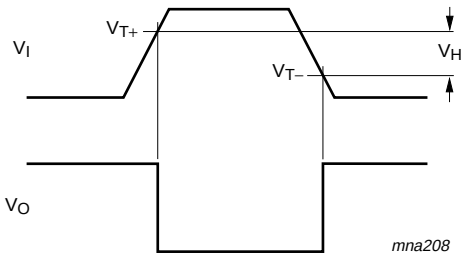
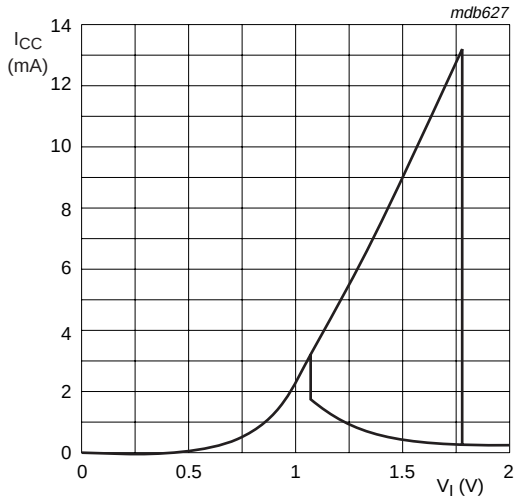


Fig.6 Transfer characteristic.



V_{T+} and V_{T-} are limits of 20 % and 70 %.

Fig.7 Definition of V_{T+}, V_{T-} and V_H.



V_{CC} = 3.0 V.

Fig.8 Typical transfer characteristic.

AC CHARACTERISTICS

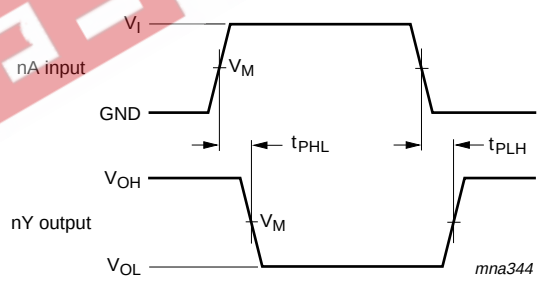
GND = 0 V.

SYMBOL	PARAMETER	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
		WAVEFORMS	V_{CC} (V)				
T_{amb} = −40 °C to +85 °C; note 1							
t_{PHL}/t_{PLH}	propagation delay input nA to output nY	see Figs 9 and 10	1.65 to 1.95	1.0	5.6	11.0	ns
			2.3 to 2.7	0.5	3.7	6.5	ns
			2.7	0.5	4.1	7.0	ns
			3.0 to 3.6	0.5	3.9	6.0	ns
			4.5 to 5.5	0.5	2.7	4.3	ns
T_{amb} = −40 °C to +125 °C							
t_{PHL}/t_{PLH}	propagation delay input nA to output nY	see Figs 9 and 10	1.65 to 1.95	1.0	–	12.0	ns
			2.3 to 2.7	0.5	–	7.2	ns
			2.7	0.5	–	7.7	ns
			3.0 to 3.6	0.5	–	6.7	ns
			4.5 to 5.5	0.5	–	4.7	ns

Note

1. All typical values are measured at T_{amb} = 25 °C.

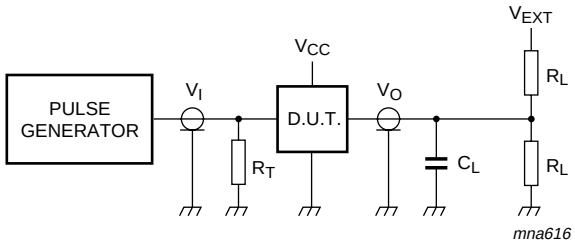
AC WAVEFORMS



V_{CC}	V_M	INPUT	
		V_I	$t_r = t_f$
1.65 V to 1.95 V	0.5 × V_{CC}	V_{CC}	≤ 2.0 ns
2.3 V to 2.7 V	0.5 × V_{CC}	V_{CC}	≤ 2.0 ns
2.7 V	1.5 V	2.7 V	≤ 2.5 ns
3.0 V to 3.6 V	1.5 V	2.7 V	≤ 2.5 ns
4.5 V to 5.5 V	0.5 × V_{CC}	V_{CC}	≤ 2.5 ns

V_{OL} and V_{OH} are typical output voltage drop that occur with the output load.

Fig.9 The input (nA) to output (nY) propagation delays.



V_{CC}	V_I	C_L	R_L	V_{EXT}
				t_{PLH}/t_{PHL}
1.65 V to 1.95 V	V_{CC}	30 pF	1 kΩ	open
2.3 V to 2.7 V	V_{CC}	30 pF	500 Ω	open
2.7 V	2.7 V	50 pF	500 Ω	open
3.0 V to 3.6 V	2.7 V	50 pF	500 Ω	open
4.5 V to 5.5 V	V_{CC}	50 pF	500 Ω	open

Definitions for test circuit:

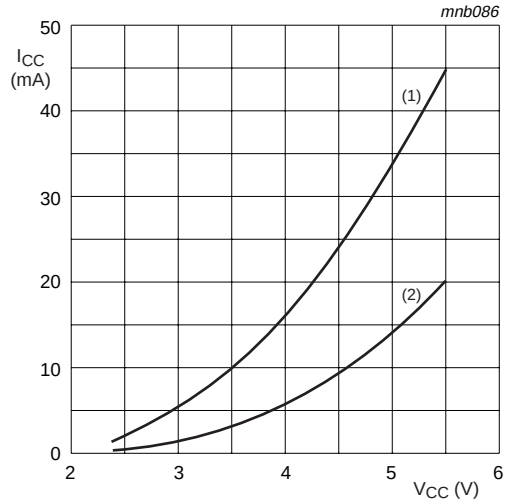
R_L = Load resistor.

C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance should be equal to the output impedance Z_o of the pulse generator.

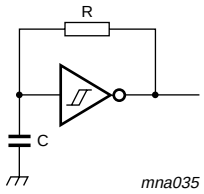
Fig.10 Load circuitry for switching times.

APPLICATION INFORMATION



All values given are typical unless otherwise specified.
Linear change of V_I between 0.8 V to 2.0 V.
(1) Positive-going edge.
(2) Negative-going edge.

Fig.11 Average I_{CC} as a function of V_{CC}.

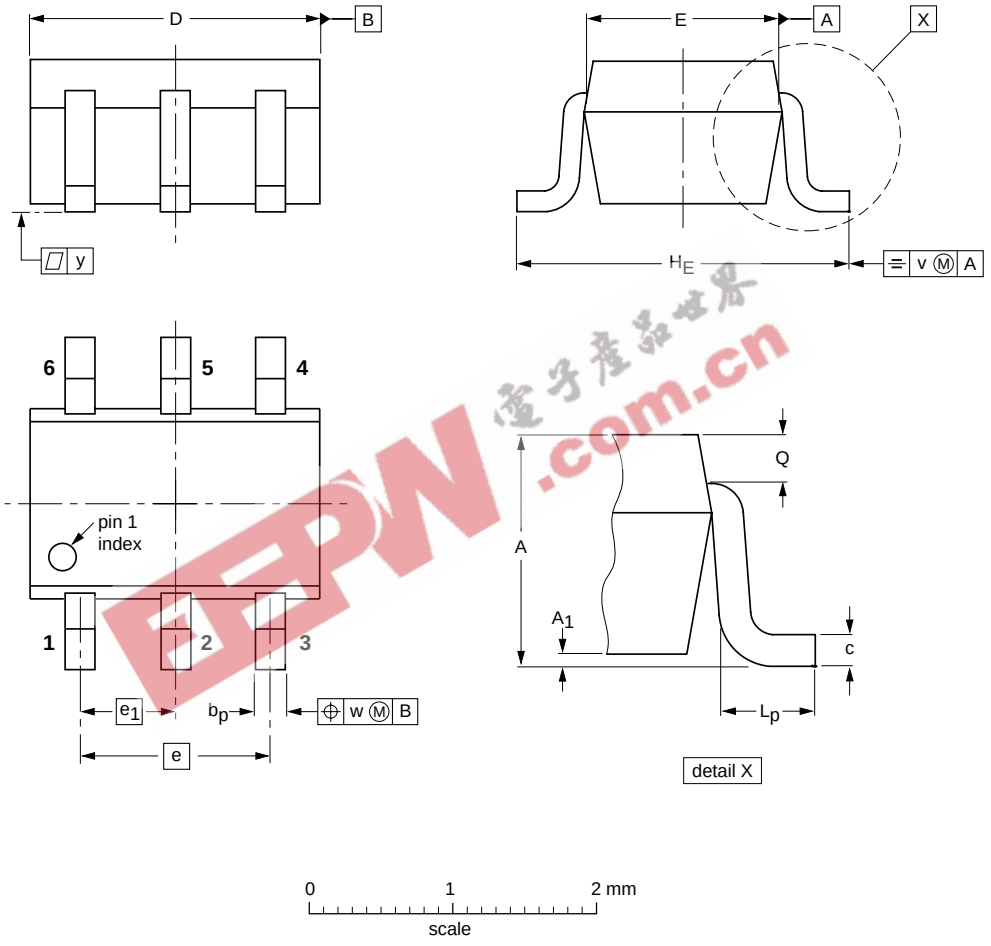


$$f = \frac{1}{T} \approx \frac{1}{0.8 \times RC}$$

Fig.12 Relaxation oscillator.

PACKAGE OUTLINES

Plastic surface mounted package; 6 leads **SOT363**

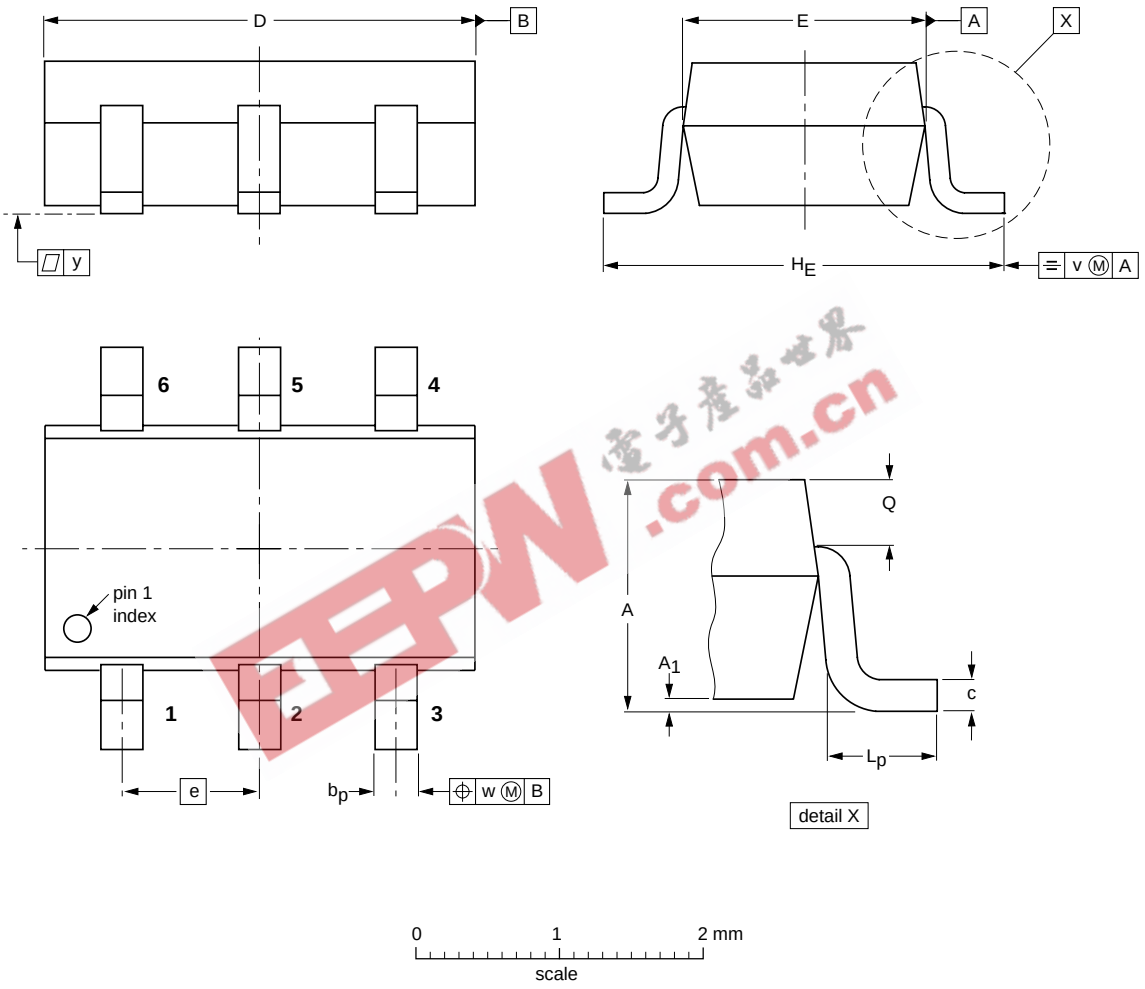


DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1 max	b_p	c	D	E	e	e_1	H_E	L_p	Q	v	w	y
mm	1.1 0.8	0.1	0.30 0.20	0.25 0.10	2.2 1.8	1.35 1.15	1.3	0.65	2.2 2.0	0.45 0.15	0.25 0.15	0.2	0.2	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT363			SC-88			97-02-28

Plastic surface mounted package; 6 leads **SOT457**

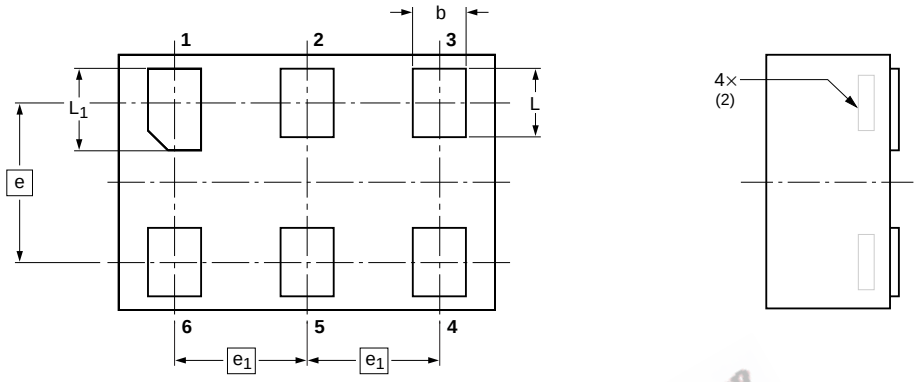


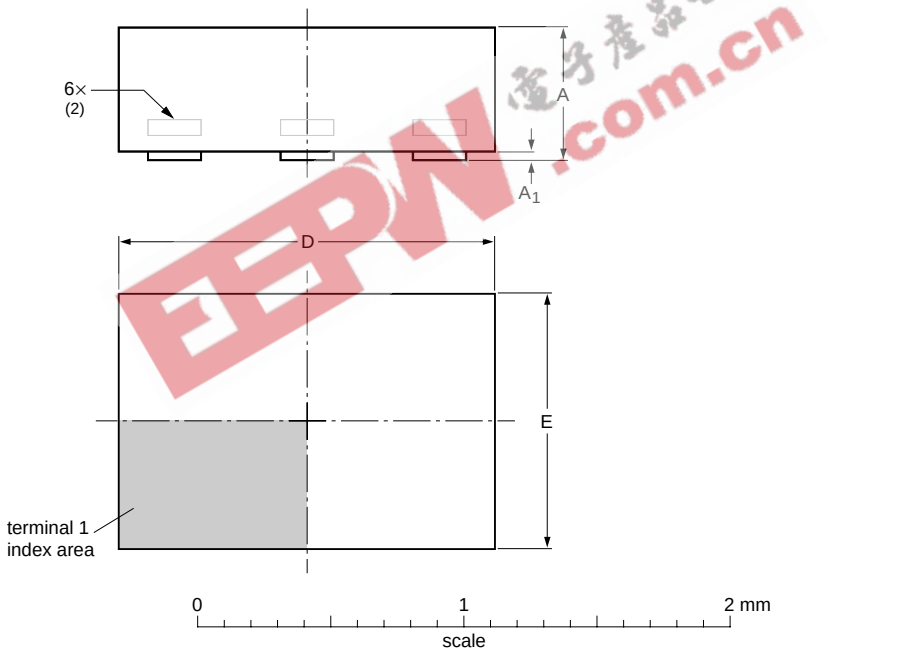
DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1	b_p	c	D	E	e	H_E	L_p	Q	v	w	y
mm	1.1 0.9	0.1 0.013	0.40 0.25	0.26 0.10	3.1 2.7	1.7 1.3	0.95	3.0 2.5	0.6 0.2	0.33 0.23	0.2	0.2	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT457			SC-74			~~97-02-28~~ 01-05-04

XSON6: plastic extremely thin small outline package; no leads; 6 terminals; body 1 x 1.45 x 0.5 mm **SOT886**





DIMENSIONS (mm are the original dimensions)

UNIT	A(1) max	A_1 max	b	D	E	e	e_1	L	L_1
mm	0.5	0.04	0.25 0.17	1.5 1.4	1.05 0.95	0.6	0.5	0.35 0.27	0.40 0.32

Notes
1. Including plating thickness.
2. Can be visible in some manufacturing processes.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT886		MO-252				~~04-07-15~~ 04-07-22

DATA SHEET STATUS

LEVEL	DATA SHEET STATUS(1)	PRODUCT STATUS(2)(3)	DEFINITION
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
III	Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN).

Notes

1. Please consult the most recently issued data sheet before initiating or completing a design.
2. The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.
3. For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

DEFINITIONS

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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