

$V_{DSM} = 2800 \text{ V}$
 $I_{TAVM} = 3740 \text{ A}$
 $I_{TRMS} = 5880 \text{ A}$
 $I_{TSM} = 60000 \text{ A}$
 $V_{T0} = 0.95 \text{ V}$
 $r_T = 0.100 \text{ m}\Omega$

Phase Control Thyristor

5STP 33L2800

Doc. No. 5SYA1011-03 Sep. 01

- Patented free-floating silicon technology
- Low on-state and switching losses
- Designed for traction, energy and industrial applications
- Optimum power handling capability
- Interdigitated amplifying gate

Blocking

Part Number	5STP 33L2800	5STP 33L2600	5STP 33L2200	Conditions	
V _{DRM} V _{RRM}	2800 V	2600 V	2200 V	f = 50 Hz, t _p = 10ms	
V _{RSM1}	3000 V	2800 V	2400 V	t _p = 5ms, single pulse	
I _{DRM}	≤ 400 mA			V _{DRM}	T _j = 125°C
I _{RRM}	≤ 400 mA			V _{RRM}	
dV/dt _{crit}	1000 V/μs			Exp. to 0.67 x V _{DRM} , T _j = 125°C	

Mechanical data

F_M	Mounting force	nom.	70 kN
		min.	63 kN
		max.	84 kN
a	Acceleration		
	Device unclamped		50 m/s ²
	Device clamped		100 m/s ²
m	Weight		1.45 kg
D_S	Surface creepage distance		36 mm
D_a	Air strike distance		15 mm

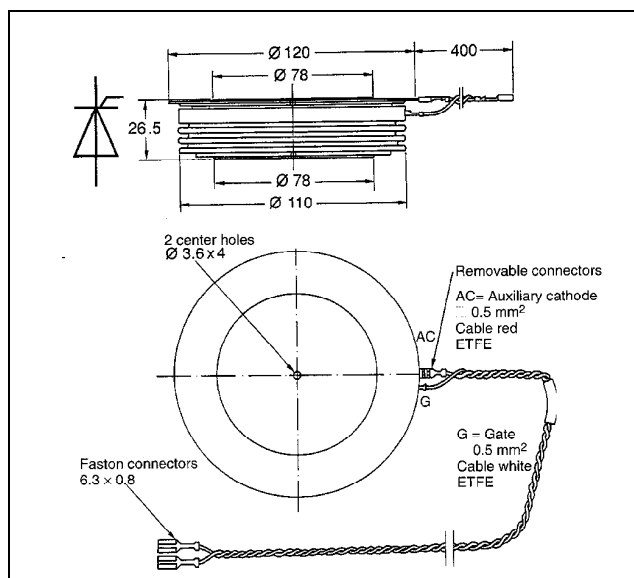


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On-state

I _{TAVM}	Max. average on-state current	3740 A	Half sine wave, T _C = 70°C	
I _{TRMS}	Max. RMS on-state current	5880 A		
I _{TSM}	Max. peak non-repetitive	60000 A	tp = 10 ms	T _j = 125°C
	surge current	65000 A	tp = 8.3 ms	After surge:
I ² t	Limiting load integral	18000 kA ² s	tp = 10 ms	V _D = V _R = 0V
		17500 kA ² s	tp = 8.3 ms	
V _T	On-state voltage	1.23 V	I _T = 3000 A	T _j = 125°C
V _{T0}	Threshold voltage	0.95 V	I _T = 2000 - 6000 A	
r _T	Slope resistance	0.100 mΩ		
I _H	Holding current	30-100 mA	T _j = 25°C	
		15-60 mA	T _j = 125°C	
I _L	Latching current	100- mA	T _j = 25°C	
		100- mA	T _j = 125°C	

Switching

di/dt_{crit}	Critical rate of rise of on-state current	250 A/ μs	Cont. $f = 50\text{ Hz}$	$V_D \leq 0.67 \cdot V_{DRM}$, $T_j = 125^\circ\text{C}$ $I_{TRM} = 4500\text{ A}$ $I_{FG} = 2\text{ A}$, $t_r = 0.5\text{ }\mu\text{s}$
		500 A/ μs	60 sec. $f = 50\text{ Hz}$	
t_d	Delay time	$\leq 3.0\text{ }\mu\text{s}$	$V_D = 0.4 \cdot V_{DRM}$	$I_{FG} = 2\text{ A}$, $t_r = 0.5\text{ }\mu\text{s}$
t_q	Turn-off time	$\leq 400\text{ }\mu\text{s}$	$V_D \leq 0.67 \cdot V_{DRM}$ $dv_D/dt = 20\text{ V}/\mu\text{s}$	$I_{TRM} = 4500\text{ A}$, $T_j = 125^\circ\text{C}$ $V_R > 200\text{ V}$, $di_T/dt = -5\text{ A}/\mu\text{s}$
Q_{rr}	Recovery charge	min	2000 μAs	
		max	4000 μAs	

Triggering

V_{GT}	Gate trigger voltage	2.6 V	$T_j = 25^\circ$
I_{GT}	Gate trigger current	400 mA	$T_j = 25^\circ$
V_{GD}	Gate non-trigger voltage	0.3 V	$V_D = 0.4 \times V_{DRM}$
I_{GD}	Gate non-trigger current	10 mA	$V_D = 0.4 \times V_{DRM}$
V_{FGM}	Peak forward gate voltage	12 V	
I_{FGM}	Peak forward gate current	10 A	
V_{RGM}	Peak reverse gate voltage	10 V	
P_G	Gate power loss	3 W	

Thermal

T_{jmax}	Max. operating junction temperature range	125 °C	
T_{stg}	Storage temperature range	-40...140 °C	
R_{thJC}	Thermal resistance junction to case	14 K/kW	Anode side cooled
		14 K/kW	Cathode side cooled
		7 K/kW	Double side cooled
R_{thCH}	Thermal resistance case to heat sink	3 K/kW	Single side cooled
		1.5 K/kW	Double side cooled

Analytical function for transient thermal impedance:

$$Z_{thJC}(t) = \sum_{i=1}^n R_i(1 - e^{-t/\tau_i})$$

i	1	2	3	4
$R_i(K/kW)$	4.7	0.853	1.07	0.49
$\tau_i(s)$	0.4787	0.0824	0.0104	0.0041

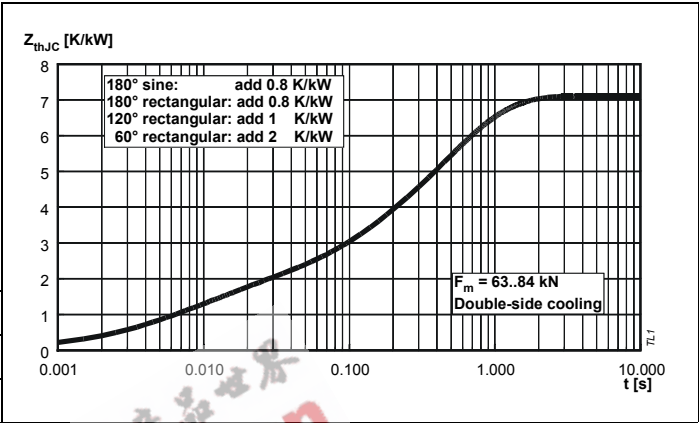


Fig. 1 Transient thermal impedance junction to case.

On-state characteristic model:

$$VT = A + B \cdot iT + C \cdot \ln(iT + 1) + D \cdot \sqrt{iT}$$

Valid for $i_T = 400 - 11000$ A

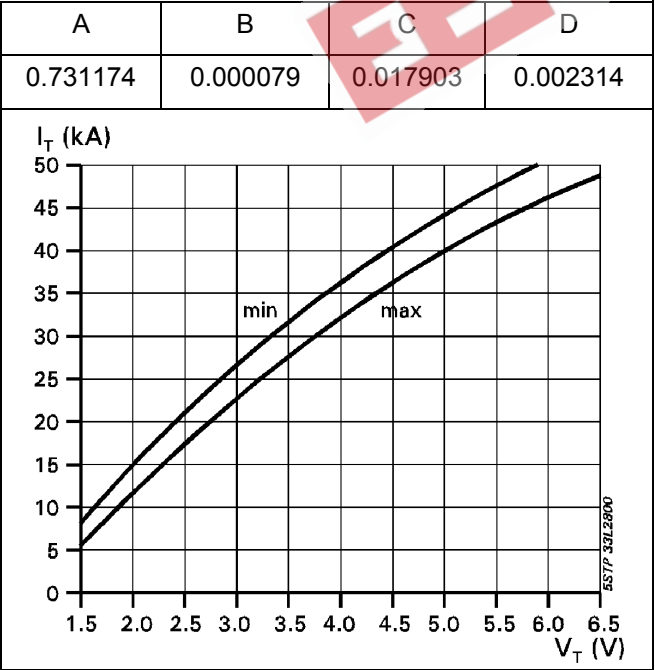


Fig. 2 On-state characteristics.
 $T_j=125^\circ\text{C}$, 10ms half sine

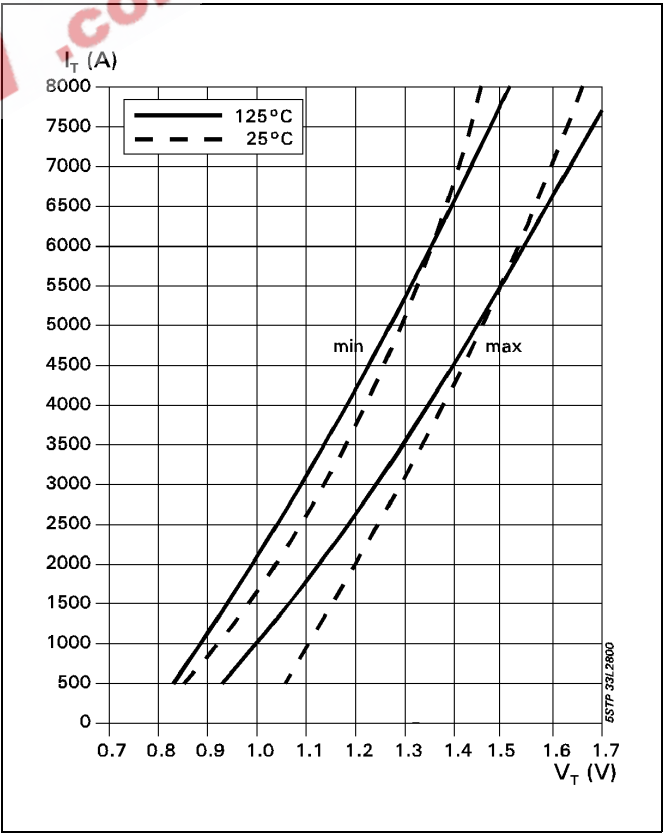


Fig. 3 On-state characteristics.

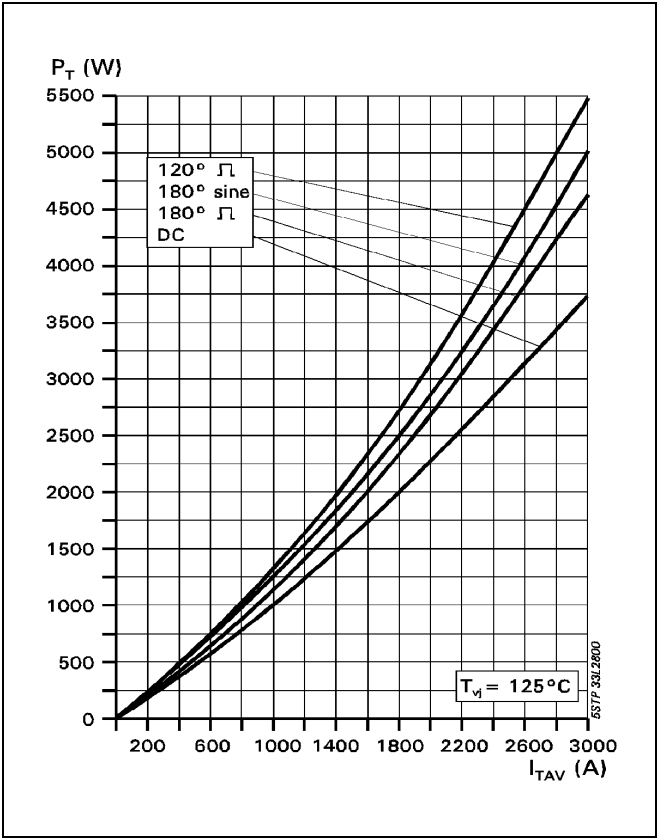


Fig. 4 On-state power dissipation vs. mean on-state current. Turn-on losses excluded.

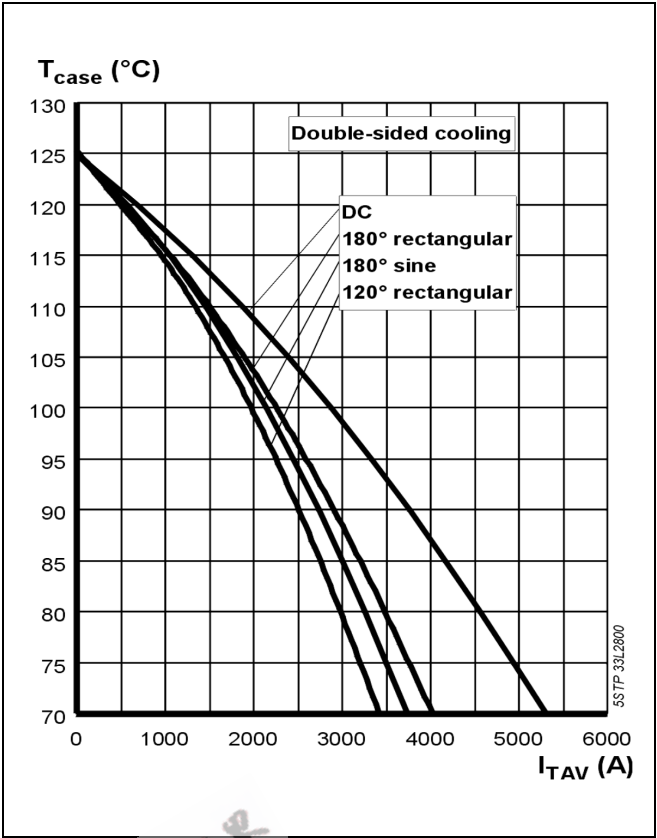


Fig. 5 Max. permissible case temperature vs. mean on-state current.

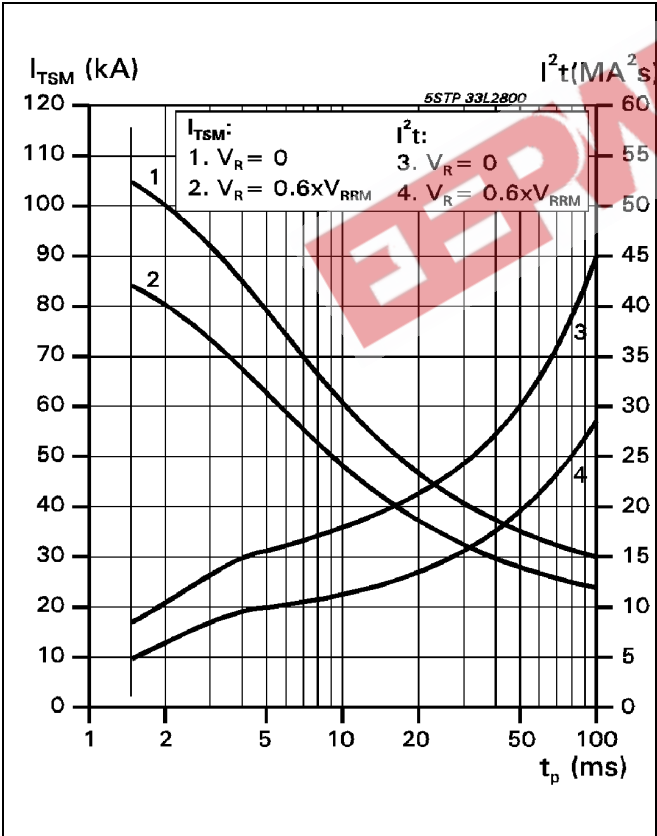


Fig. 6 Surge on-state current vs. pulse length. Half-sine wave.

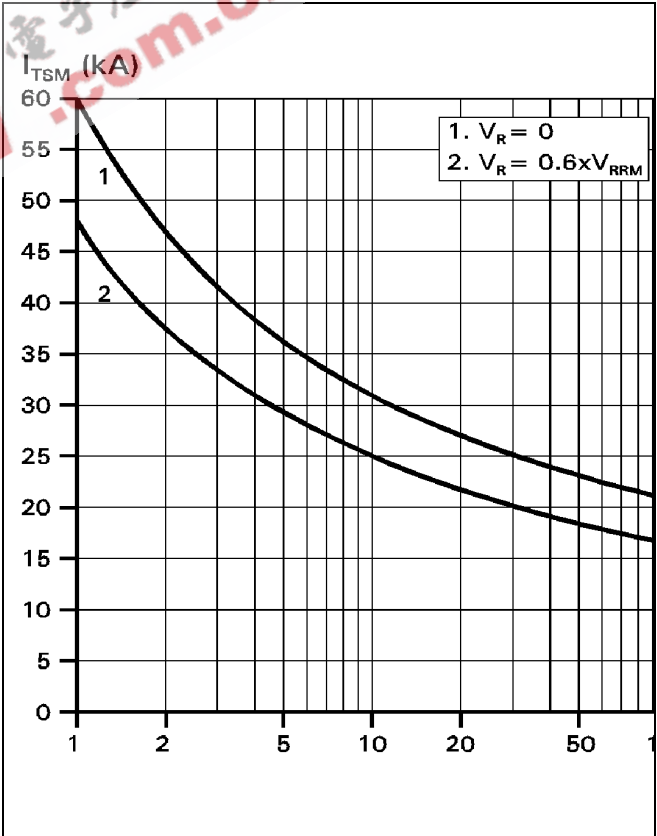


Fig. 7 Surge on-state current vs. number of pulses. Half-sine wave, 10 ms, 50Hz.

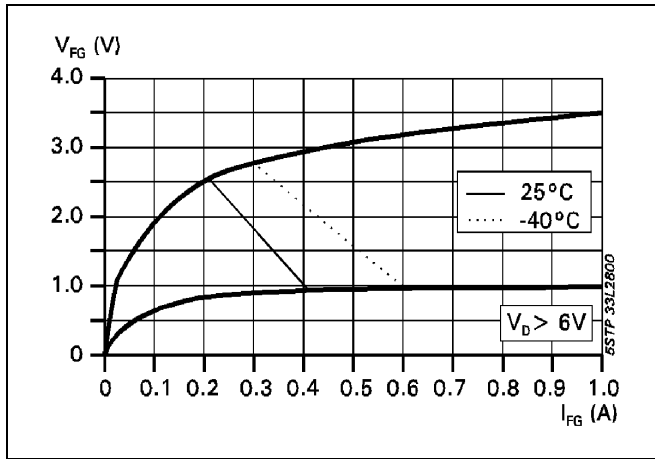


Fig. 8 Gate trigger characteristics.

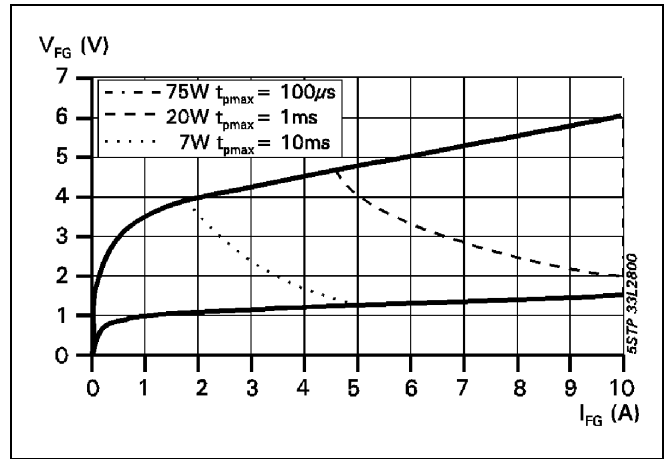


Fig. 9 Max. peak gate power loss.

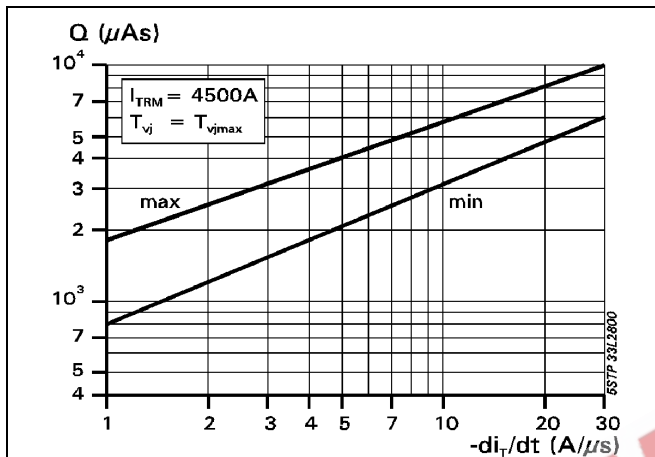


Fig. 10 Recovery charge vs. decay rate of on-state current.

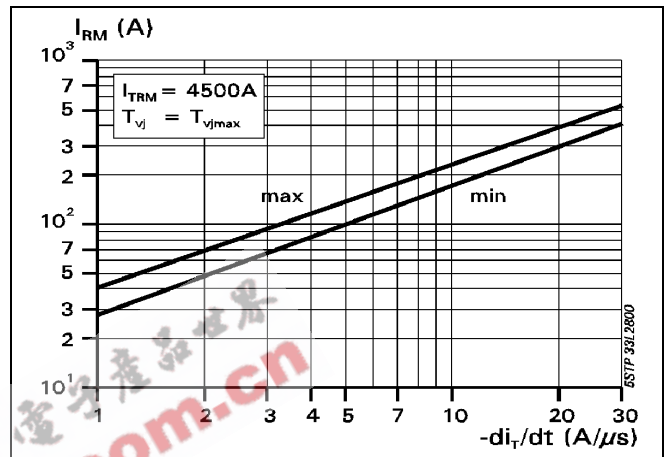
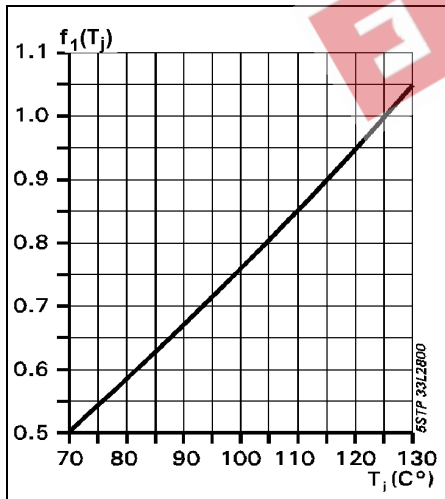
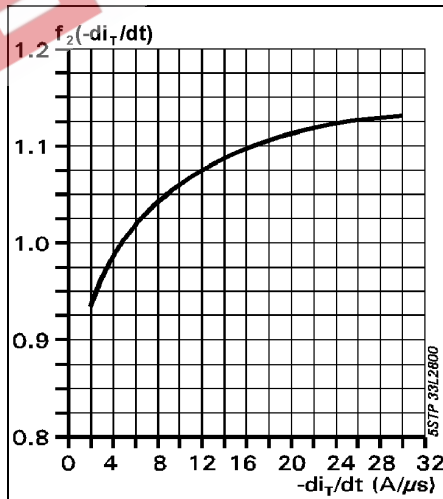
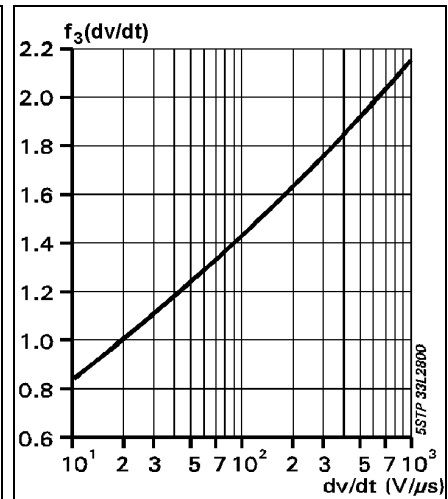


Fig. 11 Peak reverse recovery current vs. decay rate of on-state current.

Turn - off time, typical parameter relationship.

Fig. 12 $t_q/t_{q1} = f_1(T_j)$ Fig. 13 $t_q/t_{q1} = f_2(-di_T/dt)$ Fig. 14 $t_q/t_{q1} = f_3(dv/dt)$

$$t_q = t_{q1} \cdot f_1(T_j) \cdot f_2(-di_T/dt) \cdot f_3(dv/dt)$$

t_{q1} : at normalized values (see page 2)

t_q : at varying conditions

Turn-on and Turn-off losses

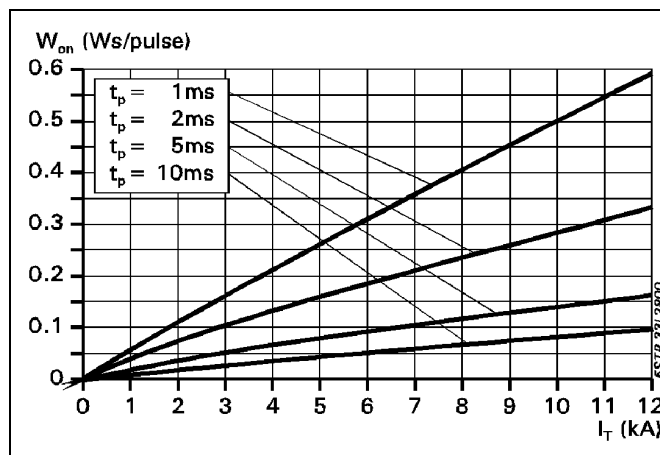


Fig. 15 $W_{on} = f(I_T, t_p)$, $T_j = 125^\circ\text{C}$.
Half sinusoidal waves.

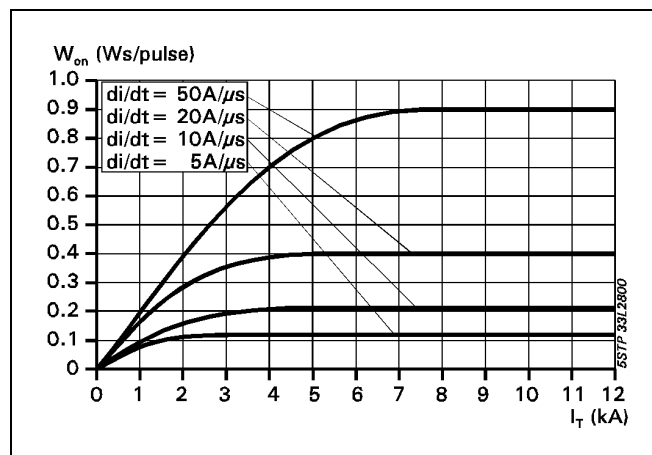


Fig. 16 $W_{on} = f(I_T, di/dt)$, $T_j = 125^\circ\text{C}$.
Rectangular waves.

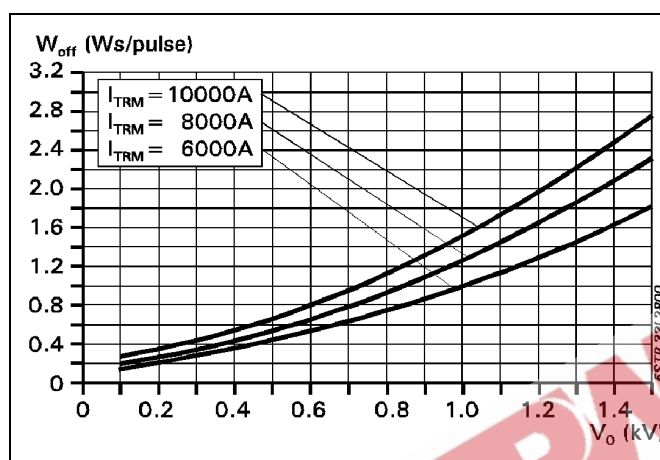


Fig. 17 $W_{off} = f(V_o, I_T)$, $T_j = 125^\circ\text{C}$.
Half sinusoidal waves. $t_p = 10 \text{ ms}$.

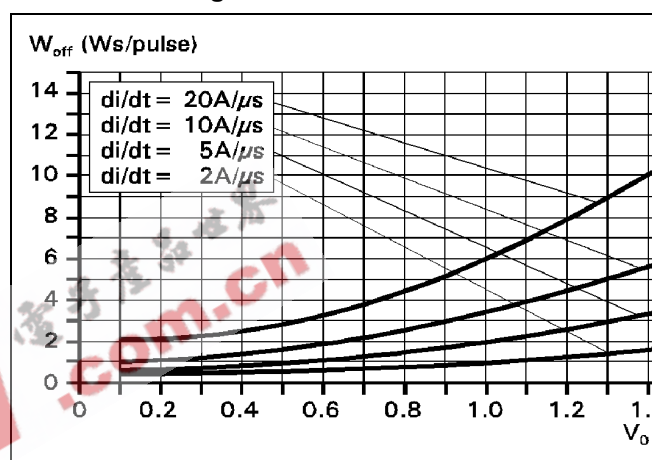


Fig. 18 $W_{off} = f(V_o, di/dt)$, $T_j = 125^\circ\text{C}$.
Rectangular waves.

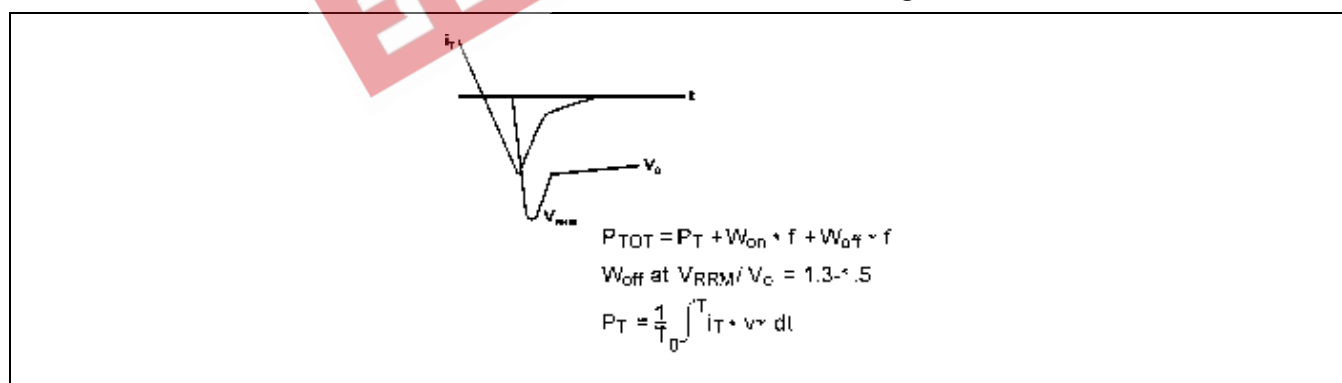


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