

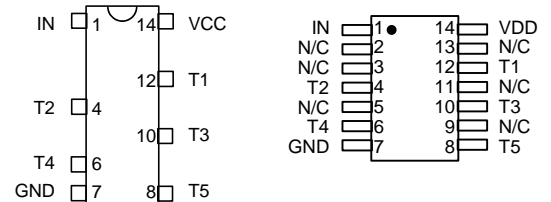
# 5-TAP, TTL-INTERFACED FIXED DELAY LINE (SERIES DDU4F)



## FEATURES

- Five equally spaced outputs
- Fits standard 14-pin DIP socket
- Low profile
- Auto-insertable
- Input & outputs fully TTL interfaced & buffered
- 10 T<sup>2</sup>L fan-out capability

## PACKAGES



DDU4F-xx	DIP	Military SMD
DDU4F-xxA2	Gull-Wing	DDU4F-xxMC2
DDU4F-xxB2	J-Lead	
DDU4F-xxM	Military DIP	

## FUNCTIONAL DESCRIPTION

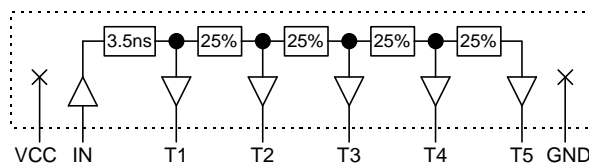
The DDU4F-series device is a 5-tap digitally buffered delay line. The signal input (IN) is reproduced at the outputs (T1-T5), shifted in time by an amount determined by the device dash number (See Table). For dash numbers less than 5025, the total delay of the line is measured from T1 to T5. The nominal tap-to-tap delay increment is given by one-fourth of the total delay, and the inherent delay from IN to T1 is nominally 3.5ns. For dash numbers greater than or equal to 5025, the total delay of the line is measured from IN to T5. The nominal tap-to-tap delay increment is given by one-fifth of this number.

## PIN DESCRIPTIONS

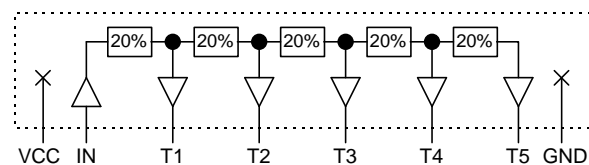
IN	Signal Input
T1-T5	Tap Outputs
VCC	+5 Volts
GND	Ground

## SERIES SPECIFICATIONS

- **Minimum input pulse width:** 20% of total delay
- **Output rise time:** 2ns typical
- **Supply voltage:** 5VDC  $\pm$  5%
- **Supply current:**  $I_{CC1}$  = 32ma typical  
 $I_{CC2}$  = 7ma typical
- **Operating temperature:** 0° to 70° C
- **Temp. coefficient of total delay:** 100 PPM/°C



Functional diagram for dash numbers < 5025



Functional diagram for dash numbers  $\geq$  5025

## DASH NUMBER SPECIFICATIONS

Part Number	Total Delay (ns)	Delay Per Tap (ns)
DDU4F-5004	4 $\pm$ 1.0 *	1.0 $\pm$ 0.5
DDU4F-5006	6 $\pm$ 1.0 *	1.5 $\pm$ 0.5
DDU4F-5008	8 $\pm$ 2.0 *	2.0 $\pm$ 1.0
DDU4F-5010	10 $\pm$ 2.0 *	2.5 $\pm$ 1.0
DDU4F-5012	12 $\pm$ 2.0 *	3.0 $\pm$ 1.0
DDU4F-5016	16 $\pm$ 2.0 *	4.0 $\pm$ 1.5
DDU4F-5020	20 $\pm$ 3.0 *	5.0 $\pm$ 2.0
DDU4F-5025	25 $\pm$ 3.0	5.0 $\pm$ 2.0
DDU4F-5030	30 $\pm$ 3.0	6.0 $\pm$ 2.0
DDU4F-5040	40 $\pm$ 3.0	8.0 $\pm$ 2.0
DDU4F-5050	50 $\pm$ 3.0	10.0 $\pm$ 3.0
DDU4F-5060	60 $\pm$ 3.0	12.0 $\pm$ 3.0
DDU4F-5075	75 $\pm$ 4.0	15.0 $\pm$ 3.0
DDU4F-5100	100 $\pm$ 5.0	20.0 $\pm$ 3.0
DDU4F-5125	125 $\pm$ 6.5	25.0 $\pm$ 3.0
DDU4F-5150	150 $\pm$ 7.5	30.0 $\pm$ 3.0
DDU4F-5200	200 $\pm$ 10.0	40.0 $\pm$ 4.0
DDU4F-5250	250 $\pm$ 12.5	50.0 $\pm$ 5.0
DDU4F-5300	300 $\pm$ 15.0	60.0 $\pm$ 6.0
DDU4F-5400	400 $\pm$ 20.0	80.0 $\pm$ 8.0
DDU4F-5500	500 $\pm$ 25.0	100.0 $\pm$ 10.0

\* Total delay is referenced to first tap output  
Input to first tap = 3.5ns  $\pm$  1ns

NOTE: Any dash number between 5004 and 5500

## APPLICATION NOTES

### HIGH FREQUENCY RESPONSE

The DDU4F tolerances are guaranteed for input pulse widths and periods greater than those specified in the test conditions. Although the device will function properly for pulse widths as small as 20% of the total delay and periods as small as 40% of the total delay (for a symmetric input), the delays may deviate from their values at low frequency. However, for a given input condition, the deviation will be repeatable from pulse to pulse. Contact technical support at Data

Delay Devices if your application requires device testing at a specific input condition.

### POWER SUPPLY BYPASSING

The DDU4F relies on a stable power supply to produce repeatable delays within the stated tolerances. A 0.1uf capacitor from VCC to GND, located as close as possible to the VCC pin, is recommended. A wide VCC trace and a clean ground plane should be used.

## DEVICE SPECIFICATIONS

TABLE 1: ABSOLUTE MAXIMUM RATINGS

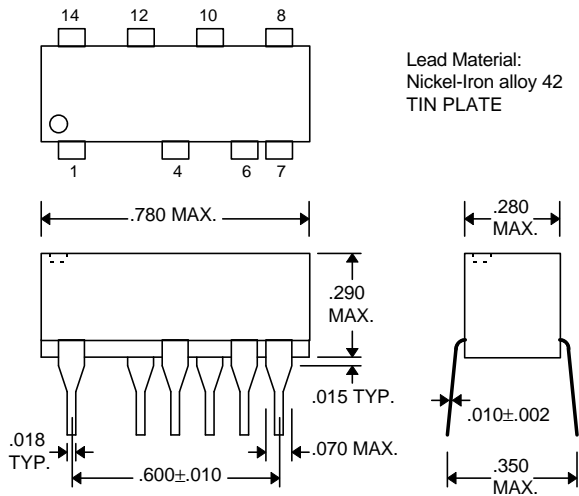
PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
DC Supply Voltage	V <sub>CC</sub>	-0.3	7.0	V	
Input Pin Voltage	V <sub>IN</sub>	-0.3	V <sub>DD</sub> +0.3	V	
Storage Temperature	T <sub>STRG</sub>	-55	150	C	
Lead Temperature	T <sub>LEAD</sub>		300	C	10 sec

TABLE 2: DC ELECTRICAL CHARACTERISTICS

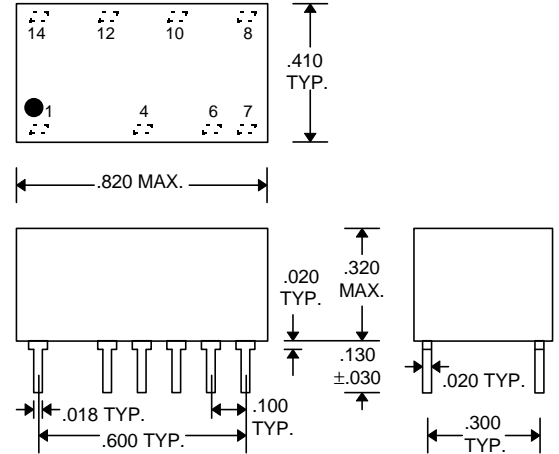
(0C to 70C, 4.75V to 5.25V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
High Level Output Voltage	V <sub>OH</sub>	2.5	3.4		V	V <sub>CC</sub> = MIN, I <sub>OH</sub> = MAX V <sub>IH</sub> = MIN, V <sub>IL</sub> = MAX
Low Level Output Voltage	V <sub>OL</sub>		0.35	0.5	V	V <sub>CC</sub> = MIN, I <sub>OL</sub> = MAX V <sub>IH</sub> = MIN, V <sub>IL</sub> = MAX
High Level Output Current	I <sub>OH</sub>			-1.0	mA	
Low Level Output Current	I <sub>OL</sub>			20.0	mA	
High Level Input Voltage	V <sub>IH</sub>	2.0			V	
Low Level Input Voltage	V <sub>IL</sub>			0.8	V	
Input Clamp Voltage	V <sub>IK</sub>			-1.2	V	V <sub>CC</sub> = MIN, I <sub>I</sub> = I <sub>IK</sub>
Input Current at Maximum Input Voltage	I <sub>IHH</sub>			0.1	mA	V <sub>CC</sub> = MAX, V <sub>I</sub> = 7.0V
High Level Input Current	I <sub>IH</sub>			20	μA	V <sub>CC</sub> = MAX, V <sub>I</sub> = 2.7V
Low Level Input Current	I <sub>IL</sub>			-0.6	mA	V <sub>CC</sub> = MAX, V <sub>I</sub> = 0.5V
Short-circuit Output Current	I <sub>OS</sub>	-60		-150	mA	V <sub>CC</sub> = MAX
Output High Fan-out				25	Unit	
Output Low Fan-out				12.5	Load	

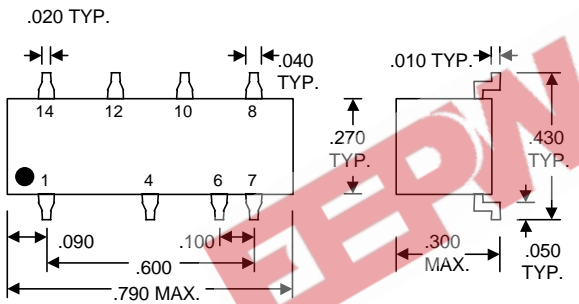
PACKAGE DIMENSIONS



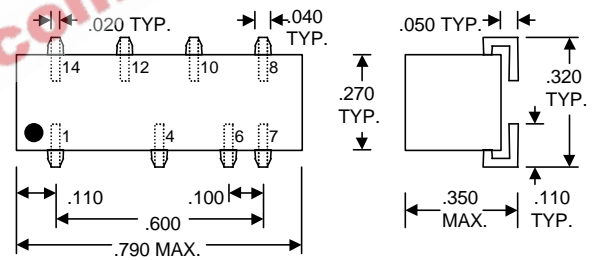
DDU4F-xx (Commercial DIP)



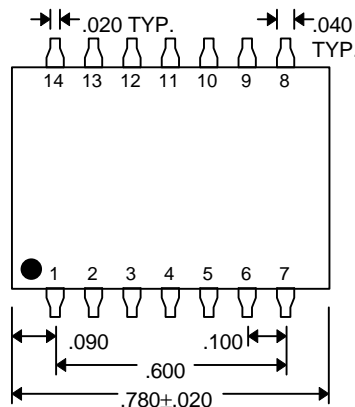
DDU4F-xxM (Military DIP)



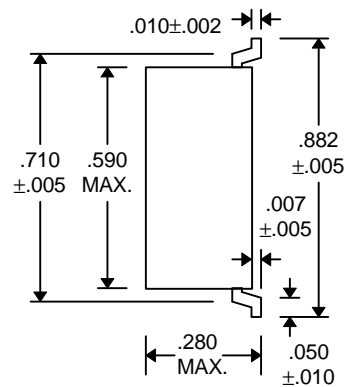
DDU4F-xxA2 (Commercial Gull-Wing)



DDU4F-xxB2 (Commercial J-Lead)



DDU4F-xxMC2 (Military SMD)



## DELAY LINE AUTOMATED TESTING

### TEST CONDITIONS

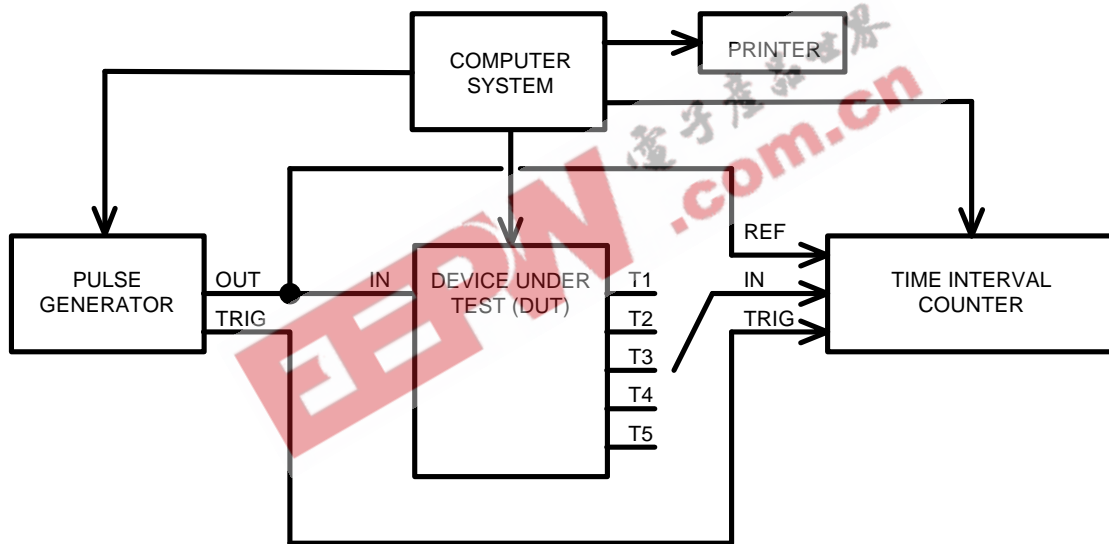
#### INPUT:

**Ambient Temperature:**  $25^{\circ}\text{C} \pm 3^{\circ}\text{C}$   
**Supply Voltage (Vcc):**  $5.0\text{V} \pm 0.1\text{V}$   
**Input Pulse:** High =  $3.0\text{V} \pm 0.1\text{V}$   
 Low =  $0.0\text{V} \pm 0.1\text{V}$   
**Source Impedance:**  $50\Omega$  Max.  
**Rise/Fall Time:**  $3.0\text{ ns}$  Max. (measured  
 between  $0.6\text{V}$  and  $2.4\text{V}$ )  
**Pulse Width:**  $\text{PW}_{\text{IN}} = 1.5 \times \text{Total Delay}$   
**Period:**  $\text{PER}_{\text{IN}} = 10 \times \text{Total Delay}$

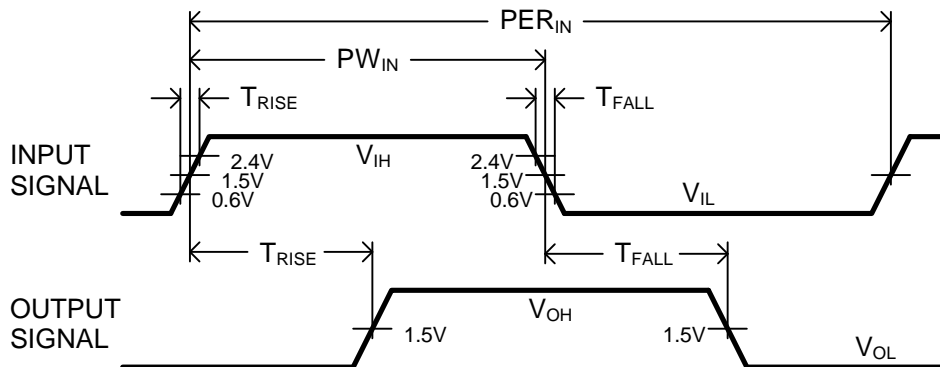
#### OUTPUT:

**Load:** 1 FAST-TTL Gate  
 **$C_{\text{load}}$ :**  $5\text{pf} \pm 10\%$   
**Threshold:**  $1.5\text{V}$  (Rising & Falling)

**NOTE:** The above conditions are for test only and do not in any way restrict the operation of the device.



Test Setup



Timing Diagram For Testing