



+5 V Low Power RS-485 PROFIBUS Transceiver

Preliminary Technical Data

ADM1486

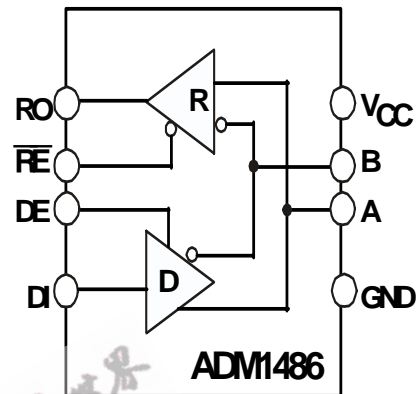
FEATURES

- Meets & Exceeds EIA RS-485 & EIA RS-422 Standard
- 50 Mb/s Data Rate
- Recommended for PROFIBUS Applications
- 2.1V Minimum Differential Output with 54Ω Termination
- Low Power 0.5mA I_{CC}
- Thermal Shutdown & Short Circuit Protection
- Zero Skew Driver & Receiver
- Driver Propagation Delay: 8 ns
- Receiver Propagation Delay: 12 ns
- High Z Outputs with Drivers Disabled or Power Off
- Superior Upgrade for SN65ALS1176
- 15kV HBM ESD Protection on I/O Pins A & B
- Available in Standard 8-pin SOIC & Miniature 8-pin Micro SOIC packages

APPLICATIONS

Industrial Field Equipment

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The ADM1486 is a differential line transceiver suitable for high speed bidirectional data communication on multipoint bus transmission lines. It is designed for balanced data transmission, complies with EIA Standards RS-485 and RS-422 and is recommended for PROFIBUS applications. The part contains a differential line driver and a differential line receiver. Both the driver and the receiver may be enabled independently. When disabled or with power off, the driver outputs are tristated.

The ADM1486 operates from a single +5 V power supply. Excessive power dissipation caused by bus contention or by output shorting is prevented by a thermal shutdown circuit. This feature forces the driver output into a high impedance state if during fault conditions a significant temperature increase is detected in the internal driver circuitry.

Up to 50 transceivers may be connected simultaneously on a bus, but only one driver should be enabled at any time. It is important therefore that the remaining disabled drivers do not load the bus. To ensure this, the ADM1486 driver features high output impedance when disabled and also when powered down.

This minimizes the loading effect when the transceiver is not being utilized. The high impedance driver output is maintained over the entire common-mode voltage range from -7 V to +12 V.

The receiver contains a fail safe feature which results in a logic high output state if the inputs are unconnected (floating).

The ADM1486 is fabricated on BiCMOS, an advanced mixed technology process combining low power CMOS with fast switching bipolar technology. All inputs and outputs contain protection against ESD; all driver outputs feature high source and sink current capability. An epitaxial layer is used to guard against latch-up.

The ADM1486 features extremely fast switching speeds. Minimal driver propagation delays permit transmission at data rates up to 50 Mbits/s while low skew minimizes EMI interference.

The part is fully specified over the commercial and industrial temperature range and is available in an 8-lead DIL/SOIC/μSOIC package.

REV Pr. B

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ADM1486—SPECIFICATIONS

($V_{CC} = +5\text{ V} \pm 5\%$. All specifications T_{MIN} to T_{MAX} unless otherwise noted.)

| Parameter | Min | Typ | Max | Unit | Test Conditions/Comments |
|---|------|-----|-----------|---------------|--|
| DRIVER | | | | | |
| Differential Output Voltage, V_{OD} | | | 5.0 | V | R = Infinity, Figure 1 |
| | 2.0 | | 5.0 | V | $V_{CC} = 5\text{ V}$, R = 50 Ω (RS-422), Figure 1 |
| | 2.1 | | 5.0 | V | R = 27 Ω (RS-485), Figure 1 |
| V_{OD3} | 2.1 | | 5.0 | V | $V_{TST} = -7\text{ V}$ to $+12\text{ V}$, Figure 2 |
| $\Delta V_{OD} $ for Complementary Output States | | | 0.2 | V | R = 27 Ω or 50 Ω , Figure 1 |
| Common-Mode Output Voltage V_{OC} | | | 3 | V | R = 27 Ω or 50 Ω , Figure 1 |
| $\Delta V_{OD} $ for Complementary Output States | | | 0.2 | V | R = 27 Ω or 50 Ω |
| Output Short Circuit Current($V_{OUT}=\text{High}$) | 60 | | 150 | mA | $-7\text{ V} \leq V_O \leq +12\text{ V}$ |
| Output Short Circuit Current($V_{OUT}=\text{Low}$) | 60 | | 150 | mA | $-7\text{ V} \leq V_O \leq +12\text{ V}$ |
| CMOS Input Logic Threshold Low, V_{INL} | | | 0.8 | V | |
| CMOS Input Logic Threshold High, V_{INH} | 2.0 | | | V | |
| Logic Input Current (DE, DI) | | | ± 1.0 | μA | |
| RECEIVER | | | | | |
| Differential Input Threshold Voltage, V_{TH} | -0.2 | | +0.2 | V | $-7\text{ V} \leq V_{CM} \leq +12\text{ V}$ |
| Input Voltage Hysteresis, ΔV_{TH} | | 70 | | mV | $V_{CM} = 0\text{ V}$ |
| Input Resistance | 20 | | | k Ω | $-7\text{ V} \leq V_{CM} \leq +12\text{ V}$ |
| Input Current (A, B) | | | + 1 | mA | $V_{IN} = 12\text{ V}$ |
| | | | -0.8 | mA | $V_{IN} = -7\text{ V}$ |
| Logic Enable Input Current (\overline{RE}) | | | ± 1 | μA | |
| CMOS Output Voltage Low, V_{OL} | | | 0.4 | V | $I_{OUT} = +4.0\text{ mA}$ |
| CMOS Output Voltage High, V_{OH} | 4.0 | | | V | $I_{OUT} = -4.0\text{ mA}$ |
| Short Circuit Output Current | 7 | | 85 | mA | $V_{OUT} = \text{GND}$ or V_{CC} |
| Tristate Output Leakage Current | | | ± 1.0 | μA | $0.4\text{ V} \leq V_{OUT} \leq +2.4\text{ V}$ |
| POWER SUPPLY CURRENT | | | | | |
| I_{CC} (Outputs Enabled) | | 1.2 | 2.0 | mA | Outputs Unloaded, Digital Inputs = GND or V_{CC} |
| I_{CC} (Outputs Disabled) | | 0.9 | 1.5 | mA | Outputs Unloaded, Digital Inputs = GND or V_{CC} |

Specifications subject to change without notice.

TIMING SPECIFICATIONS

($V_{CC} = +5\text{ V} \pm 5\%$. All specifications T_{MIN} to T_{MAX} unless otherwise noted.)

| Parameter | Min | Typ | Max | Unit | Test Conditions/Comments |
|---|-----|-----|-----|------|--|
| DRIVER | | | | | |
| Propagation Delay Input to Output T_{PLH} , T_{PHL} | 4 | 8 | 15 | ns | $R_L \text{ Diff} = 54\ \Omega$ $C_{L1} = C_{L2} = 100\text{ pF}$, Figure 3 |
| Driver O/P to O/P T_{SKEW} | | 0 | 2 | ns | $R_L \text{ Diff} = 54\ \Omega$ $C_{L1} = C_{L2} = 100\text{ pF}$, Figure 3 |
| Driver Rise/Fall Time T_R , T_F | | 5 | 10 | ns | $R_L \text{ Diff} = 54\ \Omega$ $C_{L1} = C_{L2} = 100\text{ pF}$, Figure 3 |
| Driver Enable to Output Valid | | 8 | 15 | ns | |
| Driver Disable Timing | | 8 | 15 | ns | |
| RECEIVER | | | | | |
| Propagation Delay Input to Output T_{PLH} , T_{PHL} | | 8 | 12 | 20 | ns $C_L = 15\text{ pF}$, Figure 5 |
| Skew $ T_{PLH} - T_{PHL} $ | | 0 | 2 | ns | |
| Receiver Enable T_{EN1} | | 5 | 10 | ns | Figure 6 |
| Receiver Disable T_{EN2} | | 5 | 10 | ns | Figure 6 |

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

(T_A = +25°C unless otherwise noted)

| | |
|--|-----------------------------------|
| V _{CC} | +7 V |
| Inputs | |
| Driver Input (DI) | -0.3 V to V _{CC} + 0.3 V |
| Control Inputs (DE, RE) | -0.3 V to V _{CC} + 0.3 V |
| Receiver Inputs (A, B) | -9 V to +14 V |
| Outputs | |
| Driver Outputs | -9 V to +14 V |
| Receiver Output | -0.5 V to V _{CC} + 0.5 V |
| Power Dissipation 8-Lead DIP | 500 mW |
| θ _{JA} , Thermal Impedance | +130°C/W |
| Power Dissipation 8-Lead SOIC | 450 mW |
| θ _{JA} , Thermal Impedance | +170°C/W |
| Power Dissipation 8-Lead Cerdip | 500 mW |
| θ _{JA} , Thermal Impedance | +125°C/W |
| Power Dissipation 8-Lead μSOIC | mW |
| θ _{JA} , Thermal Impedance | +°C/W |
| Operating Temperature Range | |
| Commercial (J Version) | 0°C to +70°C |
| Industrial (A Version) | -40°C to +85°C |
| Storage Temperature Range | -65°C to +150°C |
| Lead Temperature (Soldering, 10 sec) | +300°C |
| Vapor Phase (60 sec) | +215°C |
| Infrared (15 sec) | +220°C |

*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods of time may affect device reliability.

Table I. Transmitting

| RE | INPUTS | | OUTPUTS | |
|----|--------|----|---------|---|
| | DE | DI | B | A |
| X | 1 | 1 | 0 | 1 |
| X | 1 | 0 | 1 | 0 |
| X | 0 | X | Z | Z |

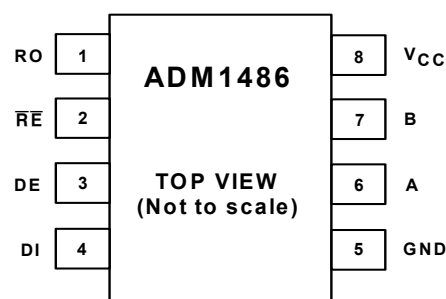
Table II. Receiving

| RE | INPUTS | | OUTPUT RO |
|----|--------|-------------|-----------|
| | DE | A-B | |
| 0 | 0 | ≥+0.2 V | 1 |
| 0 | 0 | ≤-0.2 V | 0 |
| 0 | 0 | Inputs Open | 1 |
| 1 | 0 | X | Z |

PIN FUNCTION DESCRIPTION

| Pin | Mnemonic | Function |
|-----|-----------------|---|
| 1 | RO | Receiver Output. When enabled if A > B by 200 mV, then RO = High. If A < B by 200 mV, then RO = Low. |
| 2 | RE | Receiver Output Enable. A low level enables the receiver output, RO. A high level places it in a high impedance state. |
| 3 | DE | Driver Output Enable. A high level enables the driver differential outputs, A and B. A low level places it in a high impedance state. |
| 4 | DI | Driver Input. When the driver is enabled a logic Low on DI forces A low and B high while a logic High on DI forces A high and B low. |
| 5 | GND | Ground Connection, 0 V. |
| 6 | A | Noninverting Receiver Input A/Driver Output A. |
| 7 | B | Inverting Receiver Input B/Driver Output B. |
| 8 | V _{CC} | Power Supply, 5 V ± 5%. |

PIN CONFIGURATION



ORDERING GUIDE

| Model | Temperature Range | Package Option |
|------------|-------------------|----------------|
| ADM1486JN | 0°C to +70°C | N-8 |
| ADM1486JR | 0°C to +70°C | SO-8 |
| ADM1486AN | -40°C to +85°C | N-8 |
| ADM1486AR | -40°C to +85°C | SO-8 |
| ADM1486ARM | -40°C to +85°C | RM-8 |
| ADM1486AQ | -40°C to +85°C | Q-8 |

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADM1486 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



ADM1486

Test Circuits

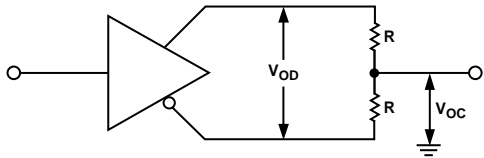


Figure 1. Driver Voltage Measurement Test Circuit

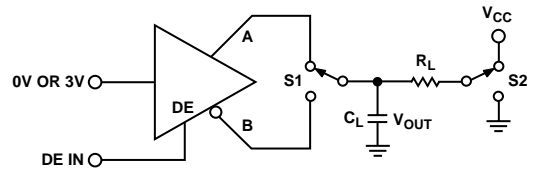


Figure 4. Driver Enable/Disable Test Circuit

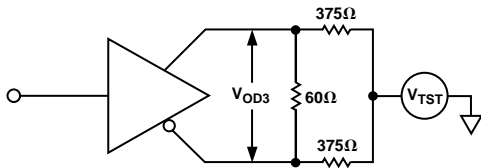


Figure 2. Driver Voltage Measurement Test Circuit 2

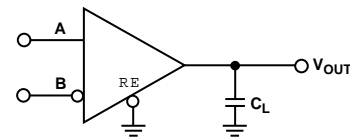


Figure 5. Receiver Propagation Delay Test Circuit

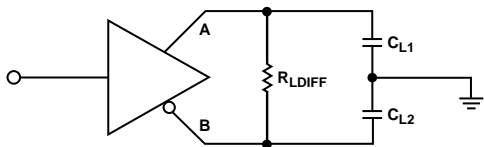


Figure 3. Driver Propagation Delay Test Circuit

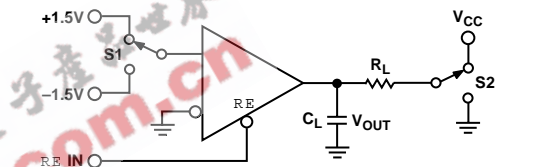


Figure 6. Receiver Enable/Disable Test Circuit

Switching Characteristics

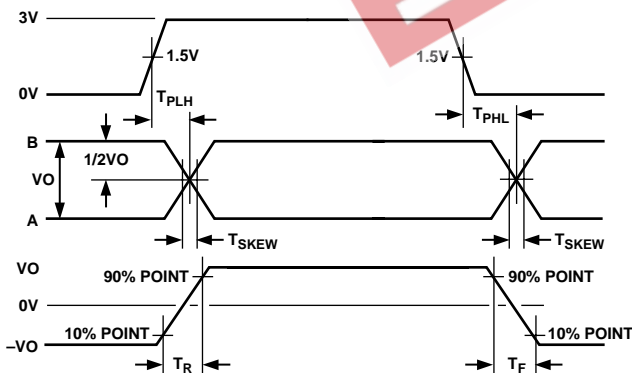


Figure 7. Driver Propagation Delay, Rise/Fall Timing

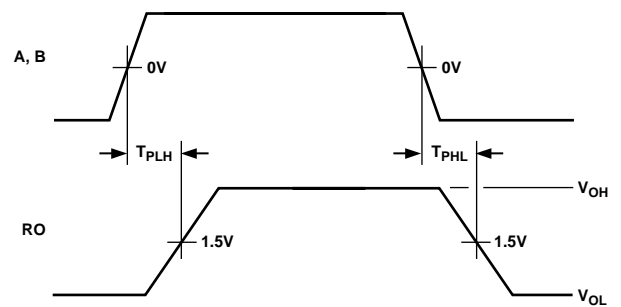


Figure 9. Receiver Propagation Delay

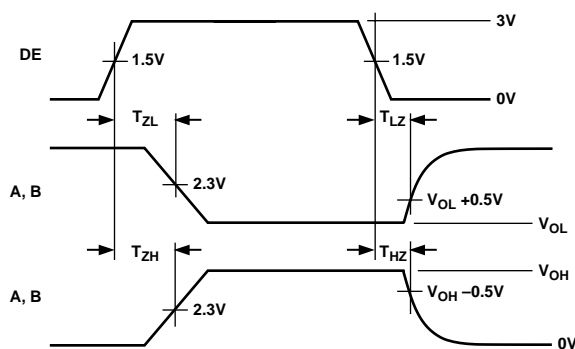


Figure 8. Driver Enable/Disable Timing

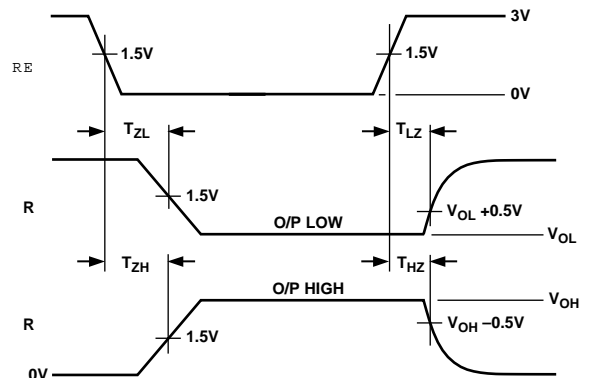


Figure 10. Receiver Enable/Disable Timing

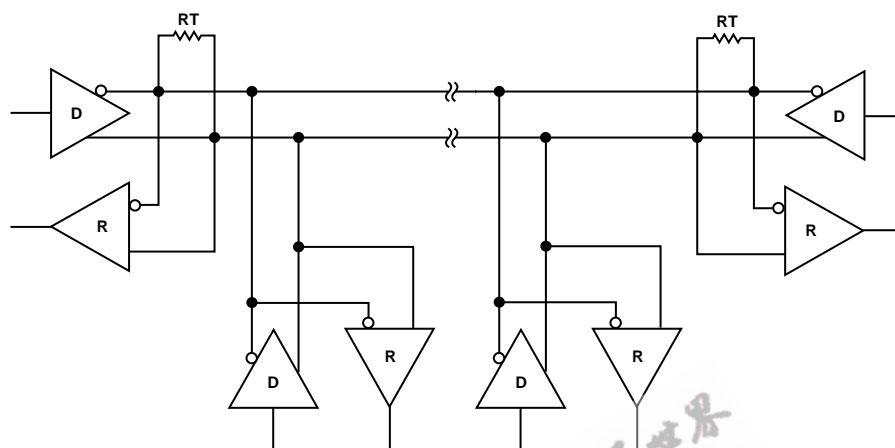


Figure 11. Typical RS-485 Network

Table III. Comparison of RS-422 and RS-485 Interface Standards

| Specification | RS-422 | RS-485 | PROFIBUS |
|----------------------------------|------------------|-------------------|--------------------|
| Transmission Type | Differential | Differential | Differential |
| Maximum Cable Length | 4000 ft. | 4000 ft. | - |
| Minimum Driver Output Voltage | ± 2 V | ± 1.5 V | ± 2.1 V |
| Driver Load Impedance | 100 Ω | 54 Ω | 54 Ω |
| Receiver Input Resistance | 4 k Ω min | 12 k Ω min | 200 k Ω min |
| Receiver Input Sensitivity | ± 200 mV | ± 200 mV | ± 200 mV |
| Receiver Input Voltage Range | -7 V to +7 V | -7 V to +12 V | -7 V to +12 V |
| No of Drivers/Receivers Per Line | 1/10 | 32/32 | 50/50 |

ADM1486

APPLICATIONS INFORMATION

Differential Data Transmission

Differential data transmission is used to reliably transmit data at high rates over long distances and through noisy environments. Differential transmission nullifies the effects of ground shifts and noise signals which appear as common-mode voltages on the line. There are two main standards approved by the Electronics Industries Association (EIA) which specify the electrical characteristics of transceivers used in differential data transmission.

The RS-422 standard specifies data rates up to 10 Mbaud and line lengths up to 4000 ft. A single driver can drive a transmission line with up to 10 receivers.

In order to cater for true multipoint communications, the RS-485 standard was defined. This standard meets or exceeds all the requirements of RS-422 but also allows for up to 32 drivers and 32 receivers to be connected to a single bus. An extended common-mode range of -7 V to $+12$ V is defined. The most significant difference between RS-422 and RS-485 is the fact that the drivers may be disabled thereby allowing more than one (32 in fact) to be connected to a single line. Only one driver should be enabled at time, but the RS-485 standard contains additional specifications to guarantee device safety in the event of line contention.

Cable and Data Rate

The transmission line of choice for RS-485 communications is a twisted pair. Twisted pair cable tends to cancel common-mode noise and also causes cancellation of the magnetic fields generated by the current

flowing through each wire, thereby, reducing the effective inductance of the pair.

The ADM1486 is designed for bidirectional data communications on multipoint transmission lines. A typical application showing a multipoint transmission network is illustrated in Figure 11. An RS-485 transmission line can have as many as 32 transceivers on the bus. Only one driver can transmit at a particular time but multiple receivers may be enabled simultaneously.

As with any transmission line, it is important that reflections are minimized. This may be achieved by terminating the extreme ends of the line using resistors equal to the characteristic impedance of the line. Stub lengths of the main line should also be kept as short as possible. A properly terminated transmission line appears purely resistive to the driver.

Thermal Shutdown

The ADM1486 contains thermal shutdown circuitry which protects the part from excessive power dissipation during fault conditions. Shorting the driver outputs to a low impedance source can result in high driver currents. The thermal sensing circuitry detects the increase in die temperature and disables the driver outputs. The thermal sensing circuitry is designed to disable the driver outputs when a die temperature of 150°C is reached. As the device cools, the drivers are re-enabled at 140°C .

Propagation Delay

The ADM1486 features very low propagation delay ensuring maximum baud rate operation. The driver is well balanced ensuring distortion free transmission.

Another important specification is a measure of the skew between the complementary outputs. Excessive skew impairs the noise immunity of the system and increases the amount of electromagnetic interference (EMI).

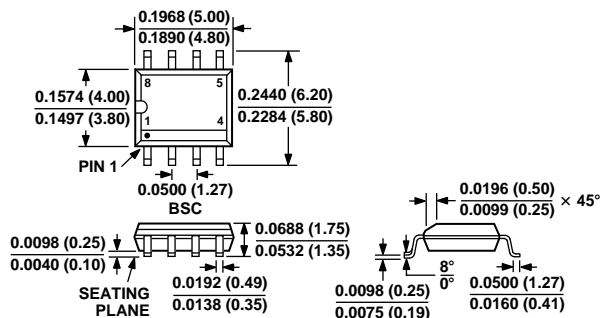
Receiver Open-Circuit Fail Safe

The receiver input includes a fail-safe feature which guarantees a logic high on the receiver when the inputs are open circuit or floating.

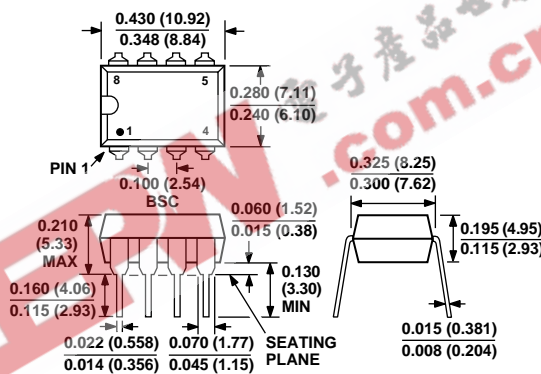
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

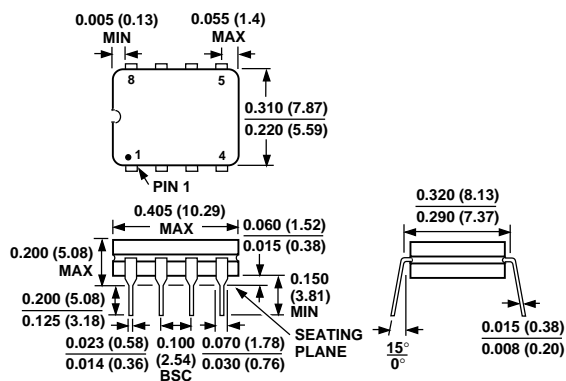
8-Lead SOIC (SO-8)



8-Lead Plastic DIP (N-8)



8-Lead Cerdip (Q-8)

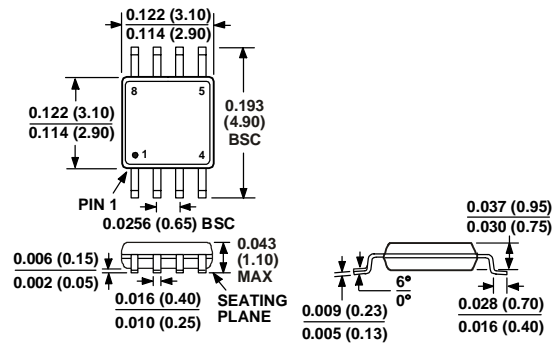


ADM1486

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

8-Lead μ SOIC (RM-8)



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