



## APPLICATION NOTES

### HIGH FREQUENCY RESPONSE

The DDU222C tolerances are guaranteed for input pulse widths and periods greater than those specified in the test conditions. Although the device will function properly for pulse widths as small as 40% of the total delay and periods as small as 80% of the total delay (for a symmetric input), the delays may deviate from their values at low frequency. However, for a given input condition, the deviation will be repeatable from pulse to pulse. Contact technical support at Data

Delay Devices if your application requires device testing at a specific input condition.

### POWER SUPPLY BYPASSING

The DDU222C relies on a stable power supply to produce repeatable delays within the stated tolerances. A 0.1uf capacitor from VDD to GND, located as close as possible to the VDD pin, is recommended. A wide VDD trace and a clean ground plane should be used.

## DEVICE SPECIFICATIONS

**TABLE 1: ABSOLUTE MAXIMUM RATINGS**

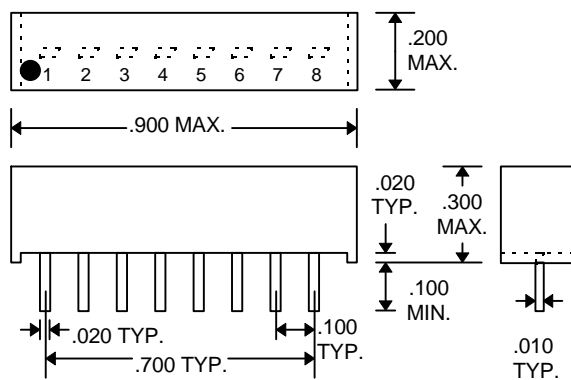
PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
DC Supply Voltage	V <sub>DD</sub>	-0.3	7.0	V	
Input Pin Voltage	V <sub>IN</sub>	-0.3	V <sub>DD</sub> +0.3	V	
Storage Temperature	T <sub>STRG</sub>	-55	150	C	
Lead Temperature	T <sub>LEAD</sub>		300	C	10 sec

**TABLE 2: DC ELECTRICAL CHARACTERISTICS**

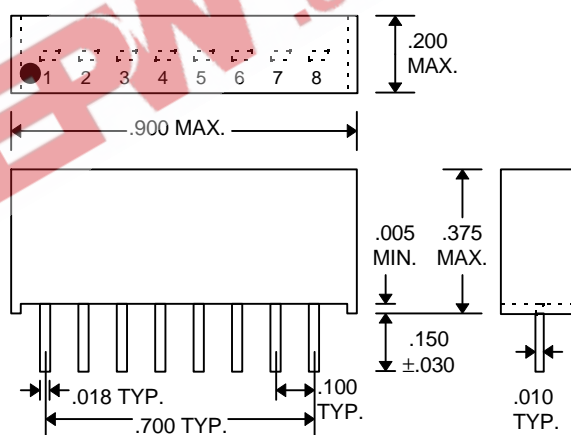
(0C to 70C, 4.75V to 5.25V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
High Level Output Voltage	V <sub>OH</sub>	3.98	4.4		V	V <sub>DD</sub> = 5.0, I <sub>OH</sub> = MAX V <sub>IH</sub> = MIN, V <sub>IL</sub> = MAX
Low Level Output Voltage	V <sub>OL</sub>		0.15	0.26	V	V <sub>DD</sub> = 5.0, I <sub>OL</sub> = MAX V <sub>IH</sub> = MIN, V <sub>IL</sub> = MAX
High Level Output Current	I <sub>OH</sub>			-4.0	mA	
Low Level Output Current	I <sub>OL</sub>			4.0	mA	
High Level Input Voltage	V <sub>IH</sub>	3.15			V	
Low Level Input Voltage	V <sub>IL</sub>			1.35	V	
Input Current	I <sub>IH</sub>			0.10	μA	V <sub>DD</sub> = 5.0

## PACKAGE DIMENSIONS



### DDU222C-xx (Commercial)



### DDU222C-xxM (Military)

## DELAY LINE AUTOMATED TESTING

### TEST CONDITIONS

#### INPUT:

**Ambient Temperature:**  $25^{\circ}\text{C} \pm 3^{\circ}\text{C}$   
**Supply Voltage (VDD):**  $5.0\text{V} \pm 0.1\text{V}$   
**Input Pulse:** High =  $5.0\text{V} \pm 0.1\text{V}$   
 Low =  $0.0\text{V} \pm 0.1\text{V}$

**Source Impedance:**  $50\Omega$  Max.

**Rise/Fall Time:** 5.0 ns Max. (measured between 0.5V and 4.5V)

**Pulse Width:**  $PW_{IN} = 1.5 \times \text{Total Delay}$

**Period:**  $PER_{IN} = 10 \times \text{Total Delay}$

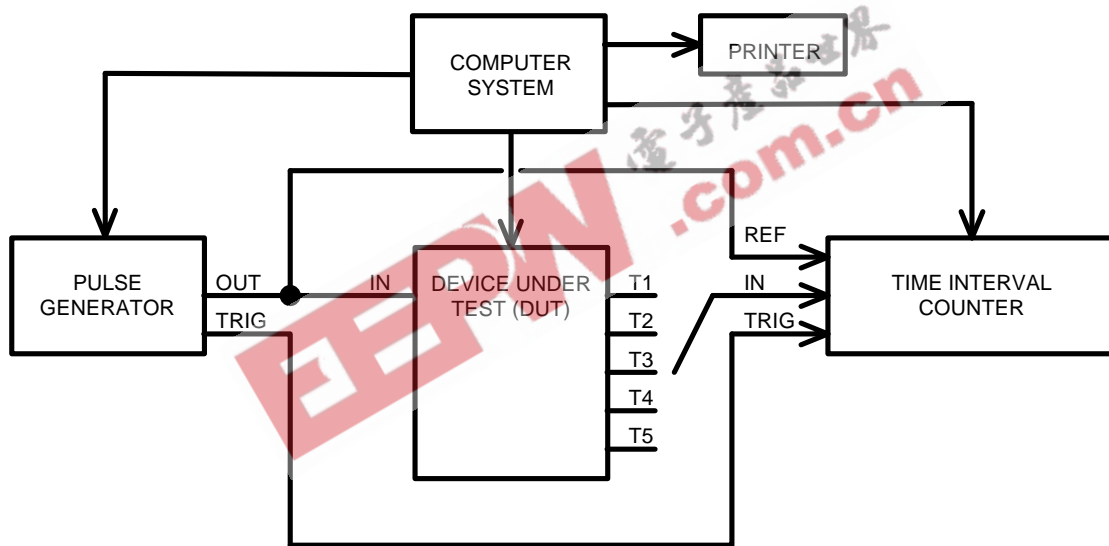
#### OUTPUT:

**Load:** 1 FAST-TTL Gate

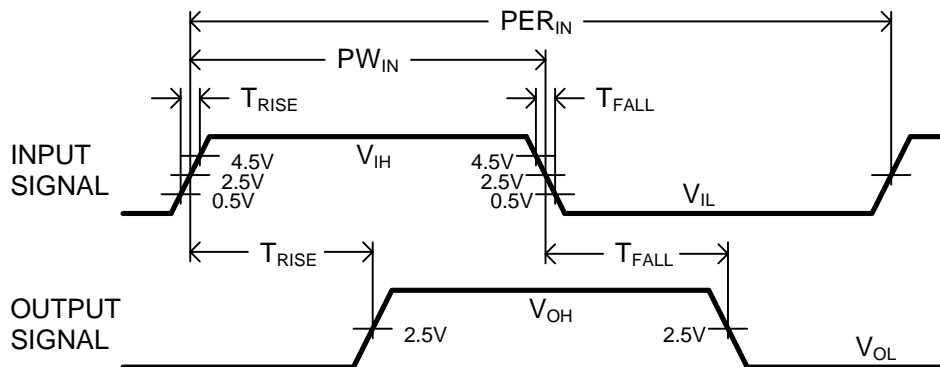
**C<sub>load</sub>:**  $5\text{pf} \pm 10\%$

**Threshold:** 2.5V (Rising & Falling)

**NOTE:** The above conditions are for test only and do not in any way restrict the operation of the device.



Test Setup



Timing Diagram For Testing