X28HC64

64K, 8K x 8 Bit

Data Sheet | June 1, 2005 | FN8109.0

5 Volt, Byte Alterable EEPROM

FEATURES

- 70ns access time
- Simple byte and page write
  - —Single 5V supply
  - —No external high voltages or V_{PP} control circuits
  - —Self-timed
  - —No erase before write
  - —No complex programming algorithms
  - —No overerase problem
- Low power CMOS
  - —40mA active current max.
  - —200µA standby current max.
- Fast write cycle times
  - —64-byte page write operation
  - —Byte or page write cycle: 2ms typical
  - —Complete memory rewrite: 0.25 sec. typical
  - —Effective byte write cycle time: 32µs typical
- Software data protection
- End of write detection
  - —DATA polling
  - —Toggle bit
- High reliability
  - —Endurance: 1 million cycles
  - —Data retention: 100 years
- JEDEC approved byte-wide pin out

DESCRIPTION

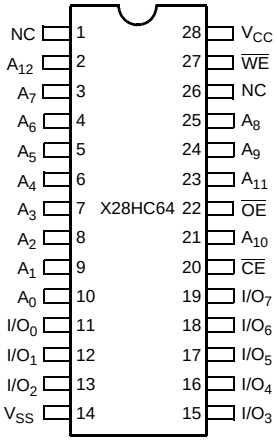
The X28HC64 is an 8K x 8 EEPROM, fabricated with Intersil's proprietary, high performance, floating gate CMOS technology. Like all Intersil programmable non-volatile memories, the X28HC64 is a 5V only device. It features the JEDEC approved pinto for byte-wide memories, compatible with industry standard RAMs.

The X28HC64 supports a 64-byte page write operation, effectively providing a 32µs/byte write cycle, and enabling the entire memory to be typically written in 0.25 seconds. The X28HC64 also features $\overline{\text{DATA}}$ Polling and Toggle Bit Polling, two methods providing early end of write detection. In addition, the X28HC64 includes a user-optional software data protection mode that further enhances Intersil's hardware write protect capability.

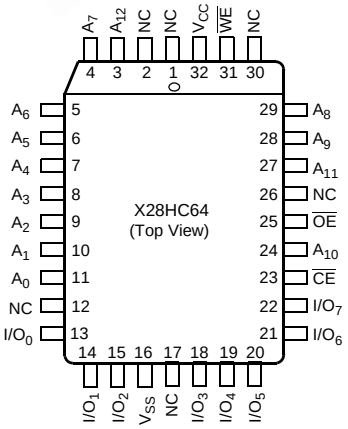
Intersil EEPROMs are designed and tested for applications requiring extended endurance. Inherent data retention is greater than 100 years.

PIN CONFIGURATIONS

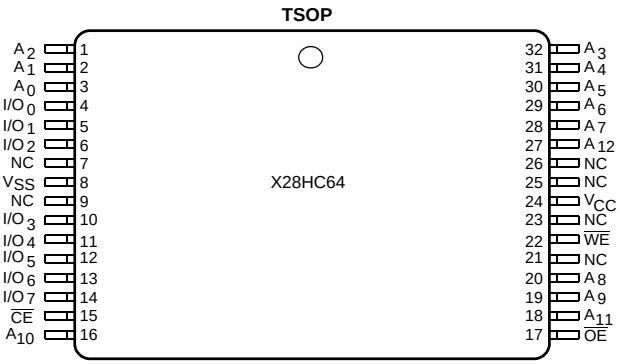
Plastic DIP, Flat Pack, CERDIP, SOIC



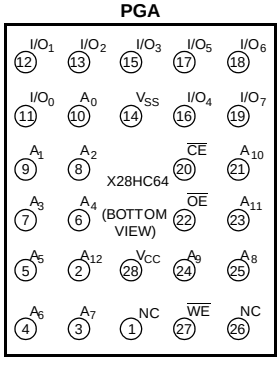
LCC, PLCC



TSOP



PGA



Bottom View

PIN DESCRIPTIONS

Addresses (A_0-A_{12})

The Address inputs select an 8-bit memory location during a read or write operation.

Chip Enable ($\overline{CE}$)

The Chip Enable input must be LOW to enable all read/write operations. When $\overline{CE}$ is HIGH, power consumption is reduced.

Output Enable ($\overline{OE}$)

The Output Enable input controls the data output buffers and is used to initiate read operations.

Data In/Data Out (I/O_0-I/O_7)

Data is written to or read from the X28HC64 through the I/O pins.

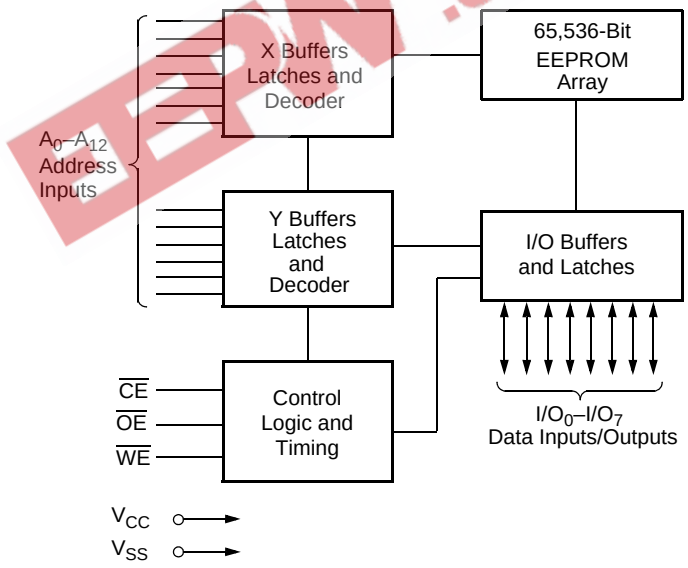
Write Enable ($\overline{WE}$)

The Write Enable input controls the writing of data to the X28HC64.

PIN NAMES

Symbol	Description
A_0-A_{12}	Address Inputs
I/O_0-I/O_7	Data Input/Output
WE	Write Enable
CE	Chip Enable
OE	Output Enable
V_{CC}	+5V
V_{SS}	Ground
NC	No Connect

BLOCK DIAGRAM



DEVICE OPERATION

Read

Read operations are initiated by both $\overline{OE}$ and $\overline{CE}$ LOW. The read operation is terminated by either $\overline{CE}$ or $\overline{OE}$ returning HIGH. This two line control architecture eliminates bus contention in a system environment. The data bus will be in a high impedance state when either $\overline{OE}$ or $\overline{CE}$ is HIGH.

Write

Write operations are initiated when both $\overline{CE}$ and $\overline{WE}$ are LOW and $\overline{OE}$ is HIGH. The X28HC64 supports both a $\overline{CE}$ and $\overline{WE}$ controlled write cycle. That is, the address is latched by the falling edge of either $\overline{CE}$ or $\overline{WE}$, whichever occurs last. Similarly, the data is latched internally by the rising edge of either $\overline{CE}$ or $\overline{WE}$, whichever occurs first. A byte write operation, once initiated, will automatically continue to completion, typically within 2ms.

Page Write Operation

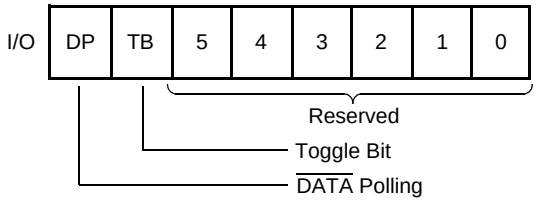
The page write feature of the X28HC64 allows the entire memory to be written in 0.25 seconds. Page write allows two to sixty-four bytes of data to be consecutively written to the X28HC64 prior to the commencement of the internal programming cycle. The host can fetch data from another device within the system during a page write operation (change the source address), but the page address (A_6 through A_{12}) for each subsequent valid write cycle to the part during this operation must be the same as the initial page address.

The page write mode can be initiated during any write operation. Following the initial byte write cycle, the host can write an additional one to sixty-three bytes in the same manner. Each successive byte load cycle, started by the $\overline{WE}$ HIGH to LOW transition, must begin within 100µs of the falling edge of the preceding $\overline{WE}$. If a subsequent $\overline{WE}$ HIGH to LOW transition is not detected within 100µs, the internal automatic programming cycle will commence. There is no page write window limitation. Effectively the page write window is infinitely wide, so long as the host continues to access the device within the byte load cycle time of 100µs.

Write Operation Status Bits

The X28HC64 provides the user two write operation status bits. These can be used to optimize a system write cycle time. The status bits are mapped onto the I/O bus as shown in Figure 1.

Figure 1. Status Bit Assignment



$\overline{DATA}$ Polling (I/O_7)

The X28HC64 features $\overline{DATA}$ Polling as a method to indicate to the host system that the byte write or page write cycle has completed. $\overline{DATA}$ Polling allows a simple bit test operation to determine the status of the X28HC64, eliminating additional interrupt inputs or external hardware. During the internal programming cycle, any attempt to read the last byte written will produce the complement of that data on I/O_7 (i.e. write data = 0xxx xxxx, read data = 1xxx xxxx). Once the programming cycle is complete, I/O_7 will reflect true data.

Toggle Bit (I/O_6)

The X28HC64 also provides another method for determining when the internal write cycle is complete. During the internal programming cycle I/O_6 will toggle from HIGH to LOW and LOW to HIGH on subsequent attempts to read the device. When the internal cycle is complete the toggling will cease and the device will be accessible for additional read or write operations.

$\overline{DATA}$ POLLING I/O_7

Figure 2. $\overline{DATA}$ Polling Bus Sequence

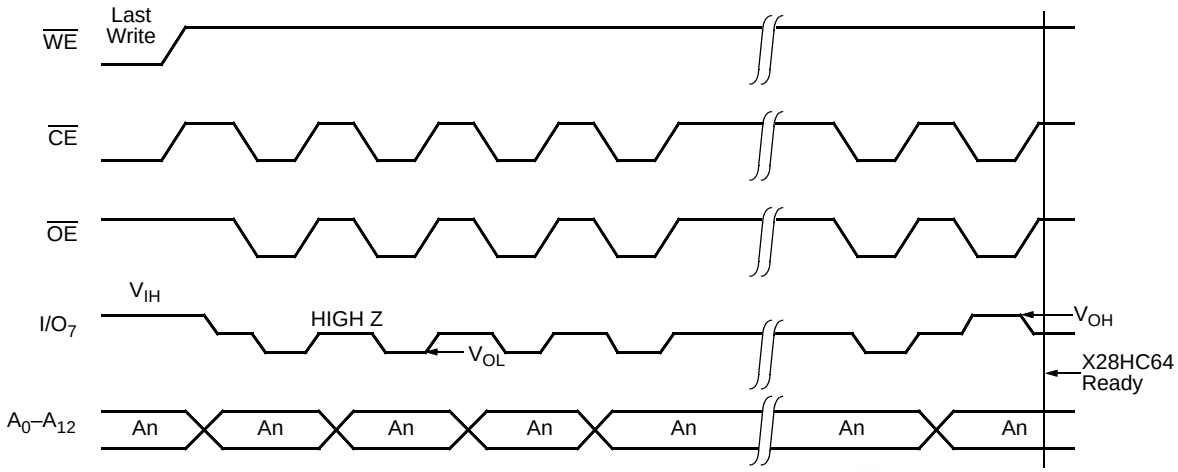
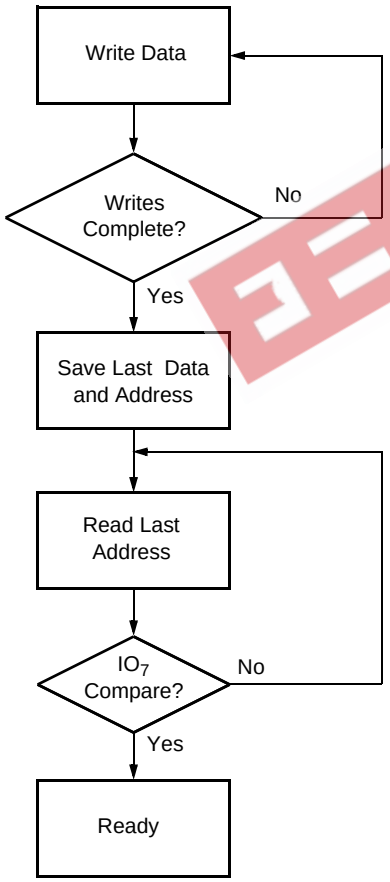


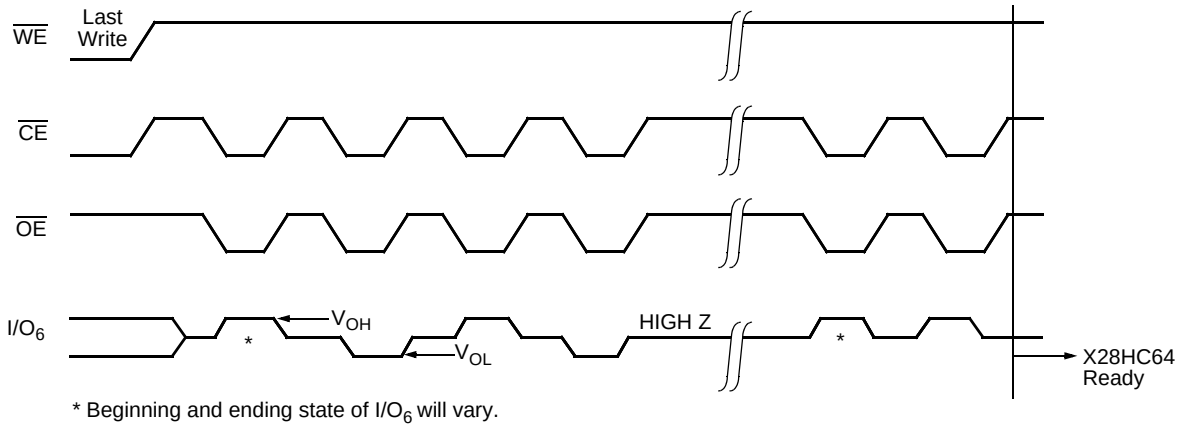
Figure 3. $\overline{DATA}$ Polling Software Flow



$\overline{DATA}$ Polling can effectively reduce the time for writing to the X28HC64. The timing diagram in Figure 2 illustrates the sequence of events on the bus. The software flow diagram in Figure 3 illustrates one method of implementing the routine.

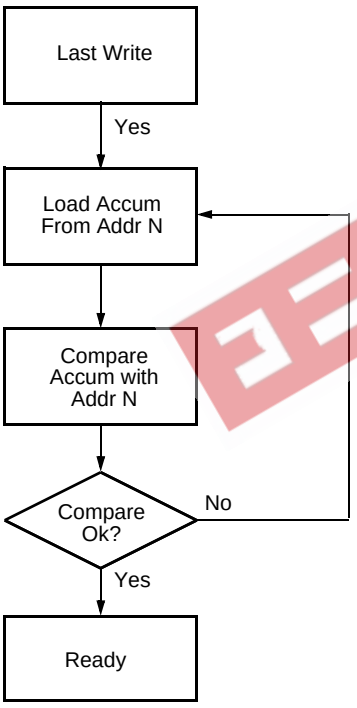
THE TOGGLE BIT I/O_6

Figure 4. Toggle Bit Bus Sequence



* Beginning and ending state of I/O_6 will vary.

Figure 5. Toggle Bit Software Flow



The Toggle Bit can eliminate the chore of saving and fetching the last address and data in order to implement DATA Polling. This can be especially helpful in an array comprised of multiple X28HC64 memories that is frequently updated. Toggle Bit Polling can also provide a method for status checking in multiprocessor applications. The timing diagram in Figure 4 illustrates the sequence of events on the bus. The software flow diagram in Figure 5 illustrates a method for polling the Toggle Bit.

HARDWARE DATA PROTECTION

The X28HC64 provides two hardware features that protect nonvolatile data from inadvertent writes.

– Default V_{CC} Sense—All write functions are inhibited when V_{CC} is 3V typically.
– Write Inhibit—Holding either $\overline{OE}$ LOW, $\overline{WE}$ HIGH, or $\overline{CE}$ HIGH will prevent an inadvertent write cycle during power-up and power-down, maintaining data integrity.

SOFTWARE DATA PROTECTION

The X28HC64 offers a software controlled data protection feature. The X28HC64 is shipped from Intersil with the software data protection NOT ENABLED; that is, the device will be in the standard operating mode. In this mode data should be protected during power-up/-down operations through the use of external circuits. The host would then have open read and write access of the device once V_{CC} was stable.

The X28HC64 can be automatically protected during power-up and power-down without the need for external circuits by employing the software data protection feature. The internal software data protection circuit is enabled after the first write operation utilizing the software algorithm. This circuit is nonvolatile and will remain set for the life of the device, unless the reset command is issued.

Once the software protection is enabled, the X28HC64 is also protected from inadvertent and accidental writes in the powered-up state. That is, the software algorithm must be issued prior to writing additional data to the device.

SOFTWARE ALGORITHM

Selecting the software data protection mode requires the host system to precede data write operations by a series of three write operations to three specific addresses. Refer to Figure 6 and 7 for the sequence. The three-byte sequence opens the page write window, enabling the host to write from one to sixty-four bytes of data. Once the page load cycle has been completed, the device will automatically be returned to the data protected state.

SOFTWARE DATA PROTECTION

Figure 6. Timing Sequence—Byte or Page Write

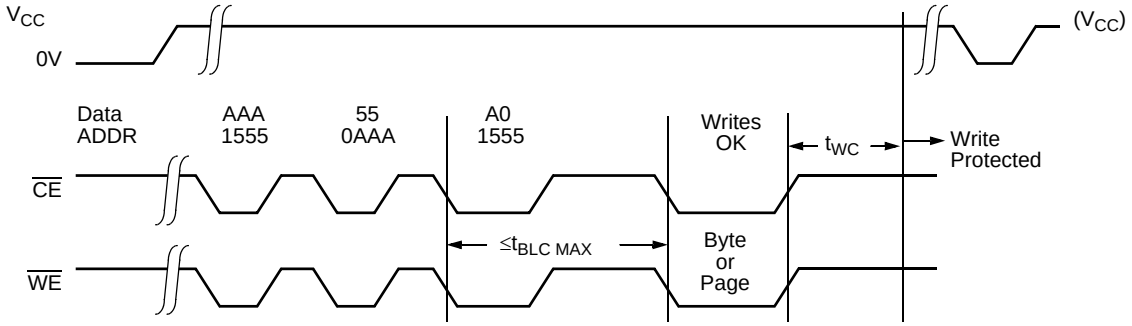
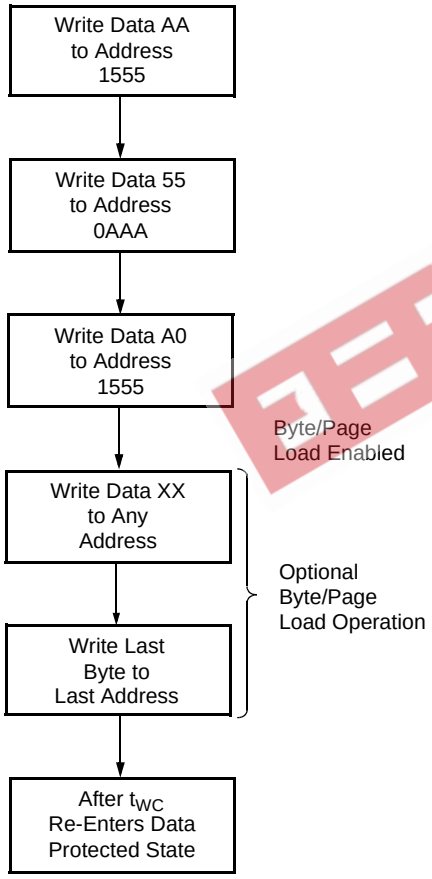


Figure 7. Write Sequence for Software Data Protection



Regardless of whether the device has previously been protected or not, once the software data protection algorithm is used, the X28HC64 will automatically disable further writes unless another command is issued to deactivate it. If no further commands are issued the X28HC64 will be write protected during power-down and after any subsequent power-up.

Note: Once initiated, the sequence of write operations should not be interrupted.

RESETTING SOFTWARE DATA PROTECTION

Figure 8. Reset Software Data Protection Timing Sequence

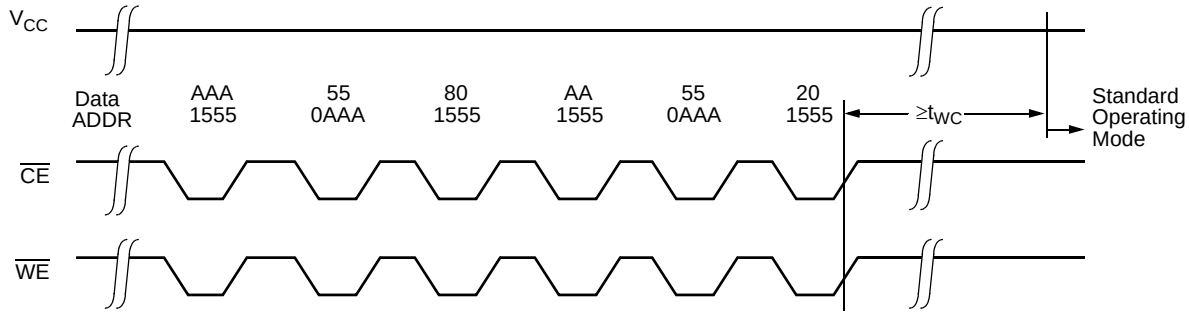
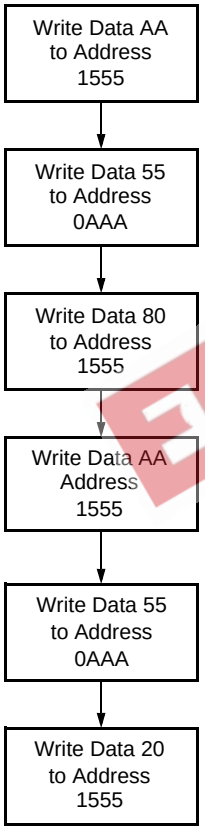


Figure 9. Software Sequence to Deactivate Software Data Protection



In the event the user wants to deactivate the software data protection feature for testing or reprogramming in an EEPROM programmer, the following six step algorithm will reset the internal protection circuit. After t_{WC}, the X28HC64 will be in standard operating mode.

Note: Once initiated, the sequence of write operations should not be interrupted.

SYSTEM CONSIDERATIONS

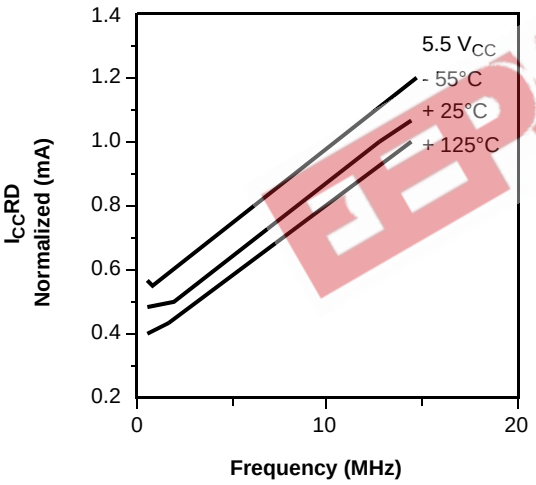
Because the X28HC64 is frequently used in large memory arrays, it is provided with a two-line control architecture for both read and write operations. Proper usage can provide the lowest possible power dissipation, and eliminate the possibility of contention where multiple I/O pins share the same bus.

To gain the most benefit, it is recommended that $\overline{CE}$ be decoded from the address bus, and be used as the primary device selection input. Both $\overline{OE}$ and $\overline{WE}$ would then be common among all devices in the array. For a read operation, this assures that all deselected devices are in their standby mode, and that only the selected device(s) is/are outputting data on the bus.

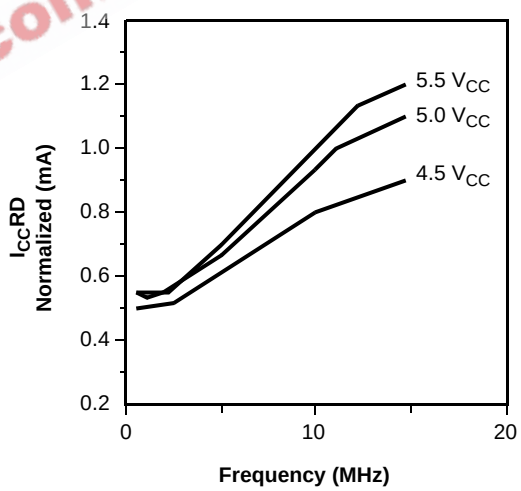
Because the X28HC64 has two power modes, standby and active, proper decoupling of the memory array is of prime concern. Enabling $\overline{CE}$ will cause transient current spikes. The magnitude of these spikes is dependent on the output capacitive loading of the I/Os. Therefore, the larger the array sharing a common bus, the larger the transient spikes. The voltage peaks associated with the current transients can be suppressed by the proper selection and placement of decoupling capacitors. As a minimum, it is recommended that a 0.1µF high frequency ceramic capacitor be used between V_{CC} and V_{SS} at each device. Depending on the size of the array, the value of the capacitor may have to be larger.

In addition, it is recommended that a 4.7µF electrolytic bulk capacitor be placed between V_{CC} and V_{SS} for each eight devices employed in the array. This bulk capacitor is employed to overcome the voltage droop caused by the inductive effects of the PC board traces.

Normalized I_{CC}(RD) by Temperature Over Frequency



Normalized I_{CC}(RD) @ 25% Over the V_{CC} Range and Frequency



ABSOLUTE MAXIMUM RATINGS

Temperature under bias
X28HC64 ..... -10°C to +85°C
X28HC64I, X28HC64M ..... -65°C to +135°C
Storage temperature ..... -65°C to +150°C
Voltage on any pin with
respect to V_{SS} ..... -1V to +7V
D.C. output current 5mA
Lead temperature
(soldering, 10 seconds) ..... 300°C

COMMENT

Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only; functional operation of the device (at these or any other conditions above those indicated in the operational sections of this specification) is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Temperature	Min.	Max.
Commercial	0°C	+70°C
Industrial	-40°C	+85°C
Military	-55°C	+125°C

Supply Voltage	Limits
X28HC64	5V ±10%

D.C. OPERATING CHARACTERISTICS (Over recommended operating conditions unless otherwise specified.)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min.	Typ.(1)	Max.		
I_{CC}	V_{CC} current (active) (TTL inputs)		15	40	mA	$\overline{CE}$ = $\overline{OE}$ = V_{IL}, $\overline{WE}$ = V_{IH}, All I/O’s = open, address inputs = TTL levels @ f = 10 MHz
I_{SB1}	V_{CC} current (standby) (TTL inputs)		1	2	mA	$\overline{CE}$ = V_{IH}, $\overline{OE}$ = V_{IL} All I/O’s = open, other inputs = V_{IH}
I_{SB2}	V_{CC} current (standby) (CMOS inputs)		100	200	µA	$\overline{CE}$ = V_{CC} - 0.3V, $\overline{OE}$ = GND, All I/O’s = open, other inputs = V_{CC} - 0.3V
I_{LI}	Input leakage current			±10	µA	V_{IN} = V_{SS} to V_{CC}
I_{LO}	Output leakage current			±10	µA	V_{OUT} = V_{SS} to V_{CC}, $\overline{CE}$ = V_{IH}
V_{IL}(2)	Input LOW voltage	-1		0.8	V	
V_{IH}(2)	Input HIGH voltage	2		V_{CC} + 1	V	
V_{OL}	Output LOW voltage			0.4	V	I_{OL} = 5mA
V_{OH}	Output HIGH voltage	2.4			V	I_{OH} = -5mA

Notes: (1) Typical values are for T_A = 25°C and nominal supply voltage
(2) V_{IL} min. and V_{IH} max. are for reference only and are not tested.

ENDURANCE AND DATA RETENTION

Parameter	Min.	Max.	Unit
Minimum endurance	100,000		Cycles
Data retention	100		Years

POWER-UP TIMING

Symbol	Parameter	Typ.(1)	Unit
t_{PUR}(3)	Power-up to read operation	100	µs
t_{PUW}(3)	Power-up to write operation	5	ms

CAPACITANCE T_A = +25°C, f = 1MHz, V_{CC} = 5V

Symbol	Parameter	Max.	Unit	Test Conditions
$C_{I/O}$(3)	Input/output capacitance	10	pF	$V_{I/O}$ = 0V
C_{IN}(3)	Input capacitance	6	pF	V_{IN} = 0V

A.C. CONDITIONS OF TEST

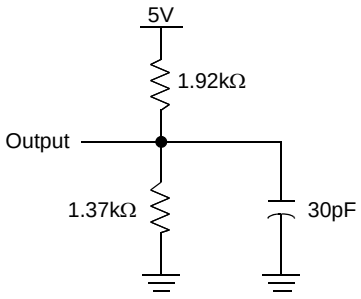
Input pulse levels	0V to 3V
Input rise and fall times	5ns
Input and output timing levels	1.5V

MODE SELECTION

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	Mode	I/O	Power
L	L	H	Read	D_{OUT}	Active
L	H	L	Write	D_{IN}	Active
H	X	X	Standby and write inhibit	High Z	Standby
X	L	X	Write inhibit	—	—
X	X	H	Write inhibit	—	—

Note: (3) This parameter is periodically sampled and not 100% tested.

EQUIVALENT A.C. LOAD CIRCUITS



SYMBOL TABLE

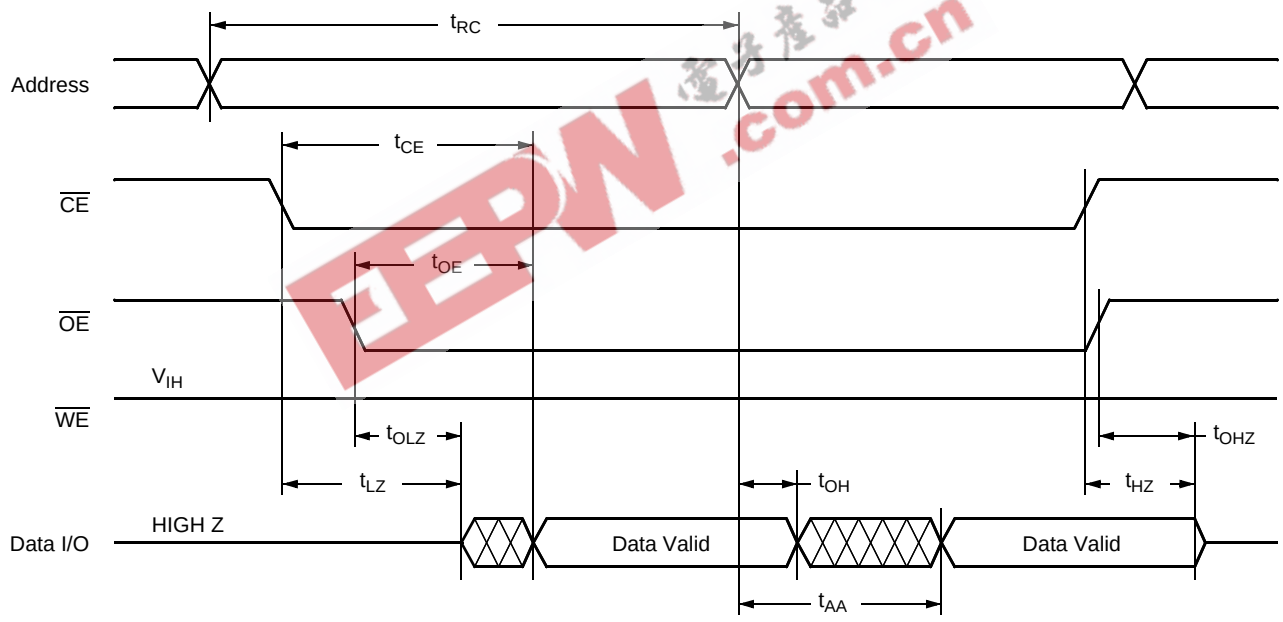
WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from LOW to HIGH	Will change from LOW to HIGH
	May change from HIGH to LOW	Will change from HIGH to LOW
	Don't Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance

A.C. CHARACTERISTICS (Over the recommended operating conditions unless otherwise specified.)

Read Cycle Limits

Symbol	Parameter	X28HC64-70		X28HC64-90		X28HC64-12		Unit
		-55°C to +125°C		-55°C to +125°C		-55°C to +125°C		
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{RC}	Read cycle time	70		90		120		ns
t_{CE}	Chip enable access time		70		90		120	ns
t_{AA}	Address access time		70		90		120	ns
t_{OE}	Output enable access time		35		40		50	ns
t_{LZ}(4)	$\overline{CE}$ LOW to active output	0		0		0		ns
t_{OLZ}(4)	$\overline{OE}$ LOW to active output	0		0		0		ns
t_{HZ}(4)	$\overline{CE}$ HIGH to high Z output		30		30		30	ns
t_{OHZ}(4)	$\overline{OE}$ HIGH to high Z output		30		30		30	ns
t_{OH}	Output hold from address change	0		0		0		ns

Read Cycle

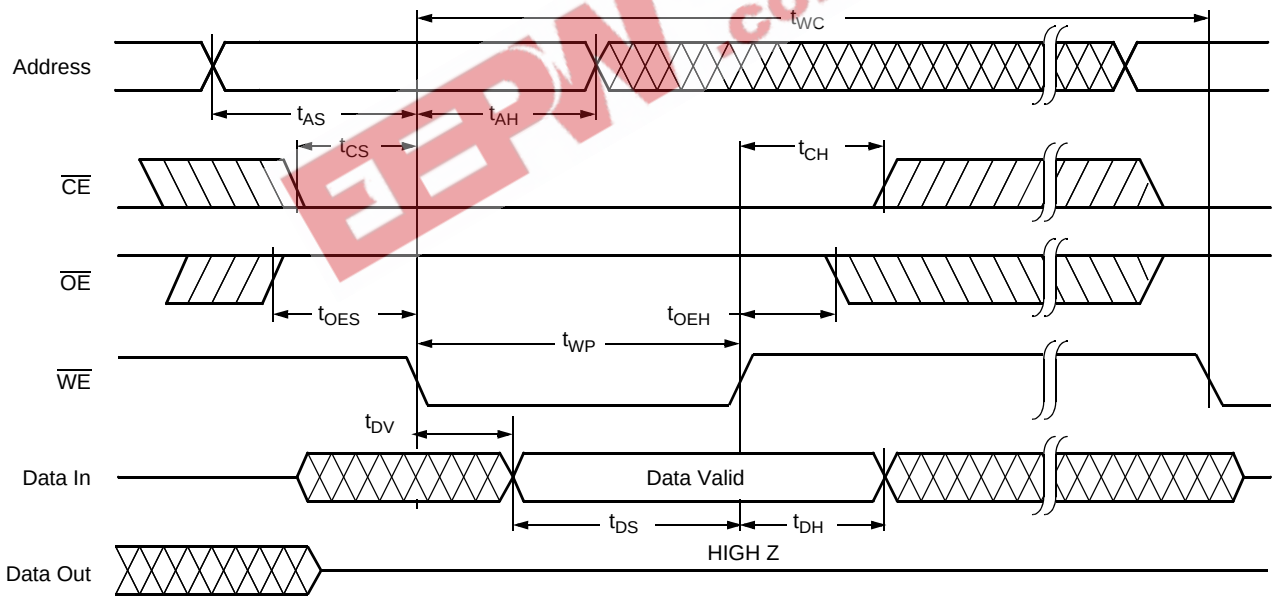


Note: (4) t_{LZ} min., t_{HZ}, t_{OLZ} min., and t_{OHZ} are periodically sampled and not 100% tested. t_{HZ} max. and t_{OHZ} max. are measured from the point when $\overline{CE}$ or $\overline{OE}$ return HIGH (whichever occurs first) to the time when the outputs are no longer driven.

WRITE CYCLE LIMITS

Symbol	Parameter	Min.	Typ.(1)	Max.	Unit
t_{WC}(5)	Write cycle time		2	5	ms
t_{AS}	Address setup time	0			ns
t_{AH}	Address hold time	50			ns
t_{CS}	Write setup time	0			ns
t_{CH}	Write hold time	0			ns
t_{CW}	$\overline{CE}$ pulse width	50			ns
t_{OES}	$\overline{OE}$ High setup time	0			ns
t_{OEH}	$\overline{OE}$ High hold time	0			ns
t_{WP}	$\overline{WE}$ pulse width	50			ns
t_{WPH}(6)	$\overline{WE}$ HIGH recovery	50			ns
t_{DV}(6)	Data valid			1	µs
t_{DS}	Data setup	50			ns
t_{DH}	Data hold	0			ns
t_{DW}(6)	Delay to next write	10			µs
t_{BLC}	Byte load cycle	0.15		100	µs

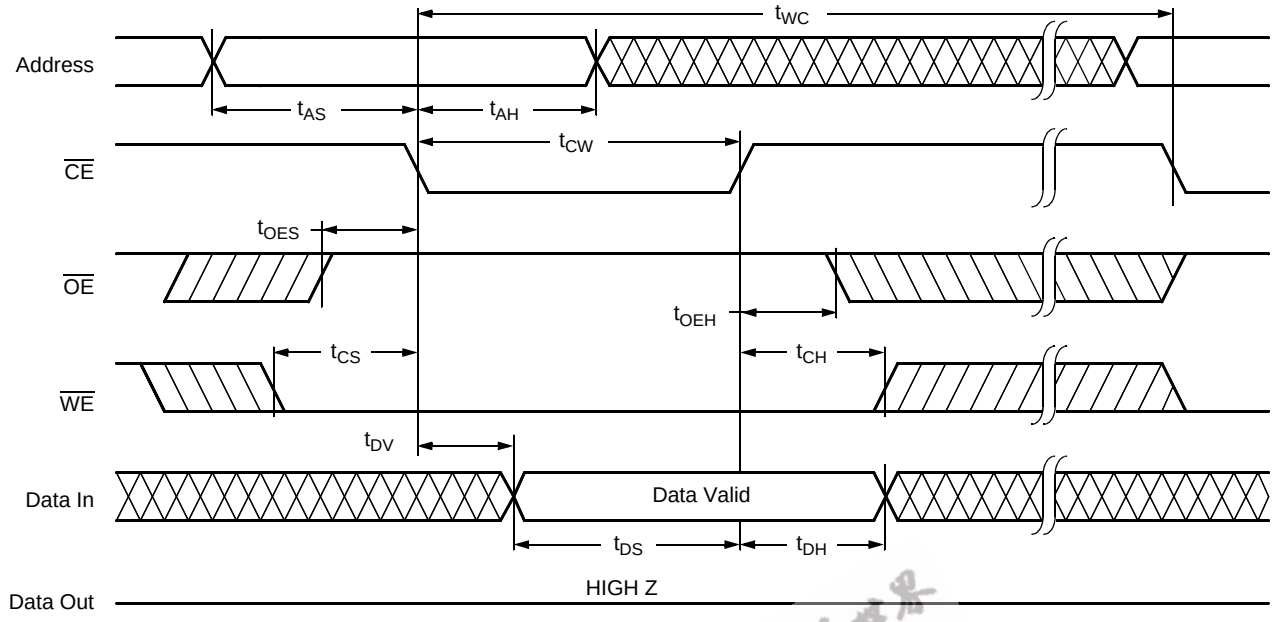
$\overline{WE}$ Controlled Write Cycle



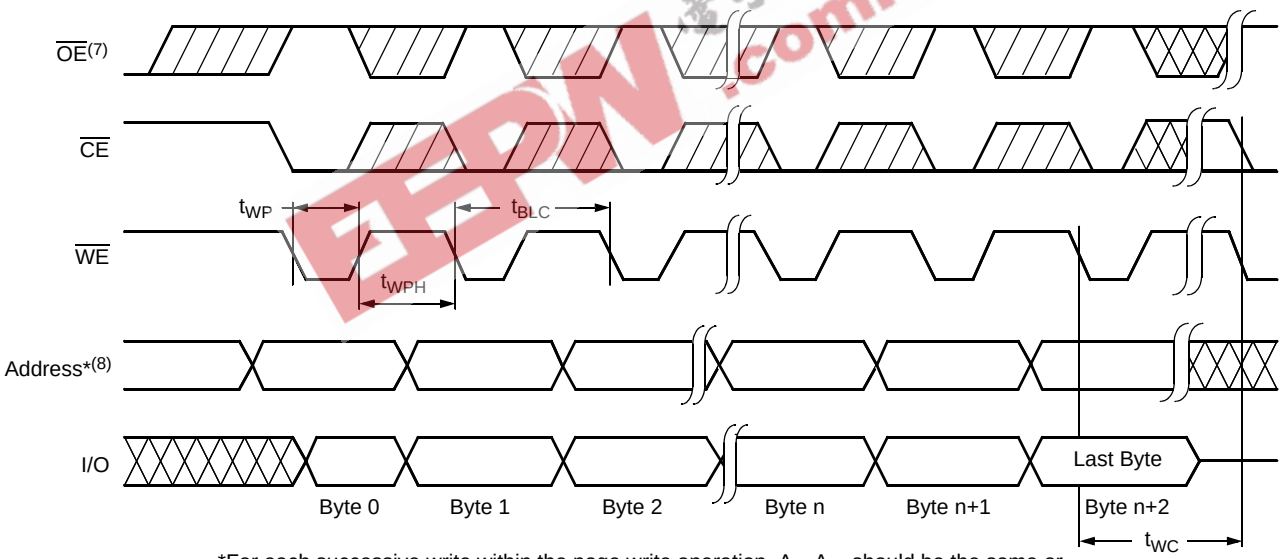
Notes: (5) t_{WC} is the minimum cycle time to be allowed from the system perspective unless polling techniques are used. It is the maximum time the device requires to automatically complete the internal write operation.

(6) t_{WPH} and t_{DW} are periodically sampled and not 100% tested.

$\overline{CE}$ CONTROLLED WRITE CYCLE



Page Write Cycle

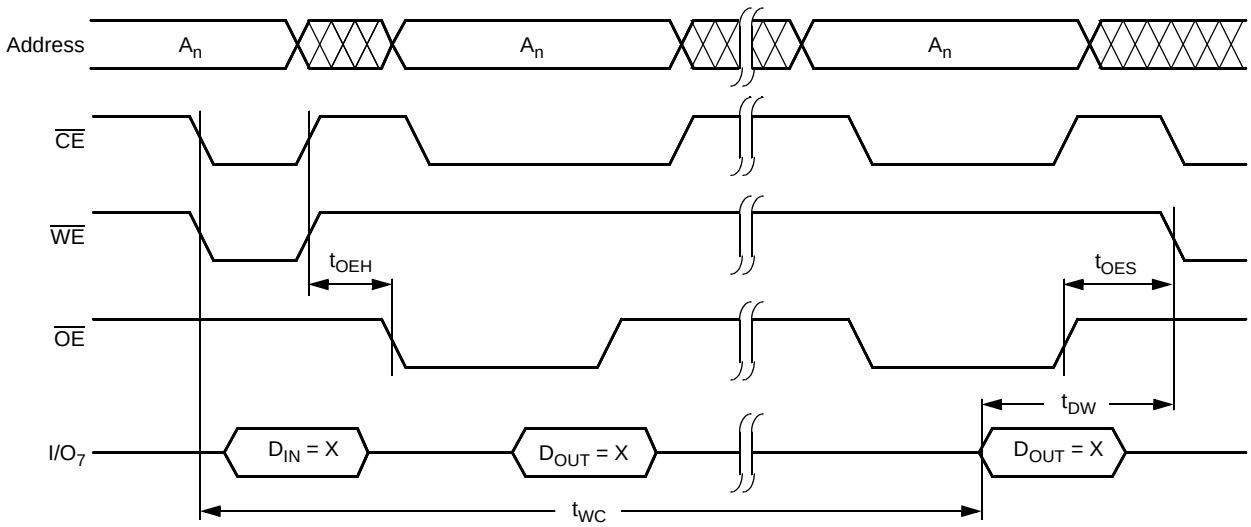


*For each successive write within the page write operation, A_6–A_{12} should be the same or writes to an unknown address could occur.

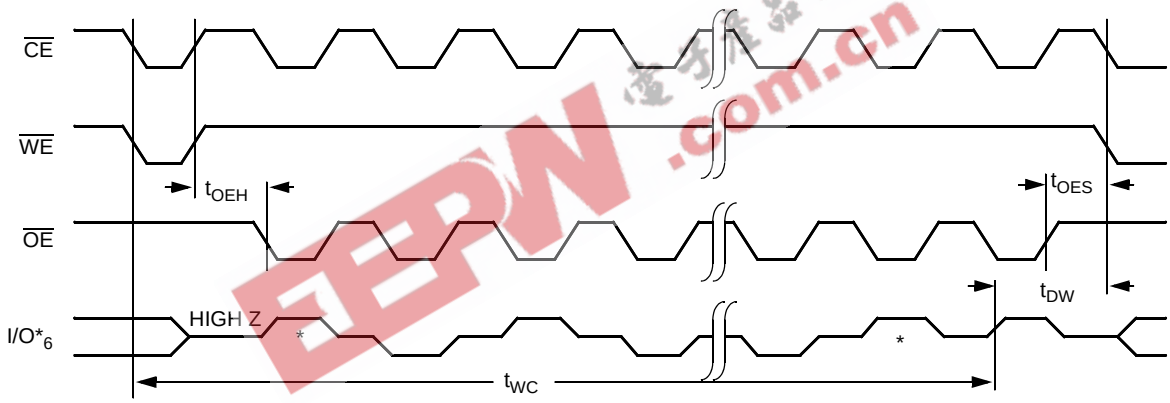
Notes: (7) Between successive byte writes within a page write operation, $\overline{OE}$ can be strobed LOW: e.g. this can be done with $\overline{CE}$ and $\overline{WE}$ HIGH to fetch data from another memory device within the system for the next write; or with $\overline{WE}$ HIGH and $\overline{CE}$ LOW effectively performing a polling operation.

(8) The timings shown above are unique to page write operations. Individual byte load operations within the page write must conform to either the $\overline{CE}$ or $\overline{WE}$ controlled write cycle timing.

$\overline{\text{DATA}}$ Polling Timing Diagram(9)



Toggle Bit Timing Diagram(9)



* I/O_6 beginning and ending state will vary, depending upon actual t_{WC}.

Note: (9) Polling operations are by definition read cycles and are therefore subject to read cycle timings.

Ordering Information