

SCDS240-JUNE 2007

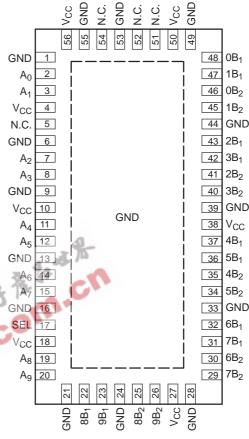
#### **FEATURES**

- Compatible With HDMI v1.2a (Type A) DVI 1.0 High-Speed Digital Interface
  - Wide Bandwidth of Over 1.65 Gbps (Bandwidth 1.9 Gbps Typ)
  - 165-MHz Speed Operation
  - Serial Data Stream at 10× Pixel Clock Rate
  - Supports All Video Formats up to 1080p and SXGA (1280 × 1024 at 75 Hz)
  - Total Raw Capacity 4.95 Gbps (Single Link)
  - HDCP Compatible
- Low Crosstalk (X<sub>TALK</sub> = -37 dB Typ)
- Low Bit-to-Bit Skew (t<sub>sk(o)</sub> = 0.1 ns Max)
- Low and Flat ON-State Resistance (r<sub>on</sub> = 4 Ω Typ, r<sub>on(flat)</sub> = 0.5 Ω Typ)
- Low Input/Output Capacitance (C<sub>ON</sub> = 8 pF Typ)
- Rail-to-Rail Switching on Data I/O Ports (0 to 3.6 V)
- V<sub>CC</sub> Operating Range From 3 V to 3.6 V
- I<sub>off</sub> Supports Partial-Power-Down Mode Operation (V<sub>CC</sub> = V<sub>IN</sub> = 0 V)
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Performance Tested Per JESD 22
  - 14000-V Human-Body Model (A114-B, Class II)

# **APPLICATIONS**

- DVI/HDMI Signal Switching
- Differential DVI, HDMI Signal Multiplexing for Audio/Video Receivers and High-Definition Televisions (HDTVs)

# TQFN PACKAGE (TOP VIEW)



N.C. - No internal connection

# **DESCRIPTION/ORDERING INFORMATION**

The TS3DV520E is a 20-bit to 10-bit multiplexer/demultiplexer digital video switch with a single select (SEL) input. SEL controls the data path of the multiplexer/demultiplexer. The device provides five differential channels for digital video signal switching.

This device provides low and flat ON-state resistance (r<sub>on</sub>) and excellent ON-state resistance match. Low input/output capacitance, high bandwidth, low skew, and low crosstalk among channels make this device suitable for various digital video applications, such as DVI and HDMI.

This device is specified for partial-power-down applications using I<sub>off</sub>. The I<sub>off</sub> feature ensures that damaging current will not backflow through the device when it is powered down. The device has isolation during power off.

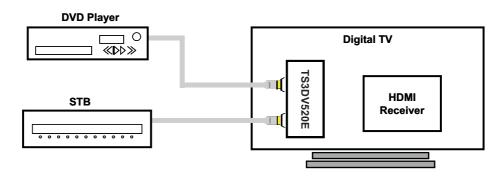
Voltage on the SEL pin should be less or equal to  $V_{CC}$ , even in the power-down mode ( $V_{CC} = 0 \text{ V}$ ).



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



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# **ORDERING INFORMATION**

T <sub>A</sub>	PACKAGE <sup>(1)(2)</sup>		ORDERABLE PART NUMBER	TOP-SIDE MARKING	
–40°C to 85°C	TQFN	Reel of 2000	TS3DV520ERHURG4	SD520E	

- (1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.
- For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com. FUNCTION TABLE

INPUT SEL	INPUT/OUTPUT An	FUNCTION
L	nB <sub>1</sub>	$A_n = nB_1$ $nB_2$ high-impedance mode
Н	nB <sub>2</sub>	$A_n = nB_2$ $nB_1$ high-impedance mode

# **PIN DESCRIPTION**

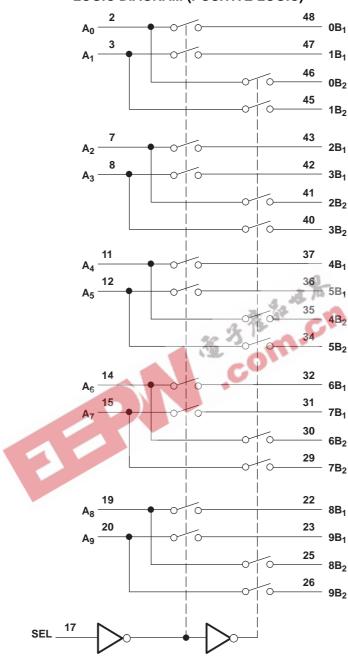
NAME	DESCRIPTION
An	Data I/O
nB <sub>m</sub>	Data I/O
SEL	Select input

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# **LOGIC DIAGRAM (POSITIVE LOGIC)**





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# Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

				MIN	MAX	UNIT
$V_{CC}$	Supply voltage range				4.6	V
V <sub>IN</sub>	Control input voltage range (2)(3)			-0.5	V <sub>CC</sub> + 0.5	V
V <sub>I/O</sub>	Switch I/O voltage range <sup>(2)(3)(4)</sup>			-0.5	7	V
I <sub>IK</sub>	Control input clamp current	V <sub>IN</sub> < 0			-50	mA
I <sub>I/OK</sub>	I/O port clamp current	V <sub>I/O</sub> < 0			-50	mA
I <sub>I/O</sub>	ON-state switch current <sup>(5)</sup>				±128	mA
	Continuous current through V <sub>CC</sub> or GND				±100	mA
$\theta_{JA}$	Package thermal impedance (6)				31.8	°C/W
T <sub>stg</sub>	Storage temperature range			-65	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltages are with respect to ground, unless otherwise specified.
- (3) The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
- (4) V<sub>I</sub> and V<sub>O</sub> are used to denote specific conditions for V<sub>I/O</sub>.
- (5) I<sub>I</sub> and I<sub>O</sub> are used to denote specific conditions for I<sub>I/O</sub>.
- (6) The package thermal impedance is calculated in accordance with JESD 51-7.

# Recommended Operating Conditions<sup>(1)</sup>

		4	135	MIN	MAX	UNIT
$V_{CC}$	Supply voltage		Co	3	3.6	V
$V_{IH}$	High-level control input voltage (SEL)	`		2	$V_{CC}$	V
$V_{IL}$	Low-level control input voltage (SEL)	1		0	0.8	V
$V_{I/O}$	Input/output voltage			0	5.5	V
$T_A$	Operating free-air temperature			-40	85	°C

All unused control inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

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# Electrical Characteristics(1)

for high-frequency switching over recommended operating free-air temperature range,  $V_{CC}$  = 3.3 V  $\pm$  0.3 V (unless otherwise noted)

PARAMETER			TEST CO	NDITIONS		MIN	TYP <sup>(2)</sup>	MAX	UNIT
V <sub>IK</sub>	SEL	$V_{CC} = 3.6 \text{ V},$	I <sub>IN</sub> = -18 mA				-0.7	-1.2	V
I <sub>IH</sub>	SEL	$V_{CC} = 3.6 \text{ V},$	$V_{IN} = V_{CC}$					±1	μA
I <sub>IL</sub>	SEL	$V_{CC} = 3.6 \text{ V},$	$V_{IN} = GND$					±1	μA
I <sub>off</sub>		$V_{CC} = 0$ ,	$V_0 = 0 \text{ to } 3.6 \text{ V},$	$V_I = 0$ ,	$V_{IN} = 0 V$			1	μA
I <sub>CC</sub>		$V_{CC} = 3.6 \text{ V},$	$I_{I/O} = 0$ ,	Switch ON or OFF			250	600	μΑ
C <sub>IN</sub>	SEL	f = 1 MHz,	$V_{IN} = 0$				2	2.5	pF
C <sub>OFF</sub>	B port	$V_I = 0$ ,	f = 1 MHz,	Outputs open,	Switch OFF		3	4	pF
C <sub>ON</sub>		$V_I = 0$ ,	f = 1 MHz,	Outputs open,	Switch ON		9	9.8	pF
r <sub>on</sub>		$V_{CC} = 3 V$ ,	$1.5 \text{ V} \leq \text{V}_{\text{I}} \leq \text{V}_{\text{CC}},$	$I_O = -40 \text{ mA}$			4	8	Ω
r <sub>on(flat)</sub> (3)		$V_{CC} = 3 V$ ,	$V_I = 1.5 \text{ V} \text{ and } V_{CC}$	$I_O = -40 \text{ mA}$			0.7		Ω
$\Delta r_{on}^{(4)}$		$V_{CC} = 3 V$ ,	$1.5 \text{ V} \leq \text{V}_{\text{I}} \leq \text{V}_{\text{CC}},$	$I_O = -40 \text{ mA}$			0.2	1.2	Ω

- $V_{I},\,V_{O},\,I_{I},\,$  and  $I_{O}$  refer to I/O pins.  $V_{IN}$  refers to the control inputs. All typical values are at  $V_{CC}$  = 3.3 V (unless otherwise noted),  $T_{A}$  = 25°C.  $r_{on(flat)}$  is the difference of  $r_{on}$  in a given channel at specified voltages.  $\Delta r_{on}$  is the difference of  $r_{on}$  from center (A4, A5) ports to any other port.

# **Switching Characteristics**

over recommended operating free-air temperature range,  $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$ ,  $R_{L}$ (unless otherwise noted) (see Figure 5 and Figure 6)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	TYP <sup>(1)</sup>	MAX	UNIT
t <sub>pd</sub> <sup>(2)</sup>	A or B	B or A		0.25		ns
t <sub>PZH</sub> , t <sub>PZL</sub>	SEL	A or B	0.5		15	ns
t <sub>PHZ</sub> , t <sub>PLZ</sub>	SEL	A or B	0.5		9	ns
t <sub>sk(o)</sub> (3)	A or B	B or A		0.05	0.1	ns
t <sub>sk(p)</sub> (4)				0.05	0.1	ns

- All typical values are at  $V_{CC}$  = 3.3 V (unless otherwise noted),  $T_A$  = 25°C.
- The propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance when driven by an ideal voltage source (zero output impedance).
- Output skew between center port (A<sub>4</sub> to A<sub>5</sub>) to any other port
- Skew between opposite transitions of the same output in a given device |t<sub>PHL</sub> t<sub>PLH</sub>|

# **Dynamic Characteristics**

over recommended operating free-air temperature range,  $V_{CC}$  = 3.3 V  $\pm$  0.3 V (unless otherwise noted)

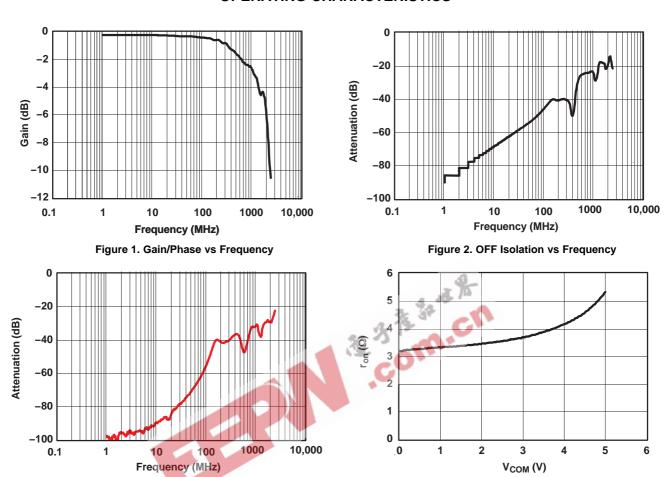
PARAMETER		TEST CONDITIONS 1					
X <sub>TALK</sub>	$R_L = 100 \Omega$ ,	f = 250 MHz,	See Figure 8	-3	7 dB		
O <sub>IRR</sub>	$R_L = 100 \Omega$ ,	f = 250 MHz,	See Figure 9	-3	7 dB		
BW	$R_L = 100 \Omega$ ,	See Figure 7		95	MHz		

(1) All typical values are at  $V_{CC}$  = 3.3 V (unless otherwise noted),  $T_A$  = 25°C.

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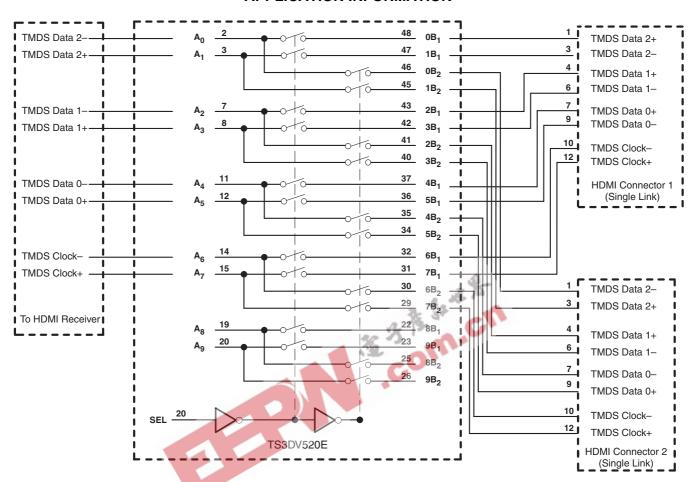


# **OPERATING CHARACTERISTICS**

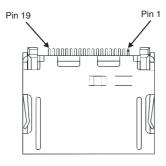


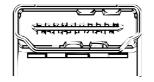
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# **APPLICATION INFORMATION**



#### Typical HDMI Connector





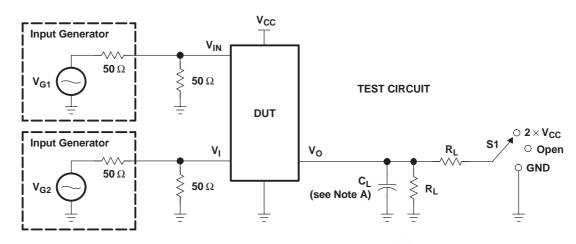
The TS3DV520E can be used to switch between two digital video ports.

Pin	Signal Assignment
1	TMDS Data 2+
2	TMDS Data 2 Shield
3	TMDS Data 2-
4	TMDS Data 1+
5	TMDS Data 1 Shield
6	TMDS Data 1-
7	TMDS Data 0+
8	TMDS Data 0 Shield
9	TMDS Data 0-
10	TMDS Clock+
11	TMDS Clock Shield
12	TMDS Clock-
13	CEC
14	Reserved (N.C. on device)
15	SCL
16	SDA
17	DDC/CEC Ground
18	5 V Power
19	Hot Plug Detect

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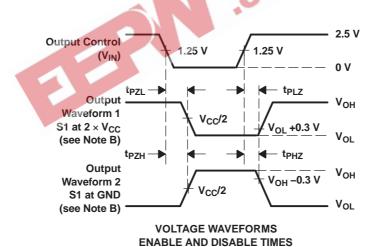


# PARAMETER MEASUREMENT INFORMATION (Enable and Disable Times)



TEST	V <sub>CC</sub>	S1	$R_{L}$	V <sub>i</sub>	CL	${f V}_{\!\Delta}$
t <sub>PLZ</sub> /t <sub>PZL</sub>	3.3 V $\pm$ 0.3 V	2×V <sub>CC</sub>	200 Ω	GND	10 pF	0.3 V
t <sub>PHZ</sub> /t <sub>PZH</sub>	3.3 V ± 0.3 V	GND	200 Ω	V <sub>CC</sub>	10 pF	0.3 V

3



NOTES: A.  $C_L$  includes probe and jig capacitance.

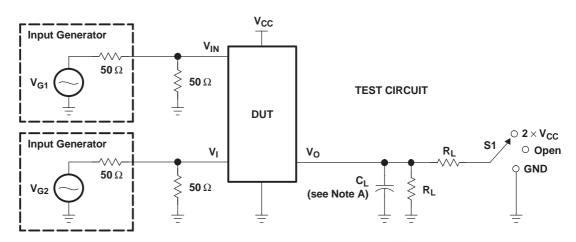
- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_O$  = 50  $\Omega$ ,  $t_r \leq$  2.5 ns.  $t_f \leq$  2.5 ns.
- D. The outputs are measured one at a time, with one transition per measurement.
- E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
- F. t<sub>PZL</sub> and t<sub>PZH</sub> are the same as t<sub>en</sub>.

Figure 5. Test Circuit and Voltage Waveforms

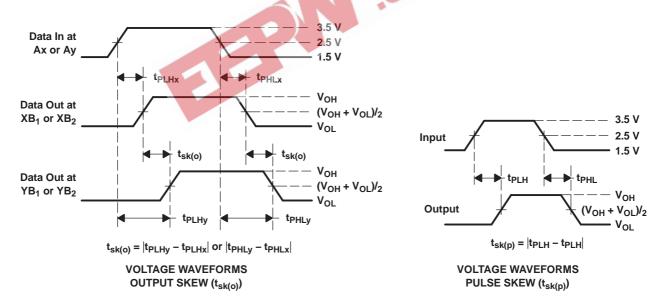
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# PARAMETER MEASUREMENT INFORMATION (Skew)



TEST	V <sub>CC</sub>	S1	$R_L$	V <sub>I</sub> C <sub>L</sub>	$V_{\Delta}$
t <sub>sk(o)</sub>	3.3 V ± 0.3 V	Open	200 Ω	V <sub>CC</sub> or GND 10 pF	
t <sub>sk(p)</sub>	3.3 V ± 0.3 V	Open	200 Ω	V <sub>CC</sub> or GND 10 pF	



NOTES: A.  $C_L$  includes probe and jig capacitance.

- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_O = 50 \Omega$ ,  $t_r \leq$  2.5 ns,  $t_f \leq$  2.5 ns.
- D. The outputs are measured one at a time, with one transition per measurement.

Figure 6. Test Circuit and Voltage Waveforms



# PARAMETER MEASUREMENT INFORMATION

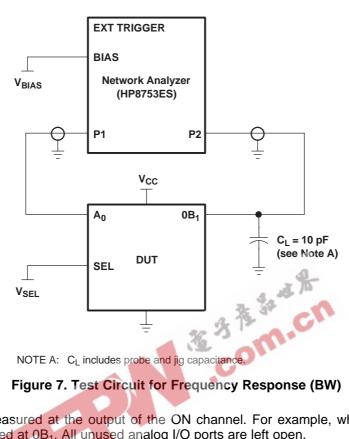


Figure 7. Test Circuit for Frequency Response (BW)

Frequency response is measured at the output of the ON channel. For example, when  $V_{SEL} = 0$  and  $A_0$  is the input, the output is measured at  $0B_1$ . All unused analog I/O ports are left open.

# HP8753ES setup

Average = 4

RBW = 3 kHz

 $V_{BIAS} = 0.35 \text{ V}$ 

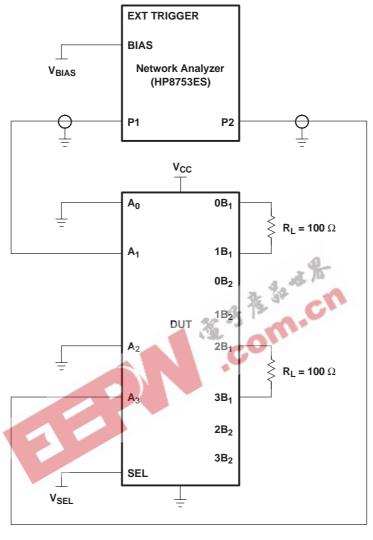
ST = 2 s

P1 = 0 dBM



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# PARAMETER MEASUREMENT INFORMATION



NOTES: A.  $C_L$  includes probe and jig capacitance.

B. A 50- $\Omega$  termination resistor is needed to match the loading of the network analyzer.

Figure 8. Test Circuit for Crosstalk (X<sub>TALK</sub>)

Crosstalk is measured at the output of the nonadjacent ON channel. For example, when  $V_{SEL}=0$  and  $A_0$  is the input, the output is measured at  $1B_1$ . All unused analog input (A) ports are connected to GND, and output (B) ports are connected to GND through  $50-\Omega$  pulldown resistors.

# HP8753ES setup

Average = 4

RBW = 3 kHz

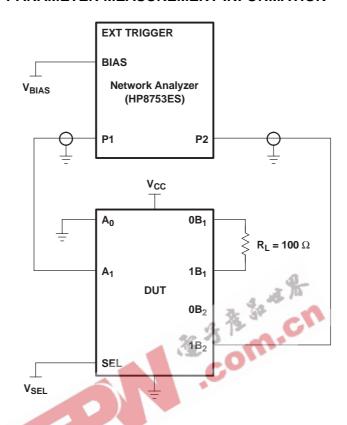
 $V_{BIAS} = 0.35 \text{ V}$ 

ST = 2 s

P1 = 0 dBM



# PARAMETER MEASUREMENT INFORMATION



NOTES: A. C<sub>L</sub> includes probe and jig capacitance.

B. A  $50-\Omega$  termination resistor is needed to match the loading of the network analyzer.

Figure 9. Test Circuit for OFF Isolation (OIRR)

OFF isolation is measured at the output of the OFF channel. For example, when  $V_{SEL} = V_{CC}$  and  $A_0$  is the input, the output is measured at  $0B_2$ . All unused analog input (A) ports are left open, and output (B) ports are connected to GND through  $50-\Omega$  pulldown resistors.

#### HP8753ES setup

Average = 4

RBW = 3 kHz

 $V_{BIAS} = 0.35 \text{ V}$ 

ST = 2

P1 = 0 dBM



# PACKAGE OPTION ADDENDUM

20-Mar-2008

# **PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins F	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
TS3DV520ERHURG4	ACTIVE	WQFN	RHU	56	2000	Green (RoHS &	CU NIPDAU	Level-1-260C-UNLIM
						no Sb/Br)		

<sup>(1)</sup> The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <a href="http://www.ti.com/productcontent">http://www.ti.com/productcontent</a> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

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**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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 $-56 \times \frac{0,30}{0,18}$ 

0,10 M C A B 0,05 (M) C

4206903/A 04/2005

# PLASTIC QUAD FLATPACK RHU (R-PQFP-N56) 11,15 A 10,85 В 48 29 49 28 5,15 4.85 Pin 1 Index Area Top And Bottom ◬ 21 0,80 0,20 Nominal 0,70 Lead Frame Seating Plane С 0,00 0,08 C Seating Height 0,50 0,50 Pin 1 Identifier +0,10 3,50 2,40 -0,15

Notes:

Exposed Thermal Pad

A

- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
- This drawing is subject to change without notice.
- C. QFN (Quad Flatpack No-Lead) package configuration.
- Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated.
- The Pin 1 identifiers are either a molded, marked, or metal feature.

  The package thermal pad must be soldered to the board for thermal and mechanical performance.
- F. JEDEC MO-220 package registration is pending.



8,40 <sup>+0,10</sup> -0,15

Bottom View

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