

54173/DM54173/DM74173 TRI-STATE® Quad D Registers

General Description

These four-bit registers contain D-type flip-flops with totem-pole TRI-STATE outputs, capable of driving highly capacitive or low-impedance loads. The high-impedance state and increased high-logic-level drive provide these flip-flops with the capability of driving the bus lines in a bus-organized system without need for interface or pull-up components.

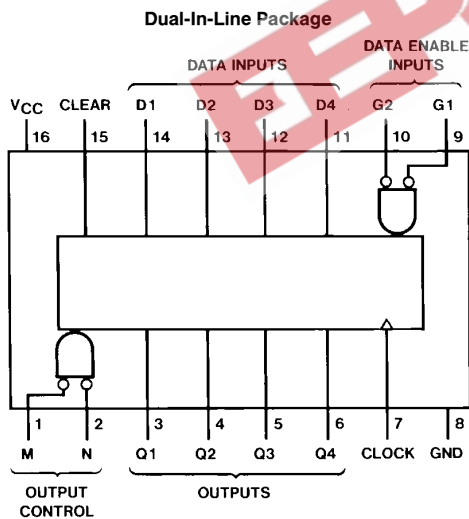
Gated enable inputs are provided for controlling the entry of data into the flip-flops. When both data-enable inputs are low, data at the D inputs are loaded into their respective flip-flops on the next positive transition of the buffered clock input. Gate output control inputs are also provided. When both are low, the normal logic states of the four outputs are available for driving the loads or bus lines. The outputs are disabled independently from the level of the clock by a high logic level at either output control input. The outputs then present a high impedance and neither load nor drive the bus line. Detailed operation is given in the function table.

To minimize the possibility that two outputs will attempt to take a common bus to opposite logic levels, the output control circuitry is designed so that the average output disable times are shorter than the average output enable times.

Features

- TRI-STATE outputs interface directly with system bus
- Gated output control lines for enabling or disabling the outputs
- Fully independent clock eliminates restrictions for operating in one of two modes:
 - Parallel load
 - Do nothing (hold)
- For application as bus buffer registers
- Typical propagation delay 18 ns
- Typical frequency 30 MHz
- Typical power dissipation 250 mW
- Alternate Military/Aerospace device (54173) is available. Contact a National Semiconductor Sales Office/Distributor for specifications.

Connection Diagram



Function Table

Clear	Clock	Inputs			Output Q
		Data Enable		Data D	
		G1	G2		
H	X	X	X	X	L
L	L	X	X	X	Q ₀
L	↑	H	X	X	Q ₀
L	↑	X	H	X	Q ₀
L	↑	L	L	L	L
L	↑	L	L	H	H

When either M or N (or both) is (are) high the output is disabled to the high-impedance state; however, sequential operation of the flip-flops is not affected.

H = high level (steady state)

L = low level (steady state)

↑ = low-to-high level transition

X = don't care (any input including transitions)

Q₀ = the level of Q before the indicated steady state input conditions were established

TL/F/6556-1

Order Number 54173DMQB, 54173FMQB,
DM54173J, DM54173W or DM74173N
See NS Package Number J16A, N16E or W16A

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Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	5.5V
Operating Free Air Temperature Range	
DM54 and 54	–55°C to +125°C
DM74	0°C to +70°C
Storage Temperature Range	–65°C to +150°C

Note: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Recommended Operating Conditions

Symbol	Parameter		DM54173			DM74173			Units
			Min	Nom	Max	Min	Nom	Max	
V _{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V _{IH}	High Level Input Voltage		2			2			V
V _{IL}	Low Level Input Voltage				0.8			0.8	V
I _{OH}	High Level Output Current				–2			–5.2	mA
I _{OL}	Low Level Output Current				16			16	mA
f _{CLK}	Clock Frequency (Note 4)		0		25	0		25	MHz
t _w	Pulse Width (Note 4)	Clock	20			20			ns
		Clear	20			20			
t _{SU}	Setup Time (Note 4)	Enable	17			17			ns
		Data	10			10			
t _H	Hold Time (Note 4)	Enable	2			2			ns
		Data	10			10			
t _{REL}	Clear Release Time (Note 4)		10			10			ns
T _A	Free Air Operating Temperature		–55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 1)	Max	Units
V _I	Input Clamp Voltage	V _{CC} = Min, I _I = –12 mA			–1.5	V
V _{OH}	High Level Output Voltage	V _{CC} = Min, I _{OH} = Max V _{IL} = Max, V _{IH} = Min	2.4			V
V _{OL}	Low Level Output Voltage	V _{CC} = Min, I _{OL} = Max V _{IH} = Min, V _{IL} = Max			0.4	V
I _I	Input Current @ Max Input Voltage	V _{CC} = Max, V _I = 5.5V			1	mA
I _{IH}	High Level Input Current	V _{CC} = Max, V _I = 2.4V			40	μA
I _{IL}	Low Level Input Current	V _{CC} = Max, V _I = 0.4V			–1.6	mA
I _{OZH}	Off-State Output Current with High Level Output Voltage Applied	V _{CC} = Max, V _O = 2.4V V _{IH} = Min, V _{IL} = Max			40	μA
I _{OZL}	Off-State Output Current with Low Level Output Voltage Applied	V _{CC} = Max, V _O = 0.4V V _{IH} = Min, V _{IL} = Max			–40	μA
I _{OS}	Short Circuit Output Current	V _{CC} = Max (Note 2)	DM54	–30	–70	mA
			DM74	–30	–70	
I _{CC}	Supply Current	V _{CC} = Max (Note 3)		50	72	mA

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

Note 3: I_{CC} is measured with all outputs open, CLEAR grounded after a momentary connection to 4.5V; N, G1, G2 and all DATA inputs grounded; and the CLOCK input and M input at 4.5V.

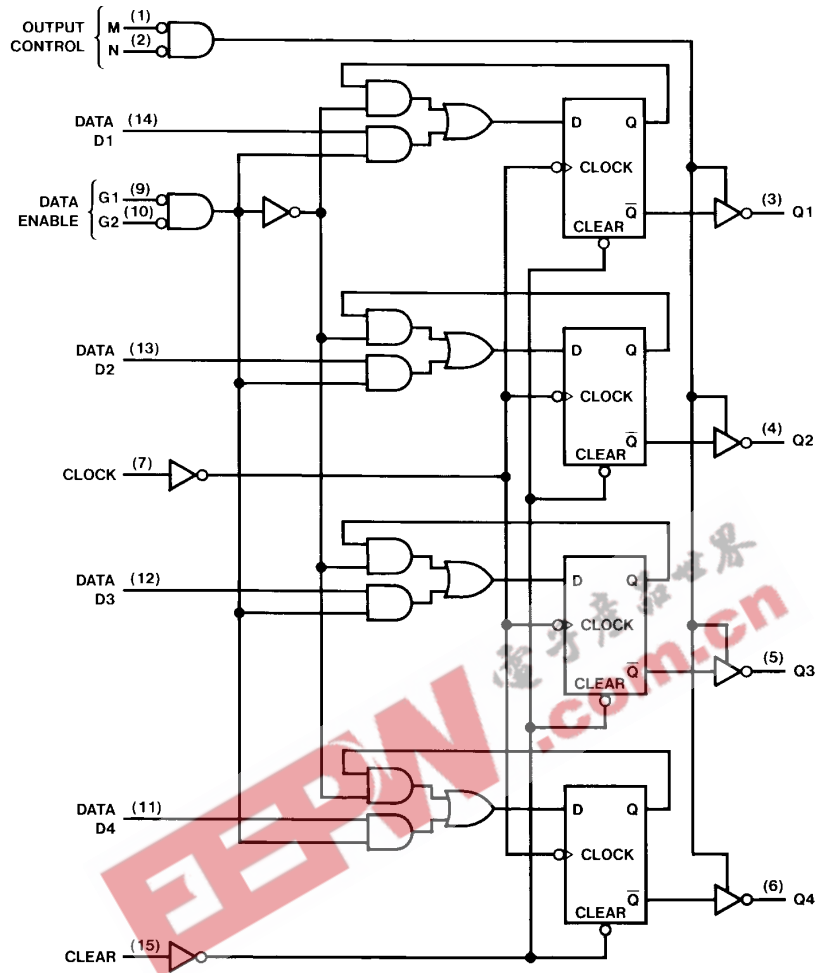
Note 4: T_A = 25°C and V_{CC} = 5V.

Switching Characteristics at $V_{CC} = 5V$ and $T_A = 25^\circ C$ (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	From (Input) To (Output)	$R_L = 400\Omega$				Units
			$C_L = 5\text{ pF}$		$C_L = 50\text{ pF}$		
			Min	Max	Min	Max	
f_{MAX}	Maximum Clock Frequency				25		MHz
t_{PLH}	Propagation Delay Time Low to High Level Output	Clock to Output				25	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clock to Output				28	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	Clear to Output				27	ns
t_{PZH}	Output Enable Time to High Level Output	Output Control to Q			7	30	ns
t_{PZL}	Output Enable Time to Low Level Output	Output Control to Q			7	30	ns
t_{PHZ}	Output Disable Time from High Level Output	Output Control to Q	3	14			ns
t_{PLZ}	Output Disable Time from Low Level Output	Output Control to Q	3	20			ns

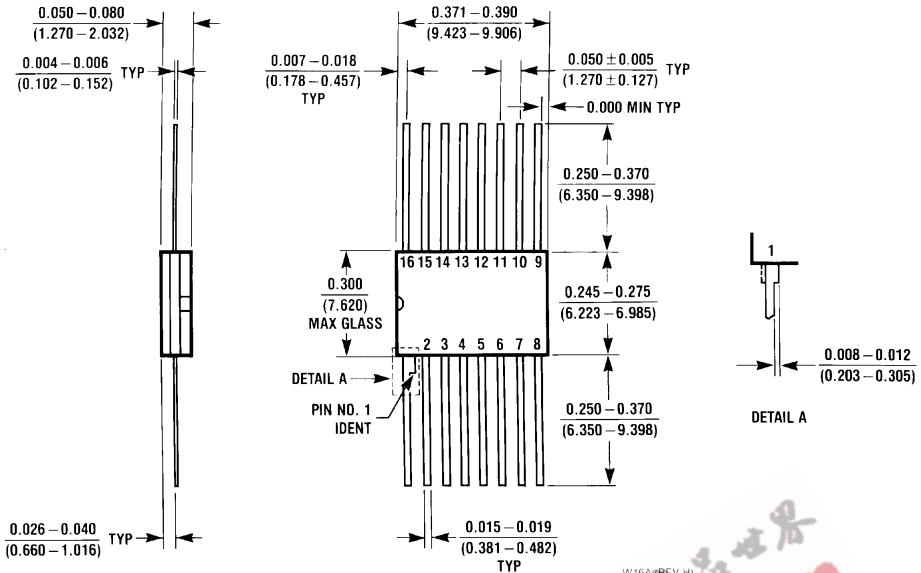
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Logic Diagram

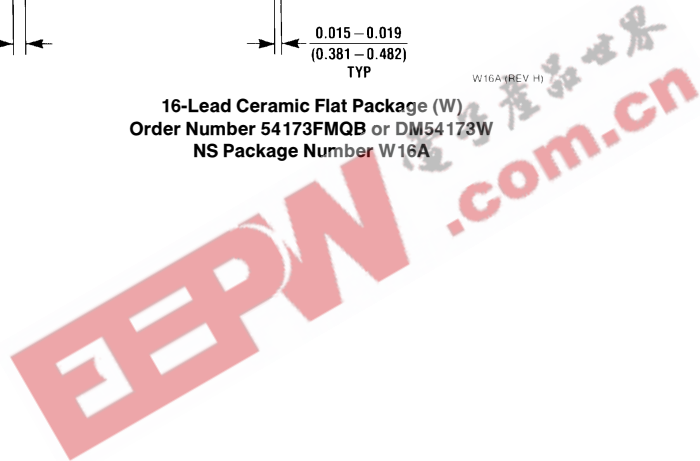


TL/F/6556-2

Physical Dimensions inches (millimeters) (Continued)



16-Lead Ceramic Flat Package (W)
Order Number 54173FMQB or DM54173W
NS Package Number W16A



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