

54/74198

8-BIT R/L SHIFT REGISTER

DESCRIPTION — The '198 features synchronous parallel load, hold, shift right and shift left modes, as determined by the Select (S_0, S_1) inputs. State changes are initiated by the rising edge of the clock. An asynchronous Master Reset ($\overline{MR}$) input overrides all other inputs and clears the register. The '198 is useful for serial-serial, serial-parallel, parallel-serial and parallel-parallel register transfers.

- PARALLEL IN/PARALLEL OUT
- SYNCHRONOUS PARALLEL LOAD
- SHIFT RIGHT AND SHIFT LEFT CAPABILITY
- ASYNCHRONOUS OVERRIDING CLEAR

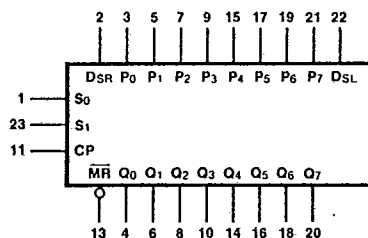
ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE	MILITARY GRADE	PKG TYPE
		$V_{CC} = +5.0\text{ V} \pm 5\%$, $T_A = 0^\circ\text{C to } +70^\circ\text{C}$	$V_{CC} = +5.0\text{ V} \pm 10\%$, $T_A = -55^\circ\text{C to } +125^\circ\text{C}$	
Plastic DIP (P)	A	74198PC		9N
Ceramic DIP (D)	A	74198DC	54198DM	6N
Flatpak (F)	A	74198FC	54198FM	4M

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

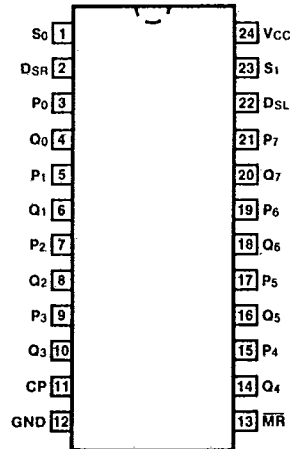
PIN NAMES	DESCRIPTION	54/74 (U.L.) HIGH/LOW
S_0, S_1	Mode Select Inputs	1.0/1.0
$P_0 - P_7$	Parallel Data Inputs	1.0/1.0
D_{SR}	Serial Data Input (Shift Right)	1.0/1.0
D_{SL}	Serial Data Input (Shift Left)	1.0/1.0
CP	Clock Pulse Input (Active Rising Edge)	1.0/1.0
$\overline{MR}$	Asynchronous Master Reset Input (Active LOW)	1.0/1.0
$Q_0 - Q_7$	Flip-flop Outputs	20/10

LOGIC SYMBOL:



$V_{CC} = \text{Pin } 24$
 $GND = \text{Pin } 12$

CONNECTION DIAGRAM PINOUT A



FUNCTIONAL DESCRIPTION — The '198 contains eight edge-triggered D-type flip-flops and the interstage gating required to perform synchronous parallel load, shift right, and shift left operations. Serial data enters at DSR for shift right and at DSL for shift left operations. Parallel data is applied to the P₀ — P₇ inputs. State changes are initiated by the rising edge of the clock. The DSR, DSL and P₀ — P₇ inputs can change when the clock is in either state, provided only that the recommended setup and hold times are observed.

The operating mode is determined by S₀ and S₁, as shown in the Mode Select Table. Clocking of the flip-flops is inhibited when both S₀ and S₁ are LOW. To avoid inadvertently clocking the register, the Select inputs should only be changed while CP is HIGH. A LOW signal on MR overrides all other inputs and forces the outputs LOW.

MODE SELECT TABLE

INPUTS				RESPONSE
MR	CP	S ₀ *	S ₁ *	
L	X	X	X	Asynchronous Reset; Outputs = LOW
H	✓	H	H	Parallel Load; P _n → Q _n
H	✓	L	H	Shift Right; DSR → Q ₀ , Q ₀ → Q ₁ , etc.
H	✓	H	L	Shift Left; DSL → Q ₇ , Q ₇ → Q ₆ , etc.
H	X	L	L	Hold

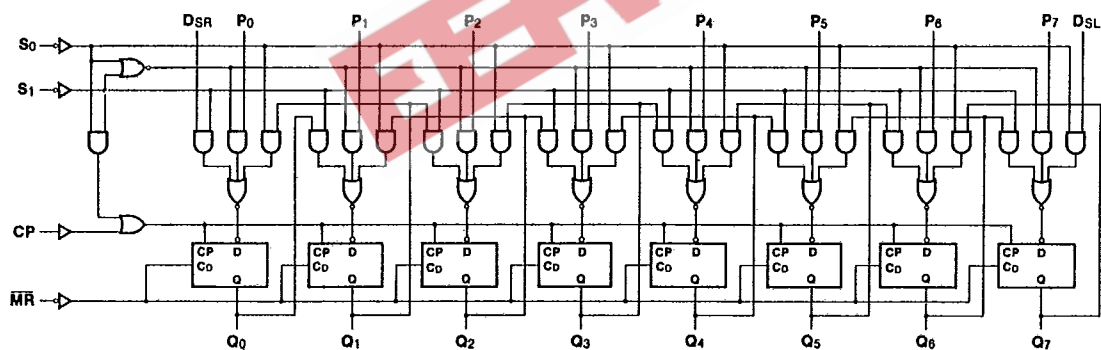
*Select inputs should be changed only while CP is HIGH

H = HIGH Voltage Level

L = LOW Voltage Level

X = Immaterial

LOGIC DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER	54/74		UNITS	CONDITIONS
		Min	Max		
I _{CC}	Power Supply Current	XC	116	mA	V _{CC} = Max; S ₀ , S ₁ = 4.5 V CP = $\overline{J}$; $\overline{MR}$, P _n = Gnd
		XM	104		

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25°C (See Section 3 for waveforms and load configurations)

AC CHARACTERISTICS: f _{max} = 100 MHz					
SYMBOL	PARAMETER	54/74		UNITS	CONDITIONS
		C _L = 15 pF R _L = 400 Ω			
		Min	Max		
f _{max}	Maximum Shift Frequency	25		MHz	Figs. 3-1, 3-8
t _{PLH} t _{PHL}	Propagation Delay CP to Q _n	26 30		ns	Figs. 3-1, 3-8
t _{PHL}	Propagation Delay <u>MR</u> to Q _n	35		ns	Figs. 3-1, 3-16

AC OPERATING REQUIREMENTS: V_{CC} = +5.0 V, T_A = +25°C

SYMBOL	PARAMETER	54/74		UNITS	CONDITIONS
		Min	Max		
t _s (H) t _s (L)	Setup Time HIGH or LOW P _n , D _{sL} , D _{sR} to CP	20 20		ns	Fig. 3-6
t _h (H) t _h (L)	Hold Time HIGH or LOW P _n , D _{sL} , D _{sR} to CP	0 0		ns	
t _s (H) t _s (L)	Setup Time HIGH or LOW S ₀ or S ₁ to CP	30 30		ns	
t _h (H) t _h (L)	Hold Time HIGH or LOW S ₀ or S ₁ to CP	0 0		ns	
t _w (H)	CP Pulse Width HIGH	20		ns	
t _w (L)	$\overline{MR}$ Pulse Width LOW	20		ns	Fig. 3-16