## ■ OVERVIEW

The SM6104 is a 6-bit flash parallel A/D converter based on NPC's proprietary molybedenum gate CMOS technology. It features a high-speed conversion of 20 Msps, and a low current consumption of 16mA (typ). The SM6104 is available speed in 18-pin plastic DIPs and 18-pin plastic SOPs.

## ■ FEATURES

- 6-bit resolution
- Maximum conversion speed: 20 Msps
- Non-linearity of ±1/2 LSB (type)
- Differential non-linearity of ±1/2 LSB (typ)
- Guaranteed mono converts without code missing
- External sample-and-hold circuits not required
- Internal output latch for 6-bit conversion data and overflow flag
- Tristate output drivers
- Supports 7-bit conversion using two devices connected in series.
- Supports 40 Msps conversion using twod evices connected in parallel (SM6104P and SM6104S only)
- Single 5 V supply
- Molybdenum gate CMOS process, low-power 16mA (typ) at 5.0V and 20 MHz (SM6104P AND SM6104S)

## ■ SELECTION GUIDE

| Version | Conversion | Package |
|---|---|---|
| SM6104P | 20Msps | 18 pinDIP |
| SM6104P1 | 15Msps | 18 pin DIP |
| SM6104S | 20Msps | 18 pin SOP |
| SM6104S1 | 15Msps | 18 pin SOP |

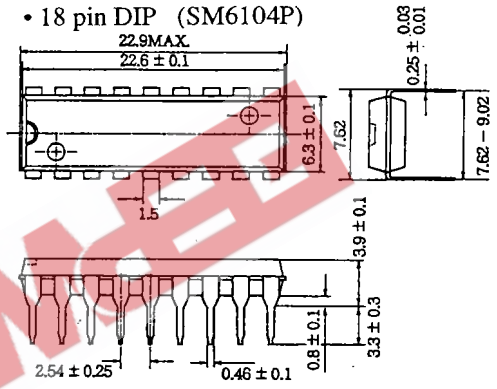
## ■ APPLICATIONS

- High-speed facsimile machines
- Digital television systems
- Color television decoder units
- Radar pulse analysis
- Data acquisition systems
- Any other applications that require high-speed, low-power A/D conversion.

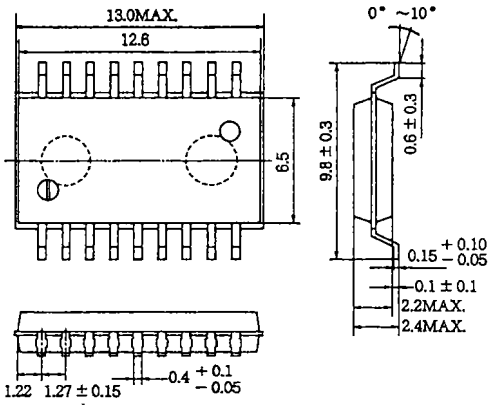
## ■ PACKAGE DIMENSIONS

Unit: mm

• 18 pin DIP (SM6104P)

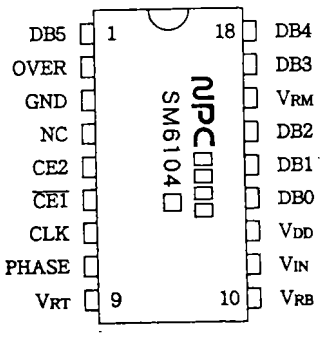



• 18 pin SOP (SM6104S)

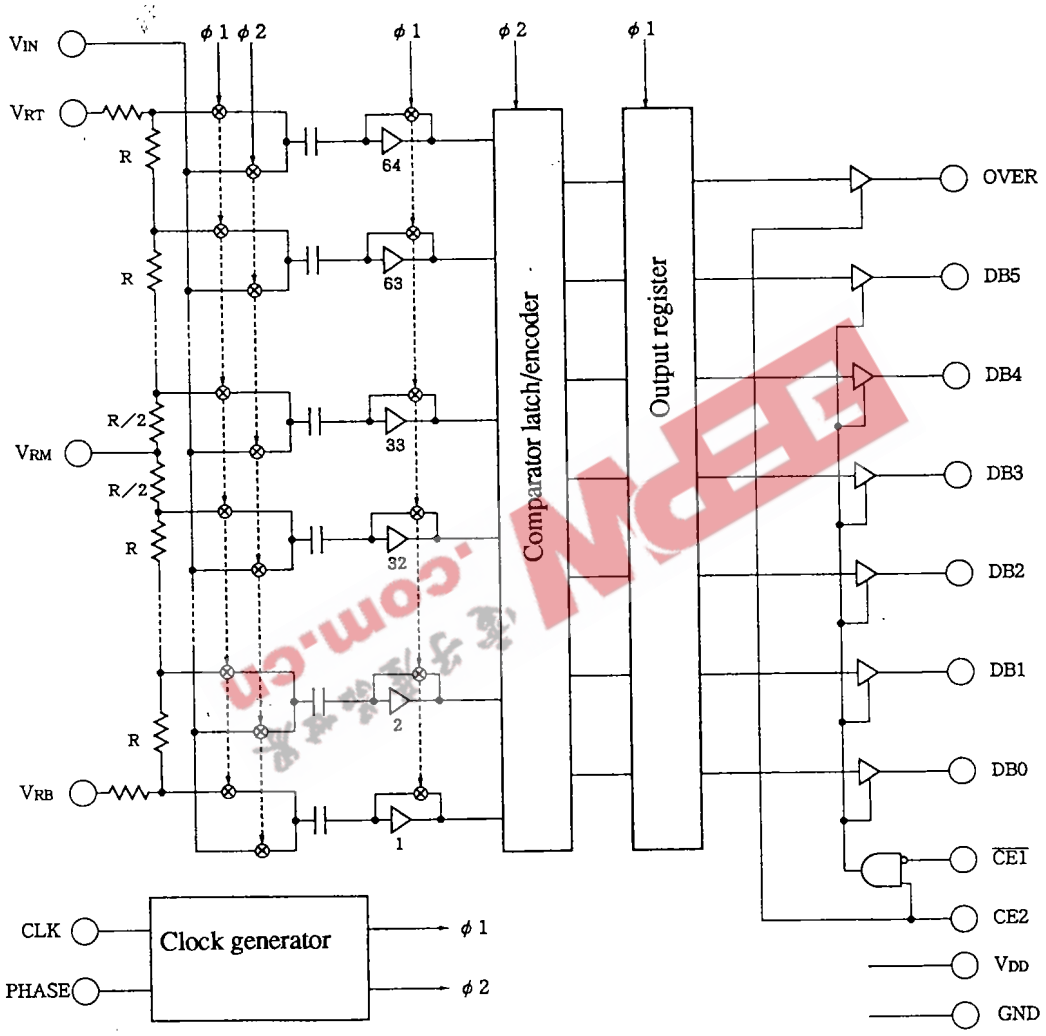



## ■ PIN OUT

TOP VIEW



## ■ BLOCK DIAGRAM




## ■ PIN DESCRIPTION

| No. | Pin | Description | No. | Pin | Description |
|---|---|---|---|---|---|
| 1 | DB5 | Data output pin (MSB) | 10 | $V_{RS}$ | Reference voltage (LOW) |
| 2 | OVER | Overflow flag (tristate) | 11 | $V_{IN}$ | Analog input, $V_{RB} \leq V_{IN} \leq V_{RT}$ |
| 3 | GND | Ground ( – ) | 12 | $V_{DD}$ | Positive supply |
| 4 | NC | No connection | 13 | DB0 | Data output (LSB) |
| 5 | CE2 | Tristate control pin | 14 | DB1 | Data output |
| 6 | $\overline{CE1}$ | Tristate control pin | 15 | DB2 | Data output |
| 7 | CLK | Clock input | 16 | $V_{RM}$ | Reference voltage centerpoint (linearity compensation) |
| 8 | PHASE | Clock polarity select | 17 | DB3 | Data output |
| 9 | $V_{RT}$ | Reference voltage (HIGH) | 18 | DB4 | Data output |

## ■ ABSOLUTE MAXIMUM RATINGS

(GND = 0V)

| Item | Symbol | Rating | Unit |
|---|---|---|---|
| Supply voltage | $V_{DD}$ | -0.3 to +7.0 | V |
| Input/output voltage | $V_{IN}$, $V_{IN}$ | -0.3 to $V_{DD}$ +0.3 | V |
| Storage temperature | $T_{STG}$ | -40 to +125 | °C |
| Power dissimption | $P_W$ | 500 | mW |
| Soldering temperature | $T_{SLD}$ | 260 | °C |
| Soldering time | $t_{SLD}$ | 10 | sec |

## ■ RECOMMENDED OPERATING CONDITIONS

(GND = 0V)

| Item | Symbol | MIN | TYP | MAX | Unit |
|---|---|---|---|---|---|
| Supply voltage | $V_{DD}$ | 4.75 | 5.0 | 5.25 | V |
| Reference voltage 1 | $V_{RT}$ | $V_{RB}$+ 2.0 | | $V_{DD}$+ 0.1 | V |
| Reference voltage 2 | $V_{RB}$ | -0.1 | | $V_{RT}$- 2.0 | V |
| Analog full scale | $V_{RT}$- $V_{RB}$ | 2.0 | | | V |
| Operating temperature | $T_{OPR}$ | 0 | | 70 | °C |

## ■ DC ELECTRICAL CHARACTERISTICS

$V_{DD}$ = 5V±5%, $f_{CLK}$=20MHz, Ta=0 to 70 °C unless otherwise noted.

| Item | Symbol | Condition | Limits MIN | Limits TYP | Limits MAX | Unit |
|---|---|---|---|---|---|---|
| Digital input voltage | $V_{IH}$ | | 3.5 | | | V |
| | $V_{IL}$ | | | | 1.0 | |
| Digital input current | $I_{IH}$ | $V_{IN}$=$V_{DD}$ | | | 2 | µA |
| | $I_{IL}$ | $V_{IN}$=0V | -2 | | | |
| Digital output voltage | $V_{OH}$ | $I_{OH}$=-1.0mA | *1 | | | V |
| | $V_{OL}$ | $I_{OL}$=2.0mA | | | 0.4 | |
| Tristate output leak voltage | $I_{OHL}$ | $V_O$=$V_{DD}$ | | | 3 | µA |
| | $I_{OLL}$ | $V_O$=0V | -3 | | | |
| Analog input registor | $R_{VIN}$ | $V_{IN}$=DC | 1 | | | MΩ |
| Analog input capacitor | $C_{VIN}$ | | | 50 | | pF |
| Reference input | $R_{REF}$ | $V_{RT}$ to $V_{RB}$ | 180 | 250 | 350 | Ω |
| Current consumption | $I_{DD}$ | SM6104P/S | | 16 | 25 | mA |
| | | SM6104P1/S1 *2 | | 16 | 25 | |

*1: VDD=0.4

*2: $f_{CLK}$=15MHz

## ■ CONVERSION CHARACTERISTICS

SM6104P/S

$V_{DD}$ = 5V±5%, Ta=0 to 70 °C, $V_{RT}$=2.0V, $V_{RB}$ =0V, unless otherwise noted.

| Item | Symbol | Condition | | Rating MIN | Rating TYP | Rating MAX | Unit |
|---|---|---|---|---|---|---|---|
| Resolution | RES | | | | | 6 | Bits |
| Non-linearity | NL | $V_{IN}$= | $f_{CLK}$=20MHz | | ±1/2 | ±1 | LSB |
| | | DC | $f_{CLK}$=5MHz | | ±1/4 | ±1/2 | |
| Differential Non-linearity | DNL | $V_{IN}$= | $f_{CLK}$=20MHz | | ±1/2 | ±3/4 | LSB |
| | | DC | $f_{CLK}$=5MHz | | ±1/4 | ±1/2 | |

SM6104P1/S1

| Item | Symbol | Condition | | Rating MIN | Rating TYP | Rating MAX | Unit |
|---|---|---|---|---|---|---|---|
| Resolution | RES | | | | | 6 | Bits |
| Non-linearity | NL | $V_{IN}$= | $f_{CLK}$=15MHz | | ±1/2 | ±3/4 | LSB |
| | | DC | $f_{CLK}$=5MHz | | ±1/4 | ±1/2 | |
| Differential Non-linearity | DNL | $V_{IN}$= | $f_{CLK}$=15MHz | | ±1/2 | ±3/4 | LSB |
| | | DC | $f_{CLK}$=5MHz | | ±1/4 | ±1/2 | |

## ■ AC ELECTRICAL CHARACTERISTICS

SM6104P/S

$V_{DD}$ = 5V±5%, Ta=0 to 70 °C, unless otherwise noted.

| Item | Symbol | Rating MIN | Rating TYP | Rating MAX | Unit |
|---|---|---|---|---|---|
| CLK HIGH-level pulse width | $t_{PWH}$ | 25 | | 5000 | ns |
| CLK LOW-level pulse width | $t_{PWL}$ | 25 | | 5000 | |
| Aperture delay time | $t_A$ | | 10 | | |
| Conversion delay time | $t_D$ | | 25 | 40 | |

SM6104P1/S1

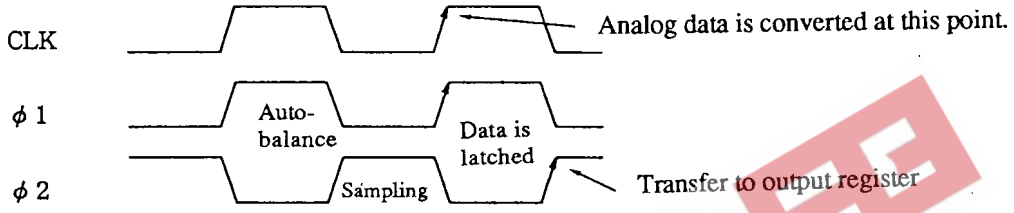
| Item | Symbol | Rating MIN | Rating TYP | Rating MAX | Unit |
|---|---|---|---|---|---|
| CLK HIGH-level pulse width | $t_{PWH}$ | 33 | | 5000 | ns |
| CLK LOW-level pulse width | $t_{PWL}$ | 33 | | 5000 | |
| Aperture delay time | $t_A$ | | 10 | | |
| Conversion delay time | $t_D$ | | 25 | 40 | |

1. Conversion Operation

Conversion is controlled by the external clock input to pin CLK which is used to generate the internal clocks ø1 and ø2. The PHASE pin switches the polarity of the internal clocks as shown in the table on the right.

| PHASE | ø 1 | ø 2 |
|---|---|---|
| 0 | CLK | $\overline{CLK}$ |
| 1 | $\overline{CLK}$ | CLK |

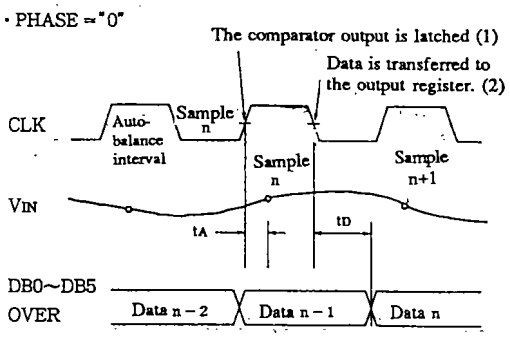
ex.) When PHASE = 0:



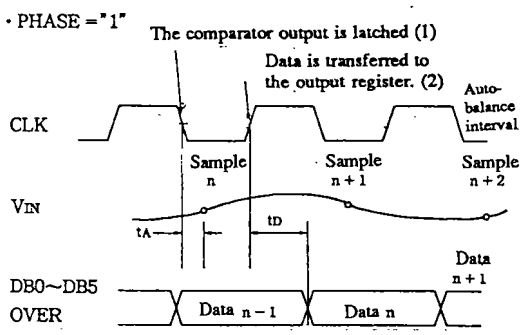

The period during which ø1 is HIGH is called the auto-balance interval. During this interval, the reference voltage is divided by the internal resistor ladder. These reference voltages are input to 64 comparators. The period during which ø2 is HIGH is called the sampling interval. During this interval, the analog voltage is input to the comparators and compared with the previously latched reference voltages.

2. Timing Charts

PHASE = LOW




PHASE = HIGH



3. Output tristate control

| $\overline{CE1}$ | CE2 | DB0 to DB5 | OVER |
|---|---|---|---|
| 0 | 1 | Enable | Enable |
| 1 | 1 | Hi-Z | Enable |
| x | 0 | Hi-Z | Hi-Z |

4. Output code

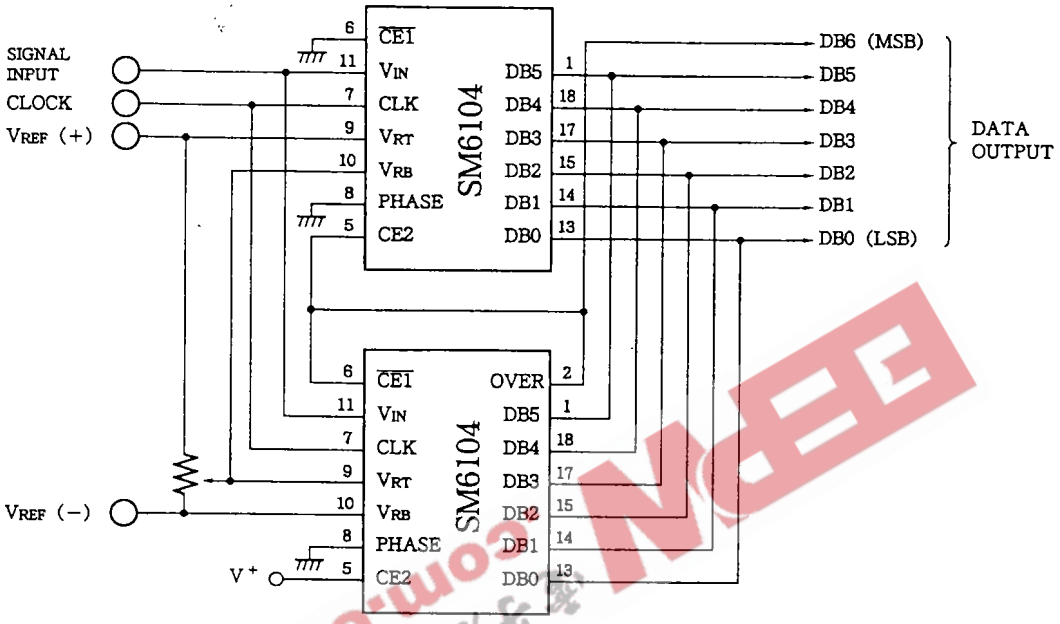
($V_{RT}$ = about 2.56V, $V_{RB}$ = about 0V)

| Analog input voltage (V) | Input code | | | | | | | Decimal |
|---|---|---|---|---|---|---|---|---|
| | OVER | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | |
| 0.00 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0.04 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| 0.08 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 2 |
| 0.12 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 3 |
| 0.16 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 4 |
| | : | | | | : | | | : |
| | : | | | | : | | | : |
| 1.20 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 30 |
| 1.24 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 31 |
| 1.28 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 32 |
| 1.32 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 33 |
| 1.36 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 34 |
| | : | | | | : | | | : |
| | : | | | | : | | | : |
| 2.40 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 60 |
| 2.44 | 0 | 1 | 1 | 1 | 1 | 0 | 1 | 61 |
| 2.48 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 62 |
| 2.52 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 63 |
| 2.56 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 127 |

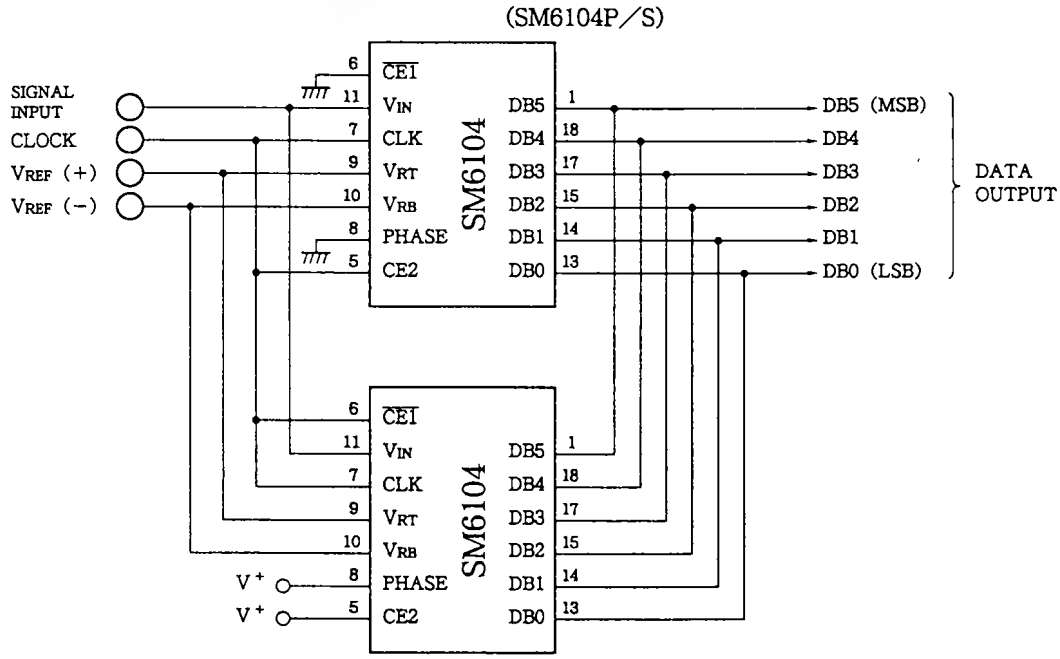
- The analog input voltages shown in this table are the center voltages of each step. Adjust VRT and VRB so that the zero transition voltage is 0.02 V, and the full-scale voltage is 2.50 V.

## ■ APPLICATION CIRCUITS

1. 7-bit resolution




2. 6-bit resolution 40MHz sampling (SM6104P/S)



* USAGE NOTES

1. Use appropriately stabilized supplies for the power supply and reference voltages, and be sure to use tantalum and ceramic bypass capacitors.
2. Use a single-point earth for the system ground.
3. Ensure that digital noise is not fed through to the analog input. For example, design the circuit board layout so that both sides of the analog input are shielded by AGND.
4. The SM6104 uses CMOS chopper comparators. Since the analog input is alternately connected and disconnected to the input capacitance of the chopper, it must be driven from a low-impedance buffer. Using buffer amplifier is preferable.

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