MRT Dev
6-, 8-, 34-Mbit/s Line Interf
TXC-02
DATA SHE

FEATURES

- 6312/8448/34368 kbit/s line interface
- AGC and equalizer
- Line quality monitor (10^{-6} error rate)
- Receive loss of signal and transmit loss of clock alarms
- Optional HDB3 encoder/decoder
- Two loopbacks:
  -Receive to transmit (digital)
  -Transmit to receive (analog)
- Optional transmit and receive AIS generators
- Rail or NRZ terminal side I/O
- Meets CCITT Recommendation G.703

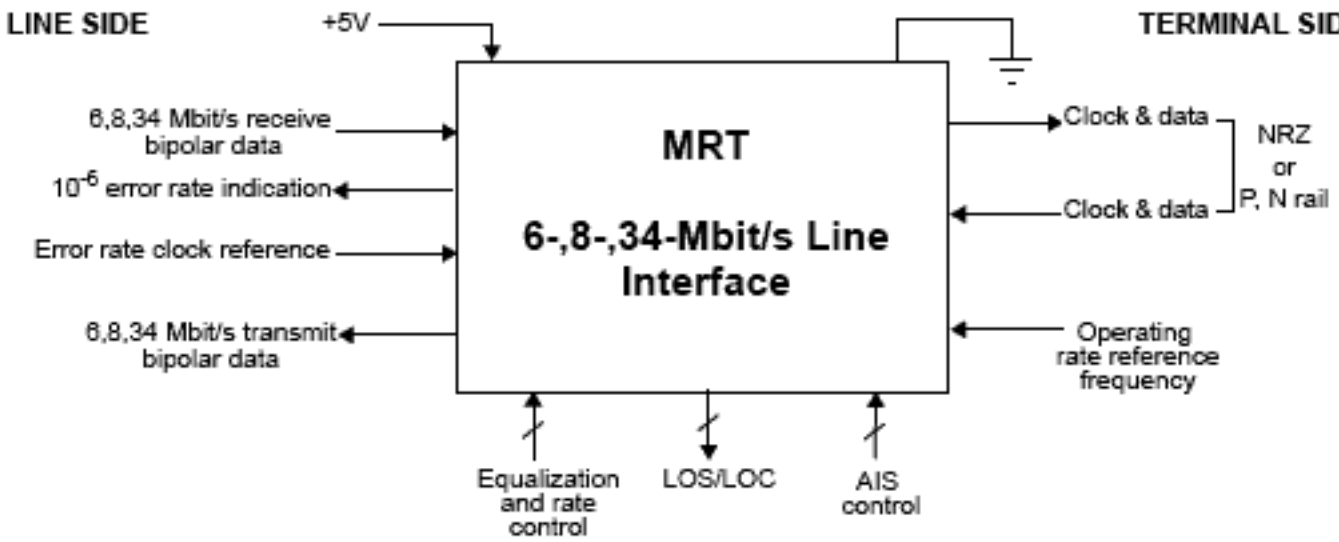
DESCRIPTION

The TranSwitch Multi-rate Receive/Transmit (M device is a CMOS VLSI device that provides the f tions needed for terminating two CCITT line rates, 8 and 34368 kbit/s, and a 6312 kbit/s rate which is sp fied in the Japanese NTT Technical Reference for Speed Digital Leased Circuits. For 8448 and 34368 k operation, the MRT provides an optional HDB3 code

The MRT is equipped with a receive equalizer circuit AGC. The MRT also provides a rail or NRZ interf HDB3 error rate monitor, alarm detection, and AIS ge ators. Testing capability is provided by transmit receive loopbacks.

APPLICATIONS

- Digital cross-connect equipment
- Remote terminals
- Terminal interface for multiplexers/demultiplexers
- Switching systems
- CSU/DSU



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BLOCK DIAGRAM

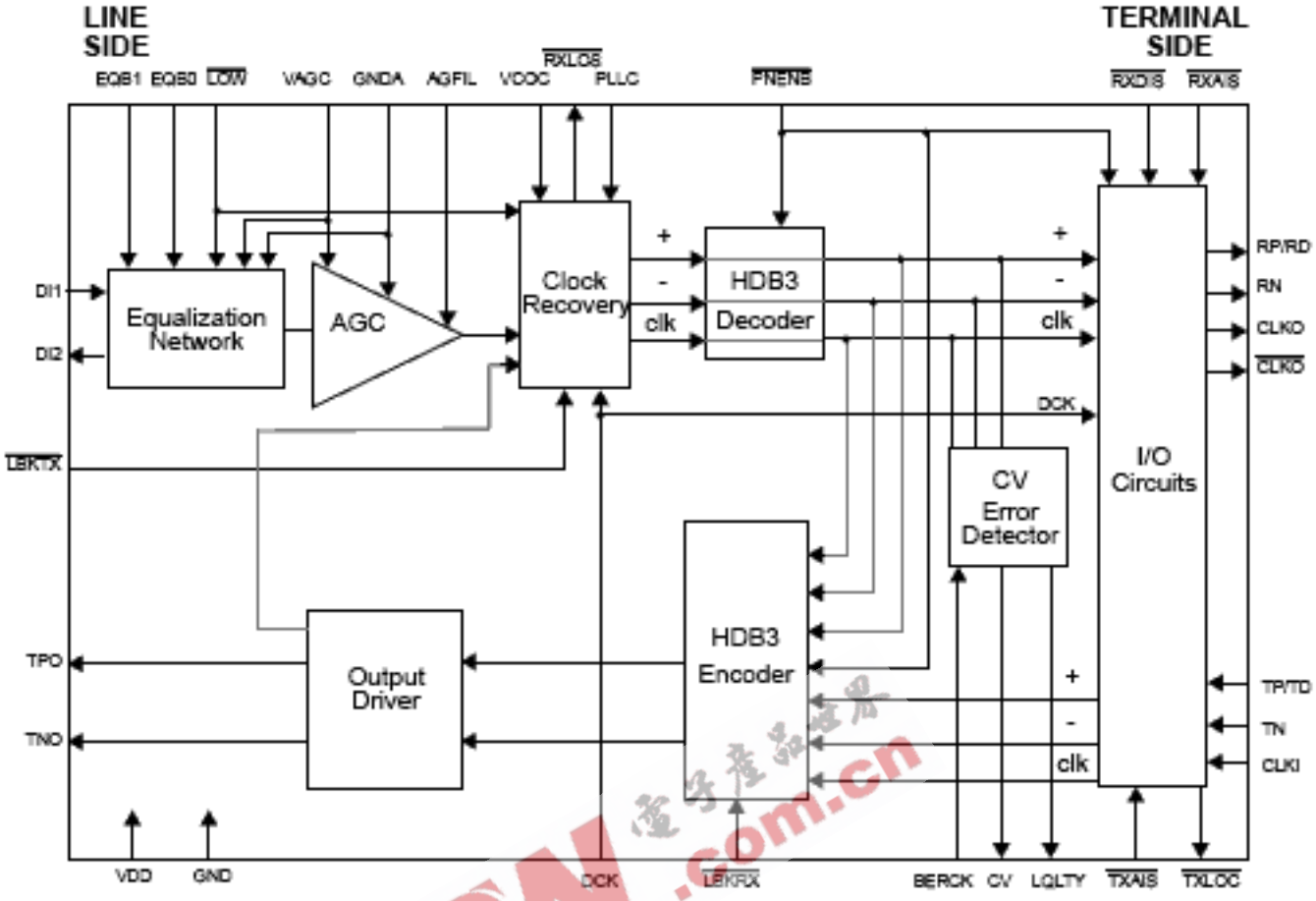


Figure 1. MRT Block Diagram

BLOCK DIAGRAM DESCRIPTION

On the Line Side, a symmetrical bipolar signal is applied to the input signal pin (DI1), which requires an external 75Ω termination. DI2 is a DC reference voltage output which serves as an AC ground.

Equalization for various lengths of cable having a $\sqrt{f}$ characteristic is compensated by the two EQB0 and EQB1 signal leads. The Equalization Network Block is connected to an AGC Block which has approximately a 20 dB dynamic range. The AGC has separate voltage and ground leads for noise immunity, and uses an external capacitor as part of an AGC filter. The AGC output is connected to the Clock Recovery Block.

The Clock Recovery Block contains a phase-locked loop and supporting logic to generate a clock signal from the line signal. The signal lead $\overline{LOW}$ selects the appropriate circuit in the Clock Recovery Block for the operating frequency and provides input attenuation for the receive line signal. The line signal is monitored for loss of signal, with an alarm indication provided on the $\overline{RXLOS}$ signal lead. The Clock Recovery Block requires an external reference clock at the operating frequency (DCK). The reference clock is also used for generating and sending a receive Alarm Indication Signal (AIS). The generation and sending of AIS for recovered data is controlled by the $\overline{RXAIS}$ signal lead.

The output of the Clock Recovery Block is connected to the HDB3 Decoder Block or the Output Circuits Block. When the decoder is enabled, indications of coding violation errors, other than the normal HDB3 zero substitution codes, are provided as pulses on the signal lead labeled CV. An external clock (BERCK) is used to generate a 10-second sampling window for detecting a 10^{-6} or greater error rate. The line quality indication is provided on the signal lead labeled LQLTY.

Two Terminal Side interfaces are provided, a positive and negative rail (RP and RN) or NRZ (RD) interface. The selection is determined by the state placed on the signal lead labeled PNENB. When a low is applied to the signal lead, the HDB3 Decoder and HDB3 Encoder Blocks are bypassed, and the terminal side I/O is a positive and negative rail interface. When a high is applied to the signal lead, an NRZ interface is provided. Data is clocked out of the MRT on negative edges of the clock signal (CLKO). Receive data and the clock signals are disabled, and forced to a high impedance state by placing a low on the receive disable lead (RXDIS). For a receive positive and negative rail interface, an inverted clock (CLKO) is also provided.

The terminal side interface for the transmitter can either be positive and negative rail (TP and TN) or NRZ (TD) data depending on the state of the common control lead PNENB. Data is clocked into the MRT on positive transitions of the clock signal (CLKI). The input clock is monitored for the loss of clock. When the input clock remains high or low, TXLOC will be set low. The MRT also provides the capability to generate and insert AIS (all ones signal), independent of the transmit data. A low placed on the TXAIS lead enables the transmit AIS generator.

Two loopbacks are provided, transmit loopback and receive loopback. Transmit loopback connects the data path from the transmitter output driver stage to the clock recovery, and disables the external receiver input. Transmit loopback is activated by placing a low on the LBKTX signal lead.

Receive loopback connects the receive data path to the transmit output circuits and disables the transmit input. Receive loopback is activated by placing a low on the LBKRX signal lead.

For 6 Mbps operation, the MRT should be operated in the P and N rail mode, bypassing the HDB3 Decoder/ Encoder.

PIN DIAGRAM

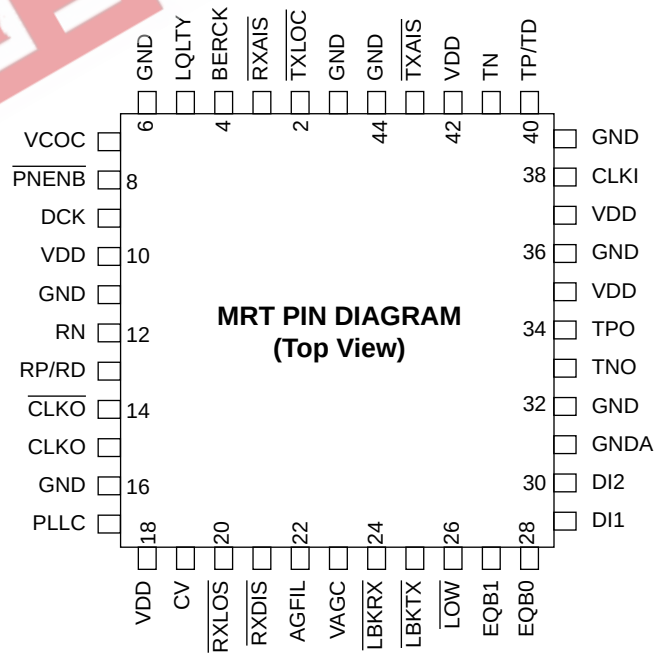


Figure 2. MRT Pin Diagram With Names and Numbers

PIN DESCRIPTIONS

Power Supply and Ground

Symbol	Pin No.	I/O/P*	Type	Name/Function
VDD	10,18,35, 37,42	P		**VDD:** 5-volt supply, ± 5%.
GND	1,6,11,16,32, 36,39,44	P		**Ground:** 0 volts reference.
VAGC	23	P		**AGC VDD:** Isolate from VDD using 1N914 or 1N4148 diode.
GNDA	31	P		**AGC Groun**d: 0 volts reference.

*Note: I = Input; O = Output; P = Power

Line Side I/O

Symbol	Pin No.	I/O/P	Type	Name/Function
DI1	29	I	Analog	**Data In 1:** HDB3 or B8ZS encoded bipolar receive data input.
DI2	30	O	Analog	**Data In 2:** DC Voltage Reference for Data Input DI1. The MRT uses an internally generated voltage reference as an AC ground for the received data input. An external 0.1 µF capacitor, in parallel with a 10 µF/6.3 V tantalum capacitor, is connected between this pin and ground. No other connection should be made to this pin.
TNO	33	O	TTL24mA	**Transmit Negative Out:** Line transmit negative; output is an active low.
TPO	34	O	TTL24mA	**Transmit Positive Out:** Line transmit positive; output is an active low.

Terminal Side I/O

Symbol	Pin No.	I/O/P	Type	Name/Function
RN	12	O	TTL4mA	**Receive Negative:** When $\overline{\text{PNENB}}$ is low, the HDB3 codec is bypassed and N-rail (RN) data is provided on this pin. When $\overline{\text{PNENB}}$ is high, the output is forced to a high impedance state.
RP/RD	13	O	TTL4mA	**Receive Positive/Receive Data:** When $\overline{\text{PNENB}}$ is low, the HDB3 codec is bypassed and P-Rail (RP) data is provided on this pin. When $\overline{\text{PNENB}}$ is high, NRZ data (RD) is provided.
$\overline{\text{CLKO}}$	14	O	CMOS8mA	**Clock Out Inverted:** Receive inverted clock output. Positive and negative rail receive data is clocked out on the rising edge. Disabled in the NRZ mode.

Symbol	Pin No.	I/O/P	Type	Name/Function
CLKO	15	O	CMOS8mA	**Clock Out:** Receive clock output. Receive positive and negative rail and NRZ data is clocked out on the falling edge.
CLKI	38	I	TTLr	**Clock In:** Transmit clock input for P and N rail and NRZ data. Transmit data is clocked into the MRT on the rising edge. This clock must have a frequency of ± 20 ppm for the 34368 kbit/s operation and ± 30 ppm for the 6312/8448 kbit/s operation (ref: CCITT recommendation G.703). The duty cycle requirement for this clock signal is 50% ± 5%, measured at the 1.4V TTL threshold level.
TP/TD	40	I	TTL	**Transmit Positive/Transmit Data:** When $\overline{\text{PNENB}}$ is low, the HDB3 codec is bypassed and transmit P-rail (TP) data is applied to this pin. When $\overline{\text{PNENB}}$ is high, NRZ transmit data (TD) is applied.
TN	41	I	TTL	**Transmit Negative:** When $\overline{\text{PNENB}}$ is low, the HDB3 codec is bypassed and transmit N-Rail (TN) is applied to this pin. When $\overline{\text{PNENB}}$ is high, this input is disabled.

Alarm Signal Outputs

Symbol	Pin No.	I/O/P	Type	Name/Function
$\overline{\text{TXLOC}}$	2	O	TTL2mA	**Transmit Loss Of Clock:** Active low output. A transmit loss of clock alarm occurs when the transmit clock input (CKLI) is stuck high or low for 20-32 clock cycles. Recovery occurs on the first input clock transition.
LQLTY	5	O	TTL2mA	**Line Quality:** This signal represents a gross estimate of the line quality which is determined by counting coding violations for 34 (8) Mbit/s operation. If the line error rate exceeds a 10^{-6} threshold during a 10 (40) second interval, LQLTY goes active high. LQLTY is active low when coding violations do not exceed the 10^{-6} threshold in a 10 (40) second interval. The output on this pin is only valid when the appropriate clock signal is applied to BERCK. It should be disregarded in the P and N mode of operation.
CV	19	O	TTL2mA	**Coding Violation:** Active high output. A coding violation pulse occurs when an HDB3 coding violation is detected in the received line data input. A coding violation is not part of the HDB3 zero-substitution code. A coding violation occurs because of noise or other impairments affecting the line signal. The output of this pin should be disregarded in the P and N mode.
$\overline{\text{RXLOS}}$	20	O	TTL2mA	**Receive Loss Of Signal:** Active low output. A receive loss of signal occurs when the input data is zero for 20-32 clock cycles. Recovery occurs when the receive signal returns.

MRT Control Leads

Symbol	Pin No.	I/O/P	Type	Name/Function
$\overline{\text{RXAIS}}$	3	I	CMOSr	**Receive Alarm Indication Signal:** When $\overline{\text{RXAIS}}$ is low, the MRT generates AIS (all ones signal) for the terminal side receive output data. The line side receive data path is disabled. The reference clock (DCK) provides the clock source required for generating AIS.
BERCK	4	I	TTLr	**Bit Error Rate Clock:** This clock establishes the time base for estimating the coding violation error rate. For 34 Mbit/s operation the clock frequency must be 6 kHz, and for 8 Mbit/s operation the clock frequency must be 1.5 kHz. This pin should be left open for P and N mode operation.
$\overline{\text{PNENB}}$	8	I	CMOSr	**P And N Enable:** When $\overline{\text{PNENB}}$ is low, the P and N rail interface is enabled, and the HDB3 codec is bypassed. When $\overline{\text{PNENB}}$ is high, the terminal side I/O data is NRZ and the HDB3 codec is enabled. This pin must be held low for 6 Mbit/s operation.
DCK	9	I	TTL	**Reference Clock:** Operating frequency reference clock. For receive signal clock recovery, ± 200 ppm frequency accuracy is adequate. If the transmit and receive AIS features are used, the frequency accuracy must be ± 20 ppm for 34368 kbit/s and ± 30 ppm for 8448 and 6312 kbit/s operation. The duty cycle requirement for this clock signal is 50% ± 5% as measured at the 1.4V TTL threshold level.
$\overline{\text{RXDIS}}$	21	I	CMOSr	**Receive Disable:** When $\overline{\text{RXDIS}}$ is low, the receive side of the MRT is disabled and the RN, RP/RD, CLKO and $\overline{\text{CLKO}}$ output leads are forced to a high impedance state.
$\overline{\text{LBKRX}}$	24	I	CMOSr	**Loopback Receive:** When $\overline{\text{LBKRX}}$ is low, the MRT loops back receive data as transmit data. The receive data is also sent to the terminal side, but the transmit data input on the terminal side is disabled. (Note 1)
$\overline{\text{LBKTX}}$	25	I	CMOSr	**Loopback Transmit:** When $\overline{\text{LBKTX}}$ is low, the MRT loops back transmit data as receive data. The transmit data is sent on the line side, but the receive data input on the line side is disabled. (Note 1)
$\overline{\text{LOW}}$	26	I	CMOSr	**Low Frequency:** When $\overline{\text{LOW}}$ is low, the MRT enables equalization and input attenuator settings for 6312 or 8448 kbit/s operation. This lead also controls the clock recovery high/low frequency range circuit.

Note 1: Setting $\overline{\text{LBKTX}}$ and $\overline{\text{LBKRX}}$ low simultaneously will cause invalid outputs at the receive terminal and transmit line ports.

Symbol	Pin No.	I/O/P	Type	Name/Function
EQB1 EQB0	27 28	I I	CMOSr	**Equalizer Bit 1:** MSB of equalizer setting. **Equalizer Bit 0:** LSB of equalizer setting. Equalization is as follows for 34 Mbit/s operation: EQB1 EQB0 CABLE EQUALIZATION $\sqrt{f}$ * 1 1 0dB< cable <3.5dB 1 0 2.6dB<cable<8dB 0 0 6dB<cable<9.9dB 0 1 8.6dB<cable<13.2dB For 8 or 6 Mbit/s operation: 1 1 0dB< cable< 4.1dB 1 0 2.5dB<cable<6.5dB * f = 1/2 the bit rate
$\overline{\text{TXAIS}}$	43	I	CMOSr	**Transmit AIS:** When $\overline{\text{TXAIS}}$ is low, the MRT sends an AIS (all ones signal) for the line side transmit output data. The terminal side transmit data path is disabled. The reference clock (DCK) provides the clock required for generating AIS.

Pins With External Components

Symbol	Pin No.	I/O/P	Type	Name/Function
VCOC	7	I/O	Analog	**Voltage Controlled Oscillator Capacitor:** For 6, 8, and 34 Mbit/s operation, a 470Ω ± 5%, 1/8 watt resistor is connected in series with a 0.1 µF ± 10% capacitor to ground. These components are used in the phase-locked loop filter.
PLLC	17	I/O	Analog	**Phase-Locked Loop Capacitor:** 0.1 µF ± 10% ceramic disk capacitor connected to ground.
AGFIL	22	I/O	Analog	**Automatic Gain Filter:** For 6/8 MHz mode, 0.01 µF ± 10% ceramic disk capacitor connected to ground. For 34 Mbit/s mode, open.

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Min	Max	Unit
Supply voltage	V_{DD}	-0.3	7.0	V
AGC Supply Voltage	V_{AGC}	-0.5	6.5	V
DC input voltage	V_{IN}	-0.5	V_{DD} + 0.5	V
Continuous power dissipation	P_C		750	mW
Ambient operating temperature	T_A	-40	85	^oC
Operating junction temperature	T_J		150	^oC
Storage temperature range	T_S	-55	150	^oC

*Note: Operating conditions exceeding those listed in Absolute Maximum Ratings may cause permanent failure. Exposure to absolute maximum ratings for extended periods may impair device reliability.

THERMAL CHARACTERISTICS

Parameter	Min	Typ	Max	Unit	Test Conditions
Thermal Resistance: Junction to Ambient			46	$^oC/W$	

POWER REQUIREMENTS

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{DD}	4.75	5.0	5.25	V	
V_{AGC}	V_{DD} - 0.7		V_{DD} - 0.5	V	Isolated from VDD via a IN4148 or 1N914 diode.
I_{DD}			100	mA	V_{DD} = 5.25V
I_{AGC}			20	mA	V_{AGC} = 4.75V
P_{DD}			525	mW	V_{DD} = 5.25V
P_{AGC}			95	mW	V_{AGC} = 4.75V

INPUT, OUTPUT, AND I/O PARAMETERS

Input Parameters For TTL

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}	2.0			V	$4.75 \leq V_{DD} \leq 5.25$
V_{IL}			0.8	V	$4.75 \leq V_{DD} \leq 5.25$
Input leakage current			10	µA	$V_{DD} = 5.25$
Input capacitance		5.5		pF	

Input Parameters For TTLr

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}	2.0			V	$4.75 \leq V_{DD} \leq 5.25$
V_{IL}			0.8	V	$4.75 \leq V_{DD} \leq 5.25$
Input leakage current		50	120	µA	$V_{DD} = 5.25$
Input capacitance		5.5		pF	

Note: Input has a 100K (nominal) internal pull-up resistor.

Input Parameters For CMOSr

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}	2.0			V	$4.75 \leq V_{DD} \leq 5.25$
V_{IL}			0.8	V	$4.75 \leq V_{DD} \leq 5.25$
Input leakage current		50	120	µA	$V_{DD} = 5.25$
Input capacitance		5.5		pF	

Note: Input has a 100K (nominal) internal pull-up resistor.

Output Parameters For TTL2mA

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{OH}	V_{DD} - 0.5			V	$V_{DD} = 4.75$; $I_{OH} = -1.0$ mA
V_{OL}			0.4	V	$V_{DD} = 4.75$; $I_{OL} = 2.0$ mA
I_{OL}			2.0	mA	
I_{OH}			-1.0	mA	
tRISE	5.5	12.5	18.2	ns	C_{LOAD} = 15pF
tFALL	2.3	4.4	6.5	ns	C_{LOAD} = 15pF

Output Parameters For TTL4mA

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{OH}	V_{DD} - 0.5			V	V_{DD} = 4.75; I_{OH} = -2.0 mA
V_{OL}			0.4	V	V_{DD} = 4.75; I_{OL} = 4.0 mA
I_{OL}			4.0	mA	
I_{OH}			-2.0	mA	
t_{RISE}	2.8	6.5	9.2	ns	C_{LOAD} = 15 pF
t_{FALL}	1.3	2.3	3.4	ns	C_{LOAD} = 15 pF

Output Parameters For TTL24mA

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{OH}	V_{DD} - 0.5			V	V_{DD} = 4.75; I_{OH} = -12.0 mA
V_{OL}			0.4	V	V_{DD} = 4.75; I_{OL} = 24.0 mA
I_{OL}			24.0	mA	
I_{OH}			-12.0	mA	
tRISE	0.8	1.4	1.8	ns	C_{LOAD} = 25 pF
tFALL	0.5	0.8	1.0	ns	C_{LOAD} = 25 pF

Output Parameters For CMOS8mA

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{OH}	V_{DD} - 0.5			V	V_{DD} = 4.75; I_{OH} = -8.0 mA
V_{OL}			0.4	V	V_{DD} = 4.75; I_{OL} = 8.0 mA
I_{OL}			8.0	mA	
I_{OH}			-8.0	mA	
tRISE	1.3	2.4	3.8	ns	C_{LOAD} = 25 pF
tFALL	1.1	1.8	2.5	ns	C_{LOAD} = 25 pF

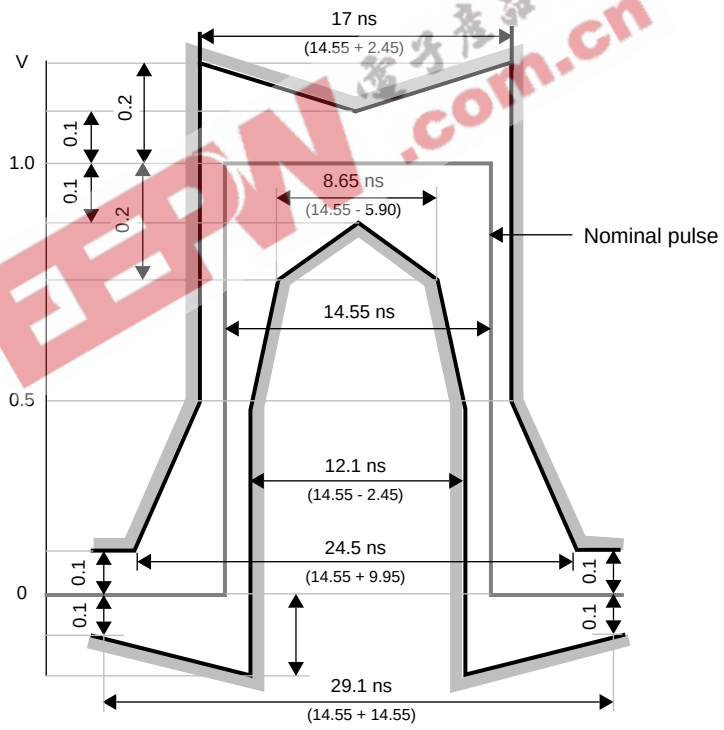
TIMING CHARACTERISTICS

Detailed timing diagrams for the MRT are illustrated in Figures 3 through 9. All output times are measured with maximum load capacitance appropriate for the pin type. Timing parameters are measured at (V_{OH} - V_{OL})/2 or (V_{IH} - V_{IL})/2 as applicable.

Line Side Timing Characteristics

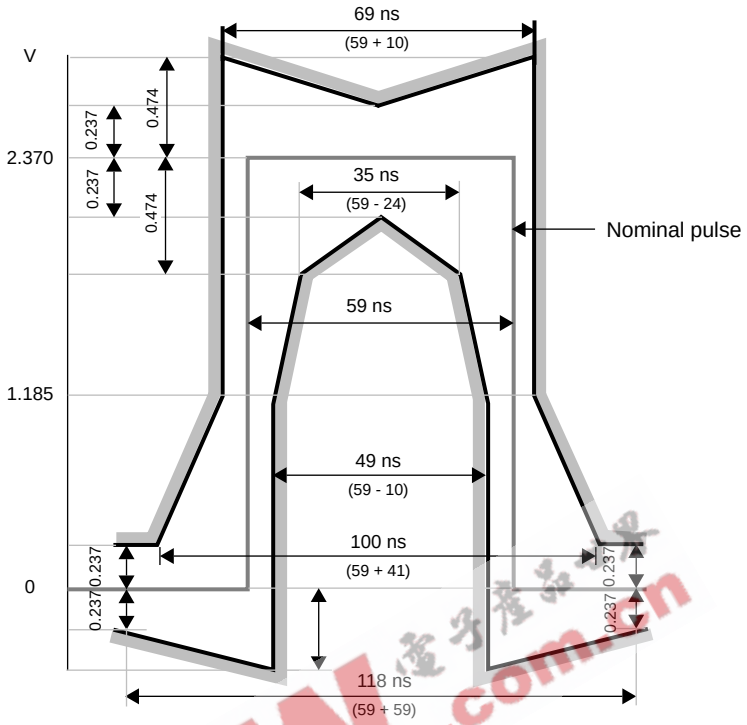
The line side timing characteristics of the MRT are designed so that the line output mask at the transformer output meets the wave shapes specified in CCITT recommendation G.703 for 34 and 8 Mbit/s operation and the NTT Technical Reference for High Speed Digital Leased Circuit Service for 6 Mbit/s operation. The pulse masks for each of the three modes of operation are shown in Figures 3, 4, and 5. Refer to the corresponding standard cited in each case for further details regarding the interface.

Figure 3. Pulse Mask at the 34368 kbit/s Interface



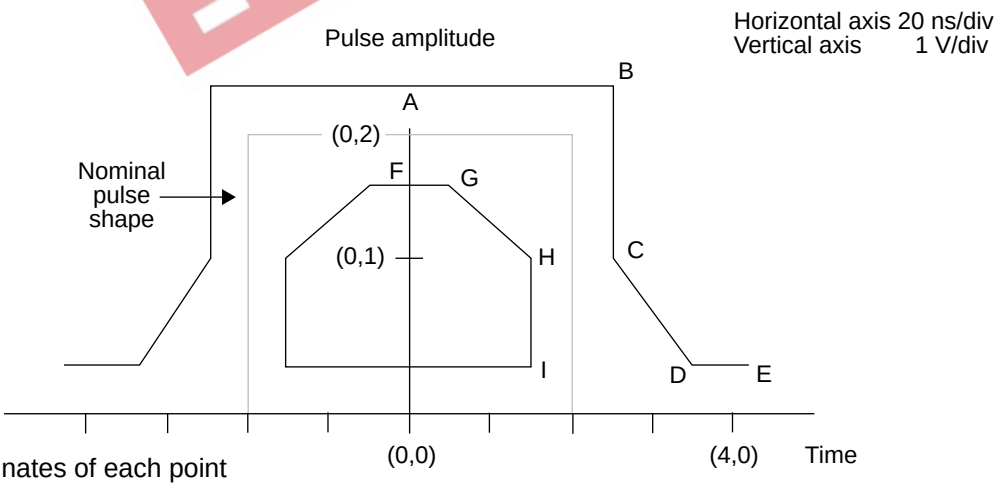
Reference: CCITT Recommendation G.703

Figure 4. Pulse Mask at the 8448 kbit/s Interface



Reference: CCITT Recommendation G.703

Figure 5. Pulse Mask at the 6312 kbit/s Interface



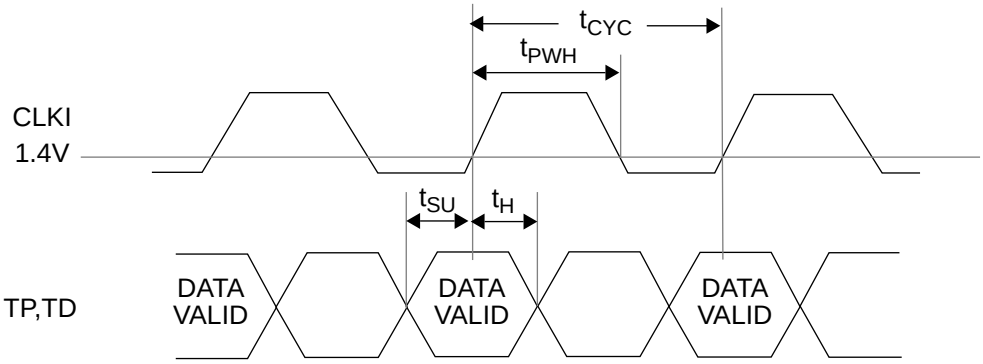
Coordinates of each point

A : (0, 2.3) F : (0, 1.7)
B : (2.4, 2.3) G : (0.4, 1.7)
C : (2.4, 1.0) H : (1.6, 0.9)
D : (3.2, 0.3) I : (1.6, 0.3)
E : (4.0, 0.3)

Reference: NTT Technical Reference for
High-Speed Digital Leased Circuit Services

Terminal Side Timing Characteristics

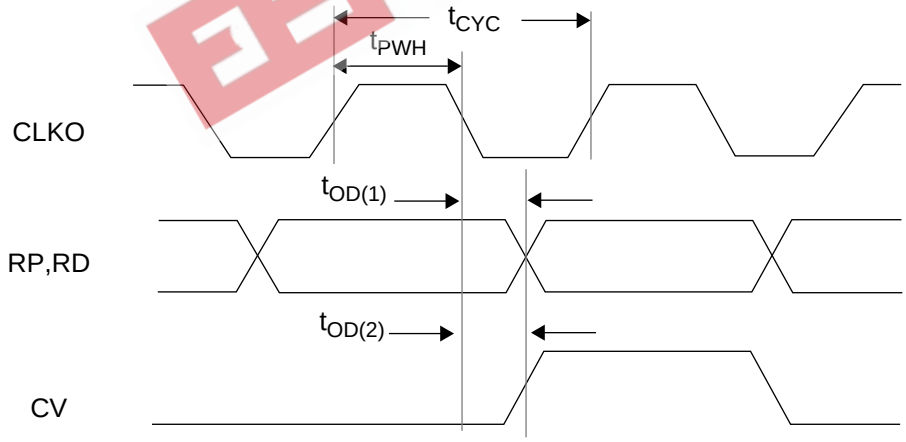
Figure 6. NRZ Transmit Input



Parameter	Symbol	Min	Typ	Max	Unit
CLKI clock period	t_{CYC}		Note 2		ns
CLKI duty cycle (t_{PWH}/t_{CYC})	--	45		55	%
TP,TD set-up time to CLKI↑	t_{SU}	3			ns
TP,TD hold time after CLKI↑	t_H	2			ns

Note 1: CLKI symmetry is measured about the 1.4VDC threshold in order to assure symmetric output waveforms.
Note 2: The clock input can be 6, 8, or 34 MHz (refer to page 5).

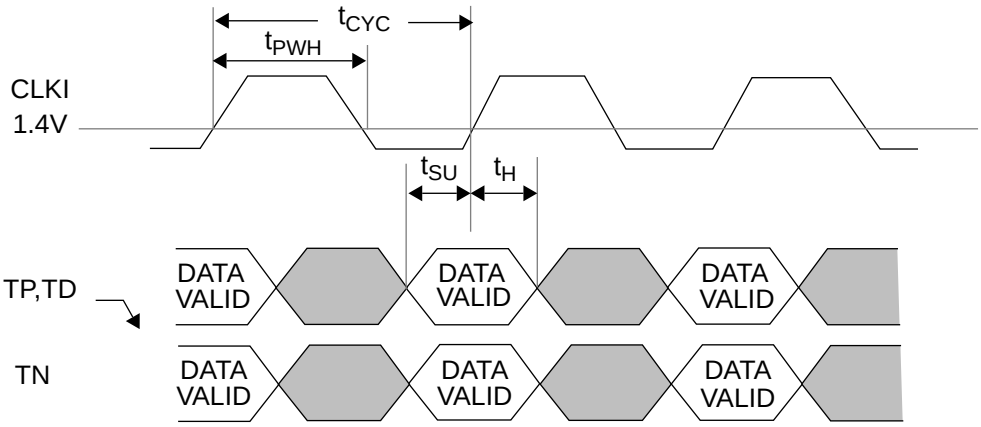
Figure 7. NRZ Receive Output



Parameter	Symbol	Min	Typ	Max	Unit
CLKO clock period	t_{CYC}		Note 2		ns
CLKO duty cycle (t_{PWH}/t_{CYC})	--	45		55	%
RP,RD output delay after CLKO↓	$t_{OD(1)}$	-5		5	ns
CV output delay after CLKO↓	$t_{OD(2)}$	-5		5	ns

Note 1: CKLO symmetry is measured about the 50% amplitude point.
Note 2: The clock output can be 6, 8, or 34 MHz (refer to page 4).

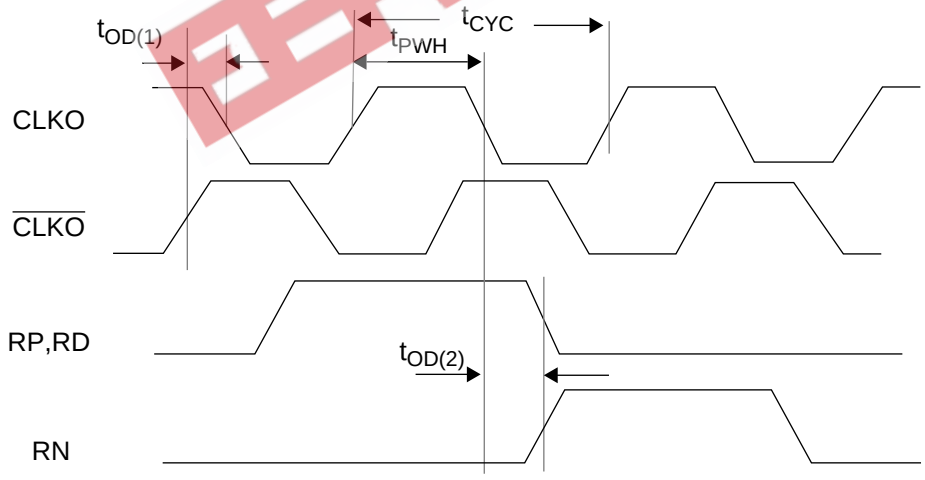
Figure 8. P and N Rail Transmit Input



Parameter	Symbol	Min	Typ	Max	Unit
CLKI clock period	t_{CYC}		Note 2		ns
CLKI duty cycle (t_{PWH}/t_{CYC})	--	45		55	%
TP,TD & TN set-up time to CLKI↑	t_{SU}	3			ns
TP,TD & TN hold time after CLKI↑	t_H	2			ns

Note 1: CLKI symmetry is measured about the 1.4VDC threshold.
Note 2: The clock input can be 6, 8, or 34 MHz (refer to page 5).

Figure 9. P and N Rail Receive Timing



Parameter	Symbol	Min	Typ	Max	Unit
CLKO clock period	t_{CYC}		Note 2		ns
CLKO duty cycle (t_{PWH}/t_{CYC})	--	45		55	%
CLKO output delay after $\overline{CLKO}$↑	$t_{OD(1)}$			2	ns
RP, RD and RN output delay after CLKO↓	$t_{OD(2)}$	-5		6	ns

Note 1: CLKO symmetry is measured about the 50% amplitude point.
Note 2: The clock output can be 6, 8, or 34 MHz (refer to page 4).

OPERATION

POWER SUPPLY

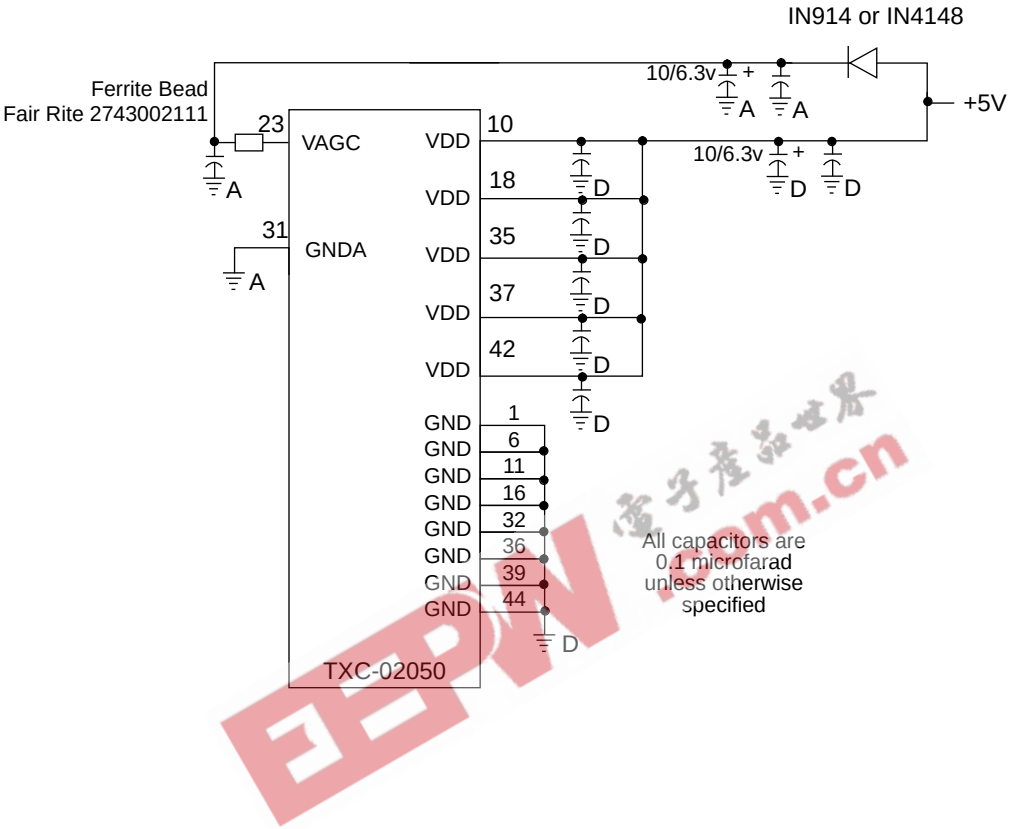


Figure 10. MRT Power Supply Connections

The MRT device has separate power supply pins labeled VDD and VAGC. The VAGC supply pin is connected to the internal AGC amplifier and requires isolation from the VDD supply as indicated in Figure 10. Separate bypass networks must be used for connecting the VDD and VAGC supply pins on the MRT to +5V. The bypass network on the VAGC pin consists of an IN4148 or IN914 diode, and a 10/6.3 volt microfarad (tantalum) capacitor connected in parallel with a 0.1 microfarad capacitor, as shown in Figure 10. TranSwitch recommends that the 0.1 microfarad decoupling capacitors be of RF quality and that they be connected in close proximity to the device.

OVERVIEW

Line Side Input Impedance

The input impedance of the MRT is a function of the state of the $\overline{\text{LOW}}$ lead and the operating rate. Table 1 lists the input impedance of the MRT at the operating line rates (which are 1/2 the bit rates).

Table 1. MRT Input Impedance

Condition	Minimum Input Impedance, | Z |
$\overline{\text{LOW}}$ = 1, line rate = 17184 kbit/s	1260 ohms
$\overline{\text{LOW}}$ = 0, line rate = 4224 kbit/s	2390 ohms
$\overline{\text{LOW}}$ = 0, line rate = 3156 kbit/s	3670 ohms

Line Side Input Sensitivity

The input voltage sensitivity of the MRT depends on the state of the $\overline{\text{LOW}}$ lead as shown in Table 2 below.

Table 2. MRT Input Sensitivity

$\overline{\text{LOW}}$ Lead	Input Sensitivity (peak volts) Min	Max	
0	0.5	2.7	(6 & 8 Mbit/s)
1	0.15	1.1	(34 Mbit/s)

Line Side Input Circuit

The circuit shown in Figure 11 illustrates the component required for operating the MRT device for 34368, 8448 or 6312 kbit/s. The transformer should have a frequency response of 0.2 to 80 MHz with an insertion loss of 1 dB, maximum. TranSwitch recommends the use of a Coilcraft transformer (part no. WB-1010) or equivalent). This gives return loss and isolation voltage values that meet or exceed requirements.

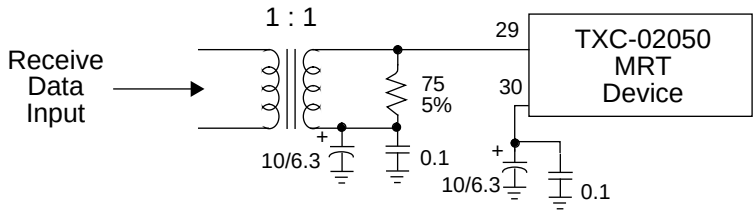


Figure 11. Line Side Input Circuit

Line Side Output Characteristics

The line side output of the MRT switches from “rail to rail” on both of its output leads, TPO and TNO. This provides the maximum voltage swing, and makes the output voltage depend on the +5 volt power supply input to the chip. The external circuit design must therefore be done with care in order to assure the meeting of the amplitude requirements.

Line Side Output Circuits

Figure 12 illustrates the output circuit required for operating the MRT device for a 34368 kbit/s application. The transformer and resistors shown assure that the output waveform meets the CCITT mask for 34368 kbit/s transmission and that the MRT device is operated within the current limits of the TTL24mA output parameters on page 10. The transformer should have a frequency response of 0.1 - 100 MHz with an insertion loss of 1dB, maximum.

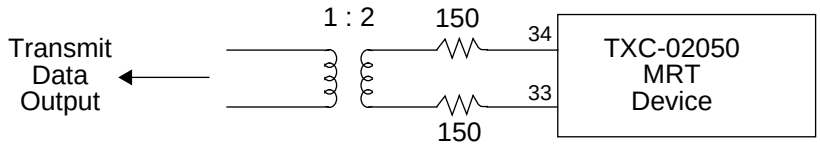


Figure 12. Line Side Output Circuit Outline (34368 kbit/s)

Figure 13 shows a variation of the circuit in Figure 12. This circuit improves performance in applications when a plastic device is mounted in a socket. The additional low-pass filter compensates for possible overshoot caused by inductance created by the device/socket interface. The transformer should have a frequency response of 0.1 - 100 MHz with an insertion loss of 1dB, maximum.

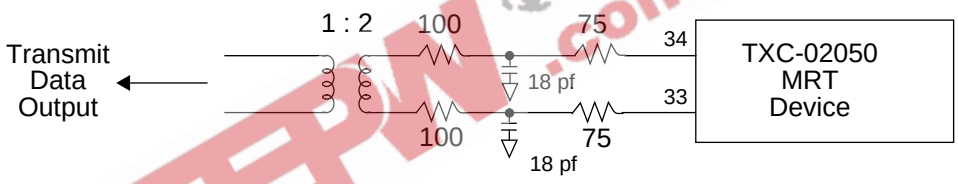


Figure 13. Line Side Output Circuit Outline (34368 kbit/s)

The peak voltage and current output requirements for 6312 and 8448 kbit/s operation are different from that required for 34368 kbit/s operation. The output circuit in Figure 14 illustrates the output circuit required for 6312 kbit/s and 8448 kbit/s operation. The transformer should have a frequency response of .01 - 50 MHz with an insertion loss of 1dB, maximum. The transformer, drivers and resistors assure that the output waveform meets the CCITT masks for these rates and that the MRT device is operated within the current limits of the TTL24mA output parameters on page 10.

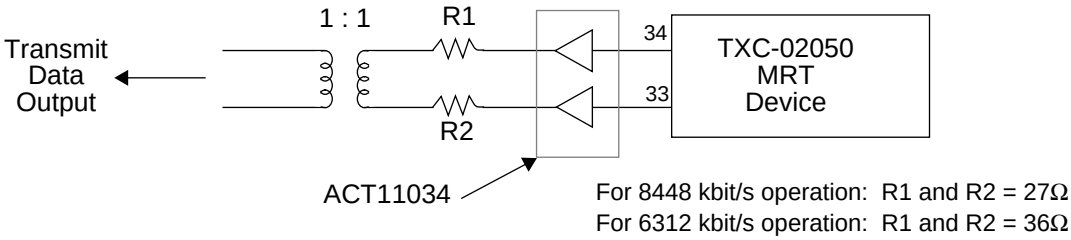


Figure 14. Line Side Output Circuit Outline (8448 and 6312 kbit/s)

Jitter Tolerance

CCITT Recommendation G.823 specifies that network equipment must be able to accommodate and tolerate levels of jitter up to certain specified limits. The MRT accommodates and tolerates more input jitter than the level of input jitter specified by the CCITT.

With input jitter applied to the MRT line side receive input DI1 (pin 29), the MRT properly recovers clock, decodes the HDB3, and outputs error-free NRZ data over (and beyond) the CCITT specified jitter input and frequency ranges. Performance characteristics are shown below in Figure 15 (34.368 Mbit/s operation) and Figure 16 (8.448 Mbit/s operation).

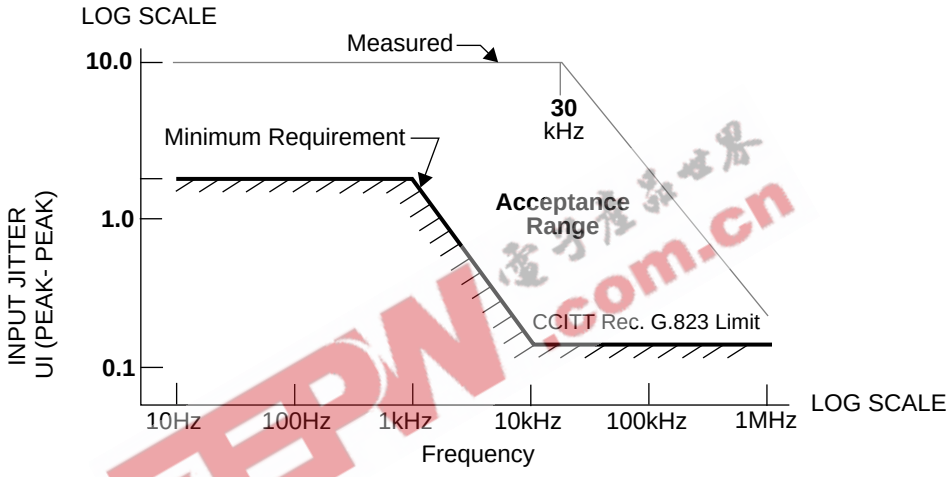


Figure 15. MRT Jitter Tolerance at34.368 Mbit/s (V_{DD} = 5V, T_A = 25°C)

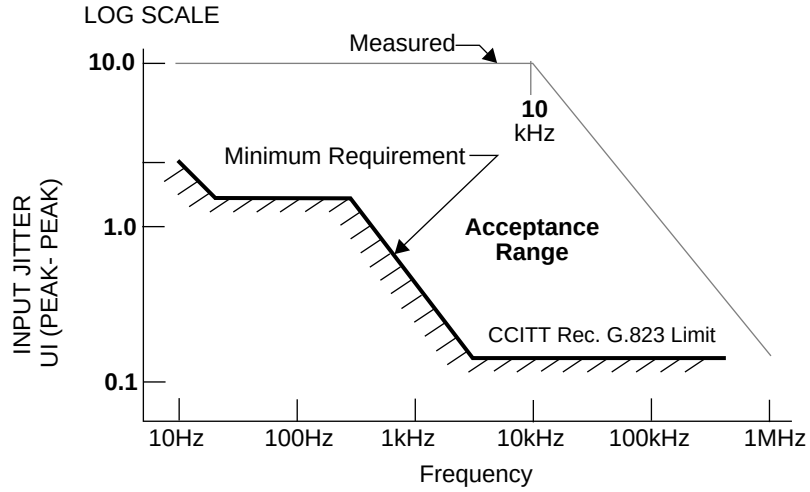


Figure 16. MRT Jitter Tolerance at 8.448 Mbit/s (V_{DD} = 5V, T_A = 25°C)

Maximum Output Jitter In Absence of Input Jitter

CCITT Recommendation G.823 specifies that it is necessary to restrict the amount of jitter generated by individual equipments. The actual limits depend on the type of equipment (and application).

In the absence of applied jitter, the receive path of the MRT introduces a maximum 0.05 Unit Intervals (UIs) peak-to-peak jitter over the following frequency ranges:

At 8.448 Mbit/s: 20 Hz to 400 kHz

At 34.368 Mbit/s: 100 Hz to 800 kHz

This operation is with the MRT terminated by the external components (and component values) specified in the Pin Description Table for pin 7 (VCOC), pin 17 (PLLC), and pin 22 (AGFIL).

Jitter Transfer

Transfer of jitter through an individual equipment is characterized by the relationship between the applied input jitter and the resulting output jitter as a function of frequency. CCITT Recommendation G.823 specifies that it is important to restrict jitter gain.

With applied input jitter at the MRT receive terminals, the maximum MRT output jitter is not greater than the level of input jitter plus 0.05 UI peak-to-peak jitter.

This operation is over the same CCITT specified frequency ranges and MRT external terminations as described in the above Maximum Output Jitter section.

Interfering Tone Tolerance

The MRT will properly recover clock and present error-free output to the receive terminal side interface in the presence of a PRBS interfering tone with the same data sequence as the data input for the following line rates:

Table 3. Interfering Tone Tolerance

Data Rate (Mbit/s)	Tone Rate (Mbit/s)	Maximum Tone Level	Data Sequence
34.368	34.368 ± 100ppm	-18 dB	2^{23}-1
8.448	8.448 ± 100ppm	-4 dB	2^{15} - 1
6.312	6.312 ± 100ppm	-4 dB	2^{15} - 1

*PRBS = Pseudo-Random Binary Sequence

PACKAGING

The MRT device is packaged in a 44-pin plastic leaded chip carrier suitable for socket or surface mounting. All dimensions shown are in inches and are nominal unless otherwise noted.

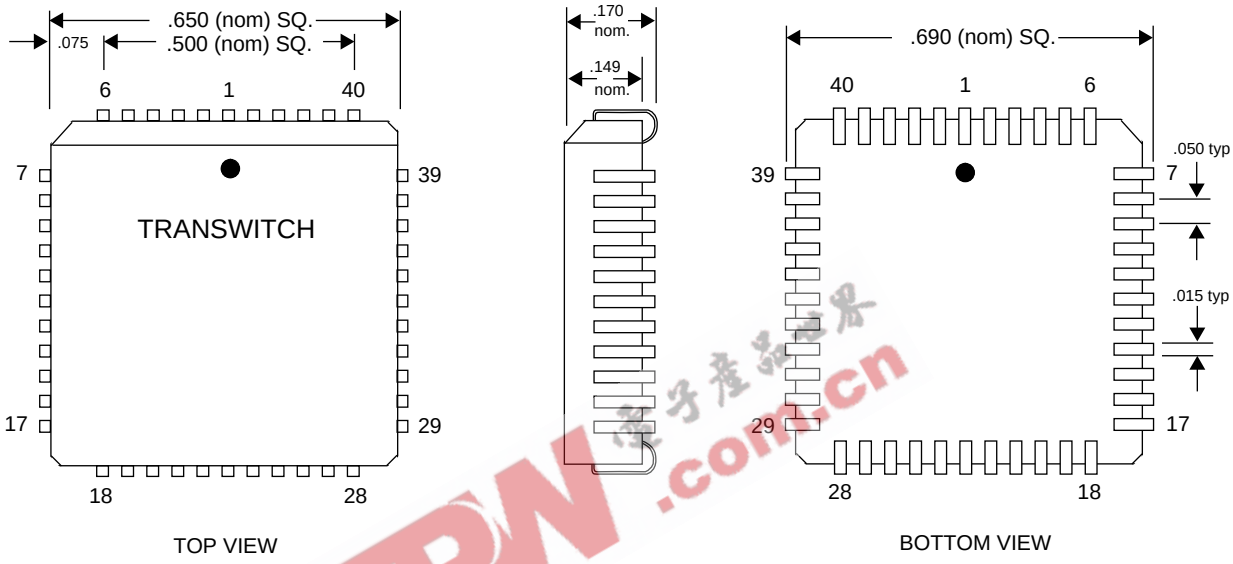


Figure 17. MRT 44-Pin Plastic Leaded Chip Carrier

ORDERING INFORMATION

Part Number:	TXC-02050-AIPL	44-pin Plastic Leaded Chip Carrier

RELATED PRODUCTS

TXC-03701 E2/E3F Framer VLSI device. The E2/E3 Framer directly interfaces with the MRT and provides multi-mode framing for CCITT G.751/G.753 (34368 kbit/s) or CCITT G.742/ G.745 (8448 kbit/s) signals.

TXC-03702 JT2F Framer VLSI device. The JT2F Framer directly interfaces with the MRT and provides framing for CCITT G.704 (6312 kbit/s) signals.

TXC-21055 MRT Evaluation Board. A complete ready-to-use single board that demonstrates the functions and features of the MRT line interface VLSI device.

STANDARDS DOCUMENTATION SOURCES

Telecommunication technical standards and reference documentation may be obtain from the following organizations:

ANSI (U.S.A.):

American National Standards Institute (ANSI)
11 West 42nd Street
New York, New York 10036

Tel: 212-642-4900
Fax: 212-302-1286

Bellcore (U.S.A.):

Bellcore
Attention - Customer Service
8 Corporate Place
Piscataway, NJ 08854

Tel: 800-521-CORE (In U.S.A.)
Tel: 908-699-5800
Fax: 908-336-2559

CCITT:

Publication Services of ITU
Place des Nations
CH 1211
Geneve 20, Switzerland

Tel: 41-22-730-5285
Fax: 41-22-730-5991

TTC (Japan):

TTC Standard Publishing Group of the
Telecommunications Technology Committee
2nd Floor, Hamamatsucho - Suzuki Building,
1 2-11, Hamamatsu-cho, Minato-ku, Tokyo

Tel: 81-3-3432-1551
Fax: 81-3-3432-1553

LIST OF DATA SHEET CHANGES

This change list identifies those areas within the updated MRT Data Sheet that have technical differences relative to the superseded MRT Data Sheet:

Updated MRT Data Sheet:	Edition 3, April 1994
Superseded MRT Data Sheet:	Edition 2, February 1992

The page numbers indicated below of the updated data sheet include changes relative to the superseded data sheet.

Page Number of Updated Data Sheet	Summary of the Change
All	Changed edition number and date on all pages.
All	Removed “Preliminary” designation.
2	Changed direction of DI2 pin in Figure 1, Block Diagram.
2-3	Made minor edits to Block Diagram Description.
4	Replaced description of pin 30, DI2.
5	Edited descriptions of pins 5 (LQLTY) and 38 (CLKI).
6	Made minor edits to descriptions of pins 4 (BERCK), 24 ($\overline{\text{LBKRX}}$) and 25 ($\overline{\text{LBKTX}}$). Also added Note 1 at bottom of page.
7	Added value for f in description of pins 27 and 28 (EQB1 and EQB0), and replaced description of pin 7 (VCOC).
8	Added values to first row of Thermal Characteristics table and removed second row.
11-12	Made minor clarifications to second paragraph of text and to Figures 3, 4, and 5.
13	Deleted Note 3 below Figure 7.
14	Deleted Note 3 below Figure 9.
15	Made minor changes to Figure 10.
16	Added two sentences to Line Side Input Circuit text.
17	Made minor edits to Figure 13 and to the paragraph of text below it.
17	Made minor changes to Figure 14.
18	Added Jitter Generation paragraph.
18	Changed Jitter Transfer text at bottom of page.
19	Changed Interfering Tone Tolerance text, added the Data Sequence column to Table 3, and removed Table 4.
20	Removed ceramic packaging diagram and added measurements to Figure 17, plastic packaging diagram.
22	Added Standards Documentation Sources.

- NOTES -

- NOTES -

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