WM8746

24-bit, 192kHz 6-Channel DAC with Volume Control

DESCRIPTION

WM8746 is a high performance 6-channel DAC designed for audio applications such as DVD, home theatre systems, and digital TV. The WM8746 supports data input word lengths from 16 to 32-bits and sampling rates up to 192kHz. The WM8746 can convert up to 6 channels at sample rates from 8 to 192kHz. Additionally WM8746 supports 2 channels at 192kHz and 4 channels at 96kHz simultaneously.

The WM8746 consists of a serial interface port, digital interpolation filters, multi-bit sigma delta modulators and 6 DACs in a small 28-pin SSOP package. The WM8746 also includes a digitally controllable mute and attenuator function on each channel.

The WM8746 supports a variety of connection schemes for audio DAC control. The serial control interface provides access to a wide range of features including on-chip mute, attenuation and phase reversal. A hardware controllable interface is also available. It is pin-compatible with the WM8736, (apart from RSTB pin which is typically unused).

The WM8746 is an ideal device to interface to AC-3™, DTS™, and MPEG audio decoders for surround sound applications, or for use in "universal" high definition audio players supporting DVD-A formats.

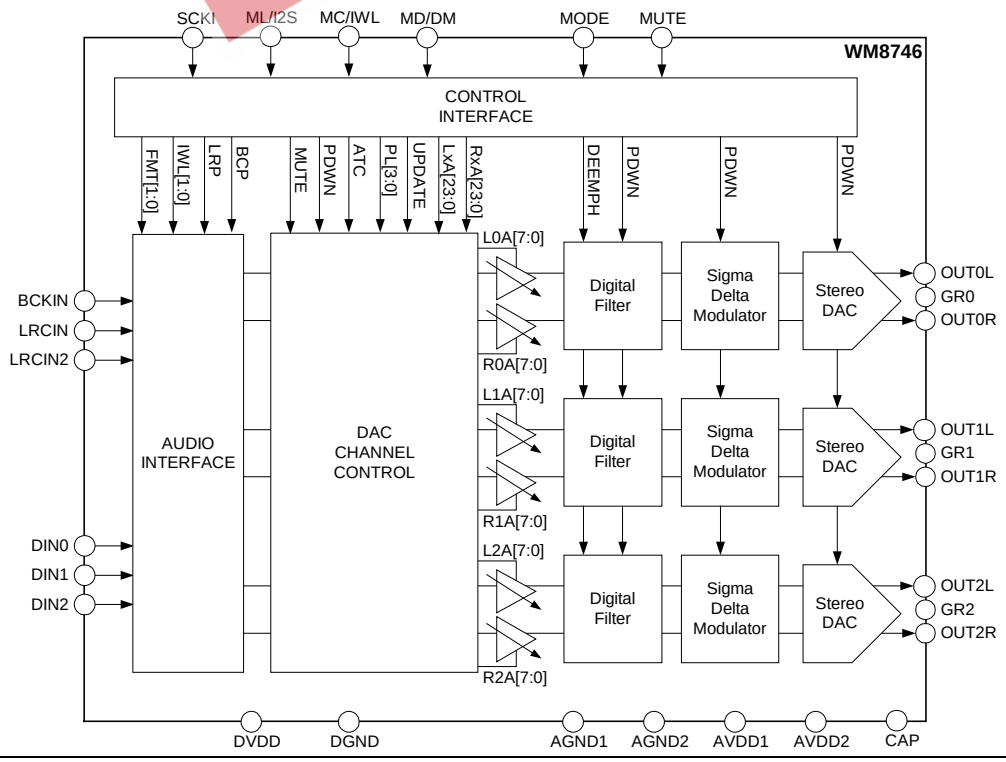
FEATURES

- 6-Channel DAC
- Audio Performance
  - 106dB SNR ('A' weighted @ 48kHz) DAC
  - -96dB THD
- DAC Sampling Frequency: 8kHz – 192kHz
- 3-Wire Serial Control Interface
- Programmable Audio Data Interface Modes
  - I^2S, Left, Right Justified or DSP
  - 16/20/24/32 bit Word Lengths
- Independent Digital Volume Control on Each Channel with 127.5dB Range in 0.5dB Steps
- 3.0V – 5.5V Supply Operation
- 28-Pin SSOP Package
- Exceeds Dolby Class A Performance Requirements
- Pin Compatible with WM8736

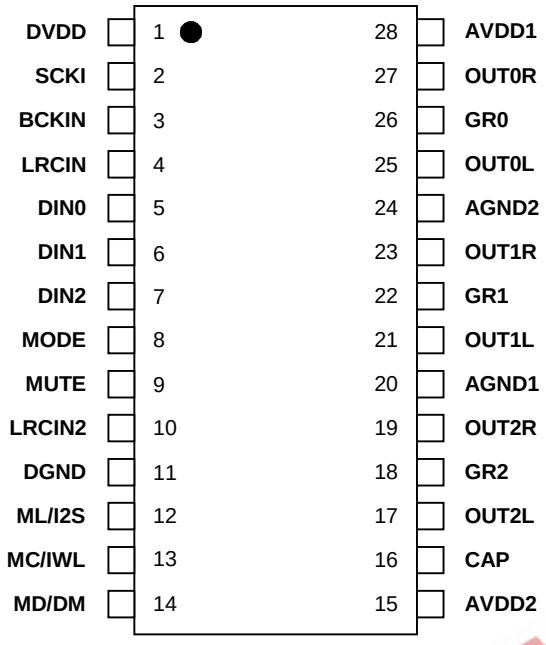
APPLICATIONS

- DVD and DVD 'Universal' Players
- Home theatre systems
- Digital broadcast receivers

BLOCK DIAGRAM



PIN CONFIGURATION



ORDERING INFORMATION

DEVICE	TEMP. RANGE	PACKAGE
WM8746EDS	-25 to +85°C	28-pin SSOP

PIN DESCRIPTION

PIN	NAME	TYPE	DESCRIPTION
1	DVDD	Supply	Digital Positive Supply.
2	SCKI	Digital input	System Clock Input
3	BCKIN	Digital input	Audio Data Bit Clock Input.
4	LRCIN	Digital input	DAC Sample Rate Clock Input
5	DIN0	Digital input	Channel 0 Serial Audio Data Input.
6	DIN1	Digital input	Channel 1 Serial Audio Data Input.
7	DIN2	Digital input	Channel 2 Serial Audio Data Input.
8	MODE	Digital input Internal pull-up	Control Method Selection Pin. Low = Software Mode High = Hardware Control Mode
9	MUTE	Digital bidirectional	Mute Control Pin in PCM Mode. **Input** / **Output** Low: Not Mute / Low: Mute Off High: Mute / High: Mute On (Zero Flag) Z: Automute
10	LRCIN2	Digital input Internal pull-down	2nd LRCIN for use in mixed 192kHz/96kHz operation (bit 2SPD = 'hi')
11	DGND	Supply	Digital GND
12	ML/I2S	Digital input Internal pull-up	Software mode: 3-Wire Serial Control Latch Hardware Mode: Input Format Selection:
13	MC/IWL	Digital input Internal pull-up	Software Mode: 3-Wire Serial Control Clock Input Hardware mode: Input Word Length Selection:
14	MD/DM	Digital input	Software mode: 3-Wire Serial Control Data Input Hardware mode: De-emphasis selection
15	AVDD2	Supply	Analogue Positive DAC Reference
16	CAP	Analogue output	Analogue Internal Mid-Rail Reference De-Coupling Point
17	OUT2L	Analogue output	Left Channel 2 Output.
18	GR2	Analogue input	Channel 2 Negative Reference.
19	OUT2R	Analogue output	Right Channel 2 Output.
20	AGND1	Supply	Analogue GND
21	OUT1L	Analogue output	Left Channel 1 Output.
22	GR1	Analogue input	Channel 1 Negative Reference.
23	OUT1R	Analogue output	Right Channel 1 Output.
24	AGND2	Supply	Analogue GND
25	OUT0L	Analogue output	Left Channel 0 Output.
26	GR0	Analogue input	Channel 0 Negative Reference.
27	OUT0R	Analogue output	Right Channel 0 Output.
28	AVDD1	Supply	Analogue VDD

Notes

1. Digital input pins have Schmitt trigger input buffers

ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings are stress ratings only. Permanent damage to the device may be caused by continuously operating at or beyond these limits. Device functional operating limits and guaranteed performance specifications are given under Electrical Characteristics at the test conditions specified.

ESD Sensitive Device. This device is manufactured on a CMOS process. It is therefore generically susceptible to damage from excessive static voltages. Proper ESD precautions must be taken during handling and storage of this device.

CONDITION	MIN	MAX
Digital supply voltage	-0.3V	+7V
Analogue supply voltage	-0.3V	+7V
Voltage range digital inputs	DGND -0.3V	DVDD +0.3V
Voltage range analogue inputs	AGND -0.3V	AVDD +0.3V
Master Clock Frequency		37MHz
Operating temperature range, T_A	-25°C	+85°C
Storage temperature prior to soldering	30°C max / 85% RH max	
Storage temperature after soldering	-65°C	+150°C
Package body temperature (soldering 10 seconds)		+240°C
Package body (soldering 2 minutes)		+183°C

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Digital supply range	DVDD		3.0		5.5	V
Analogue supply range	AVDD1, AVDD2		3.0		5.5	V
Ground	AGND, GR, DGND			0		V
Difference DGND to AGND			-0.3	0	+0.3	V
Analogue supply current		AVDD = 5V		58		mA
Digital supply current		DVDD = 5V		22		mA
Analogue supply current		AVDD = 3.3V		57		mA
Digital supply current		DVDD = 3.3V		11		mA
Analogue supply current		Power down, stop clock		0.4		mA
Digital supply current		Power down, stop clock		0.09		mA

Note:

1. The digital supply voltages must not exceed the analogue supply voltages.

AC ELECTRICAL CHARACTERISTICS

Test Conditions

AVDD = DVDD = 3V, AGND = 0V = DGND = 0V, T_A = +25°C, fs = 48kHz, SCKI = 256fs unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Digital Logic Levels (TTL Levels)						
Input LOW level	V_{IL}				0.8	V
Input HIGH level	V_{IH}		2.0			V
Output LOW	V_{OL}	I_{OL} = 2mA			0.4	V
Output HIGH	V_{OH}	I_{OH} = 2mA	2.4			V
Analogue Reference Levels						
Reference voltage	V_{CAP}			AVDD2-GR2 /2		V
Potential divider resistance	R_{CAP}			25K		Ohms
DAC Output (Load = 10K ohms. 50pF)						
0dBFs Full scale output voltage		At DAC outputs		1.1 x AVDD1/5		V_{rms}
SNR (Note 1,2,3)		A-weighted, @ fs = 48kHz	100	106		dB
SNR (Note 1,2,3)		A-weighted @ fs = 96kHz	98	105		dB
SNR (Note 1,2,3)		A-weighted @ fs = 192kHz		105		dB
SNR (Note 1,2,3)		A-weighted, @ fs = 48kHz AVDD=DVDD=3.3V		103		dB
SNR (Note 1,2,3)		A-weighted @ fs = 96kHz AVDD=DVDD=3.3V		103		dB
SNR (Note 1,2,3)		Non 'A' weighted @ fs = 48kHz AVDD=DVDD=5V		103		dB
THD (Note 1,2,3)		1kHz, 0dBFs	-90	-95		dB
THD+N (Dynamic range, Note 2)		1kHz, -60dBFs	-100	-106		dB
DAC channel separation				<95		dB

Test Conditions

AVDD = DVDD = 3V, AGND = 0V = DGND = 0V, T_A = +25°C, fs = 48kHz, SCKI = 256fs unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Analogue Output Levels						
Output level		Load = 10kOhms, 0 dBFS, (AVDD=5.0V)		1.1		V_{rms}
		Load = 10kOhms, 0 dBFS, (AVDD=3.3V)		0.73		
Gain mismatch channel-to-channel				±1		%FSR
Minimum resistance load		To midrail or a.c. coupled		1		kOhms
		To midrail or a.c. coupled (AVDD = 3.3V)		1		kOhms
Maximum capacitance load		5V or 3.3V		100		pF
Output d.c. level				AVDD1-AGND/2		V
Power On Reset (POR)						
POR threshold				2.0		V

Notes:

1. Ratio of output level with 1kHz full scale input, to the output level with all zeros into the digital input, measured 'A' weighted over a 20Hz to 20kHz bandwidth.
2. All performance measurements done with 20kHz low pass filter, and where noted an A-weight filter. Failure to use such a filter will result in higher THD+N and lower SNR and Dynamic Range readings than are found in the Electrical Characteristics. The low pass filter removes out of band noise; although it is not audible it may affect dynamic specification values.
3. CAP decoupled with 10uF and 0.1uF capacitors (smaller values may result in reduced performance).

TERMINOLOGY

1. Signal-to-noise ratio (dB) - SNR is a measure of the difference in level between the full scale output and the output with no signal applied. (No Auto-zero or Automute function is employed in achieving these results).
2. Dynamic range (dB) - DNR is a measure of the difference between the highest and lowest portions of a signal. Normally a THD+N measurement at 60dB below full scale. The measured signal is then corrected by adding the 60dB to it. (e.g. THD+N @ -60dB= -32dB, DR= 92dB).
3. THD+N (dB) - THD+N is a ratio, of the rms values, of (Noise + Distortion)/Signal.
4. Stop band attenuation (dB) - Is the degree to which the frequency spectrum is attenuated (outside audio band).
5. Channel Separation (dB) - Also known as Cross-Talk. This is a measure of the amount one channel is isolated from the other. Normally measured by sending a full scale signal down one channel and measuring the other.
6. Pass-Band Ripple - Any variation of the frequency response in the pass-band region.

MASTER CLOCK TIMING

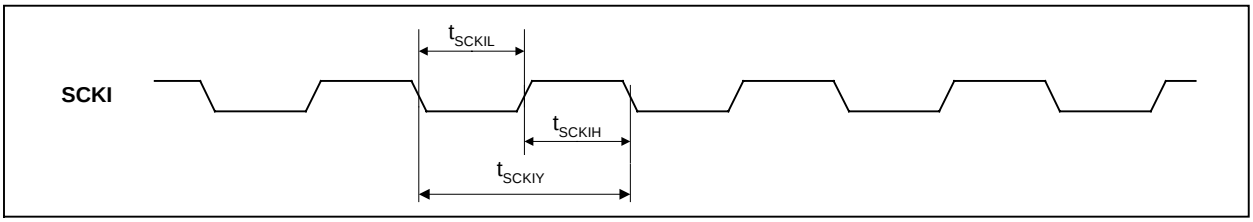


Figure 1 Master Clock Timing Requirements

Test Conditions

AVDD = DVDD = 5V, AGND = GR = DGND = 0V, T_A = +25°C, fs = 48kHz, SCKI = 256fs unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
System Clock Timing Information						
SCKI System clock pulse width high	t_{SCKIH}		13			ns
SCKI System clock pulse width low	t_{SCKIL}		13			ns
SCKI System clock cycle time	t_{SCKIY}		26			ns
SCKI Duty cycle			40:60		60:40	

Table 1 Master Clock Timing Requirements

DIGITAL AUDIO INTERFACE TIMING

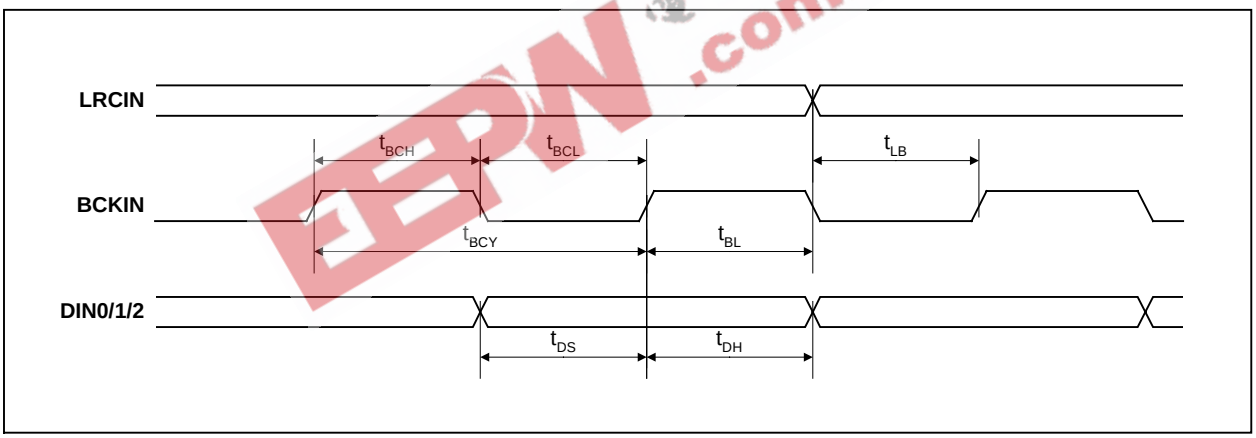


Figure 2 PCM Digital Audio Data Timing

Test Conditions

AVDD = DVDD = 5V, AGND = GR = DGND = 0V, T_A = +25°C, fs = 48kHz, SCKI = 256fs unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Audio Data Input Timing Information						
BCKIN cycle time	t_{BCY}		40			ns
BCKIN pulse width high	t_{BCH}		16			ns
BCKIN pulse width low	t_{BCL}		16			ns
LRCIN set-up time to BCKIN rising edge	t_{LB}		8			ns
LRCIN hold time from BCKIN rising edge	t_{BL}		8			ns
DIN0/1/2 set-up time to BCKIN rising edge	t_{DS}		8			ns
DIN0/1/2 hold time from BCKIN rising edge	t_{DH}		8			ns

Table 2 PCM Digital Audio Timing

DIGITAL CONTROL INTERFACE

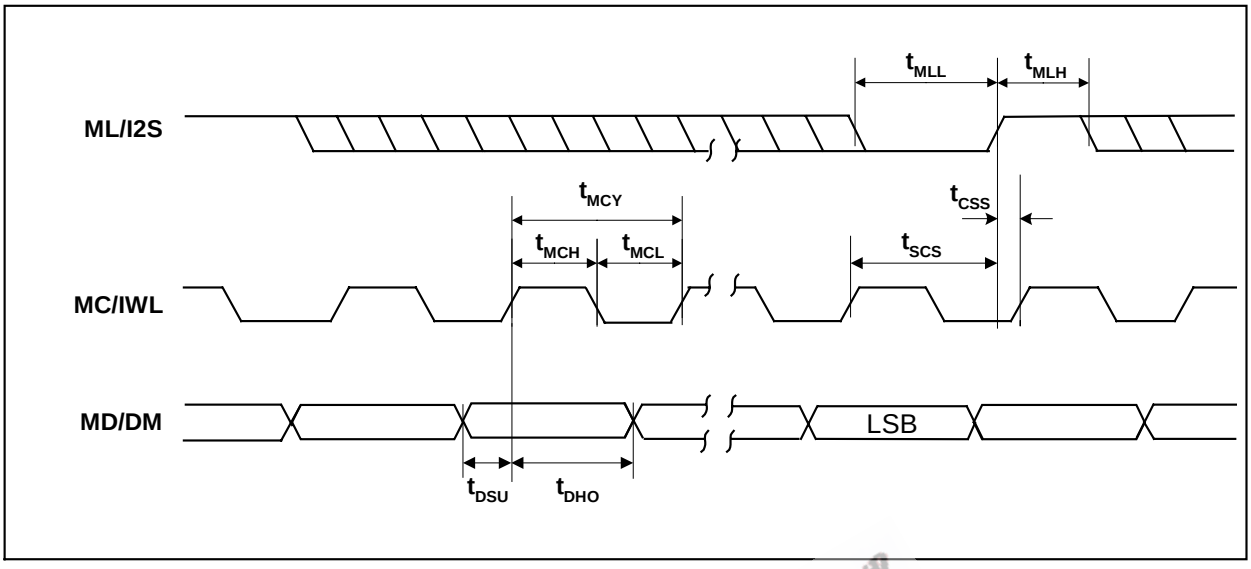


Figure 3 Control Interface Input Timing: 3-Wire Serial Control Mode

Test Conditions
AVDD = DVDD = 5V, AGND = GR = DGND = 0V, T_A = +25°C, fs = 48kHz, SCKI = 256fs unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Program Register Input Information						
MC/IWL rising edge to ML/I2S rising edge	t_{SCS}		20			ns
MC/IWL pulse cycle time	t_{MCY}		80			ns
MC/IWL pulse width low	t_{MCL}		30			ns
MC/IWL pulse width high	t_{MCH}		30			ns
MD/DM to MC/IWL set-up time	t_{DSU}		20			ns
MC/IWL to MD/DM hold time	t_{DHO}		20			ns
ML/I2S pulse width low	t_{MLL}		20			ns
ML/I2S pulse width high	t_{MLH}		20			ns
ML/I2S rising to MC/IWL rising	t_{CSS}		20			ns

Table 3 Control Interface Input Timing Information: 3-Wire Serial Control Mode

DEVICE DESCRIPTION

INTRODUCTION

WM8746 is a complete 6-channel stereo audio digital-to-analogue converter, including digital interpolation filter, multi-bit sigma delta with dither, and switched capacitor multi-bit stereo DAC and output smoothing filters.

The device is implemented as three separate stereo DACs in a single package and controlled by a single interface. Each DAC has its own data input DIN0/1/2, and LRCIN, BCKIN and SCKI are shared between them. An additional LRCIN2 input is provided to allow for the front channels in a surround system to be run at higher sample rate than the other 4 channels (ie. 192kHz for front channels and 96kHz). In this mode the same SCKI is used for all channels, the front channels being run at twice the over-sampling rate of the other channels.

Control of internal functionality of the device is by either hardware control (pin programmed) or software control (3-wire serial control interface). The MODE pin selects between hardware and software control. In software control mode, an SPI type interface is used. This interface may be asynchronous to the audio data interface. Control data will be re-synchronised to the audio processing internally.

Operation using a system clock of 256fs, 384fs, 512fs or 768fs is provided, selection between clock rates being automatically detected. Sample rates (fs) from less than 8ks/s to 96ks/s are allowed, provided the appropriate system clock is input. Support is also provided for up to 192ks/s using a system clock of 128fs or 192fs.

The audio data interface supports right, left and I^{2}S (Philips left justified, one bit delayed) interface formats along with a highly flexible DSP serial port interface. When in hardware mode, the three serial interface pins become control pins to allow selection of input data format type (I^{2}S or right justified), input word length (16, 20, 24, or 32-bit) and de-emphasis functions.

AUDIO DATA SAMPLING RATES

In a typical digital audio system there is only one central clock source producing a reference clock to which all audio data processing is synchronised. This clock is often referred to as the audio system's Master Clock. The external master system clock can be applied directly through the SCKI input pin with no software configuration necessary. Note that on the WM8746, SCKI is used to derive clocks for the DAC path. The DAC path consists of DAC sampling clock, DAC digital filter clock and DAC digital audio interface timing. In a system where there are a number of possible sources for the reference clock it is recommended that the clock source with the lowest jitter be used to optimise the performance of the DAC.

The system clock for WM8746 supports audio sampling rates from 128fs to 768fs, where fs is the audio sampling frequency (LRCIN) typically 32kHz, 44.1kHz, 48kHz, 96kHz or 192kHz. The system clock is used to operate the digital filters and the noise shaping circuits.

The WM8746 has a system clock detection circuit that automatically determines the relationship between the system clock frequency and the sampling rate (to within +/- 32 system clocks). If greater than 32 clocks error, the interface defaults to 768fs and maintains the output level at the last sample. The system clock should be synchronised with LRCIN, although the WM8746 is tolerant of phase differences or jitter on this clock. Table 4 shows the typical system clock frequency inputs for the WM8746.

SAMPLING RATE (FS) (LRCIN)	SYSTEM CLOCK FREQUENCY (MHZ)					
	128fs	192fs	256fs	384fs	512fs	768fs
32kHz	4.096	6.144	8.192	12.288	16.384	24.576
44.1kHz	5.6448	8.467	11.2896	16.9340	22.5792	33.8688
48kHz	6.144	9.216	12.288	18.432	24.576	36.864
96kHz	12.288	18.432	24.576	36.864	Unavailable	Unavailable
192kHz	24.576	36.864	Unavailable	Unavailable	Unavailable	Unavailable

Table 4 System Clock Frequencies Versus Sampling Rate

DIGITAL AUDIO INTERFACE

Audio data is applied to the internal DAC filters via the Digital Audio Interface. Five popular interface formats are supported:

- Left Justified mode
- Right Justified mode
- I^2S mode
- DSP Early mode
- DSP Late mode

All 5 formats send the MSB first and support word lengths of 16, 20, 24 and 32 bits, except right justified that does not support 32 bit data. DIN0/1/2 and LRCIN are sampled on the rising, or falling edge of BCKIN.

In left justified, right justified and I^2S modes, the digital audio interface receives data on the DIN0/1/2 inputs. Audio Data for each stereo channel is time multiplexed with LRCIN indicating whether the left or right channel is present. LRCIN is also used as a timing reference to indicate the beginning or end of the data words.

In left justified, right justified and I^2S modes, the minimum number of BCKINs per LRCIN period is twice the selected word length. LRCIN must be high for at least the word length number of BCKINs and low for at least the same. Any mark to space ratio on LRCIN is acceptable provided the above requirements are met. The WM8746 will automatically detect when data with a LRCIN period of exactly 32 is sent, and select 16 bit mode - overriding any previously programmed word length. Word length will revert to the previously programmed value if a LRCIN period other than 32 is detected.

In DSP early or DSP late mode, all 6 channels are time multiplexed onto DIN0. LRCIN is used as a frame sync signal to identify the MSB of the first word. The minimum number of BCKINs per LRCIN period is 6 times the selected word length. Any mark to space ratio is acceptable on LRCIN provided the rising edge is correctly positioned. (see Figure 7, Figure 8)

LEFT JUSTIFIED MODE

In left justified mode, the MSB is sampled on the first rising edge of BCKIN following a LRCIN transition. LRCIN is high during the left samples and low during the right samples.

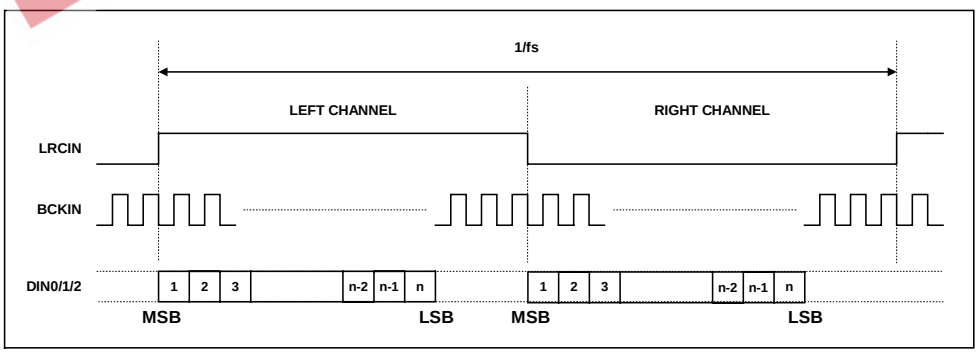


Figure 4 Left Justified Mode TIming Diagram

RIGHT JUSTIFIED MODE

In right justified mode, the LSB is sampled on the rising edge of BCKIN preceding a LRCIN transition. LRCIN is high during the left samples and low during the right samples.

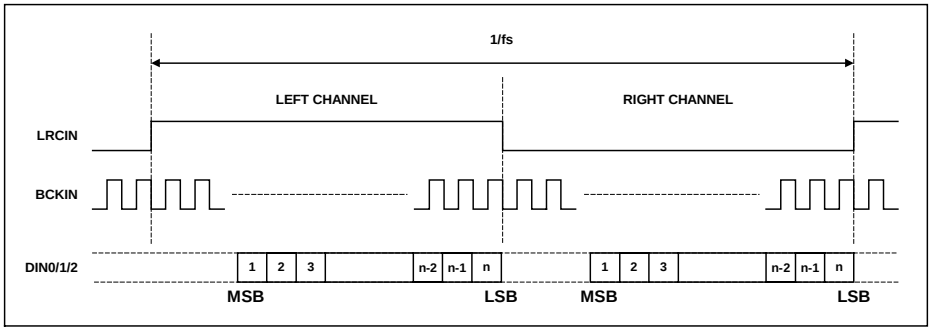


Figure 5 Right Justified Mode TIming Diagram

I²S MODE

In I²S mode, the MSB is sampled on the second rising edge of BCKIN following a LRCIN transition. LRCIN is low during the left samples and high during the right samples.

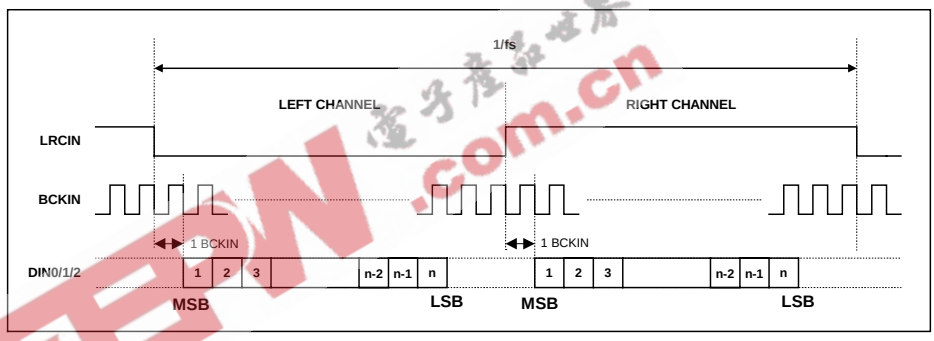


Figure 6 I²S Mode TIming Diagram

DSP EARLY MODE

In DSP early mode, the first bit is sampled on the BCKIN edge following the one which detects a low to high transition on LRCIN.

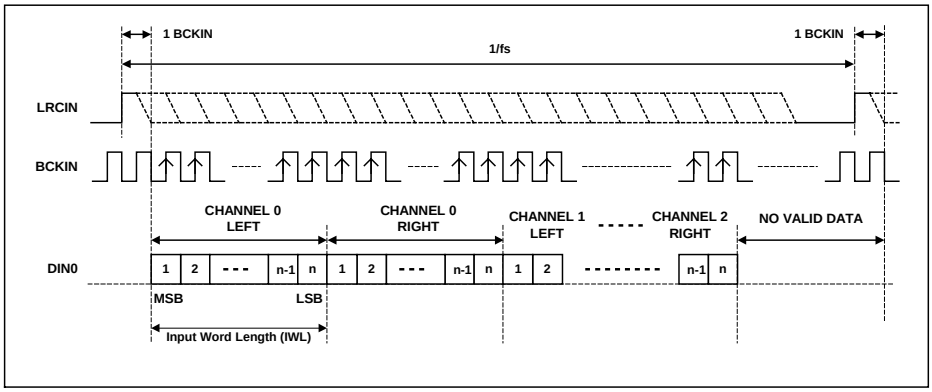


Figure 7 DSP Early Mode Timing Diagram

DSP LATE MODE

In DSP late mode, the first bit is sampled on the BCKIN edge which detects a low to high transition on LRCIN.

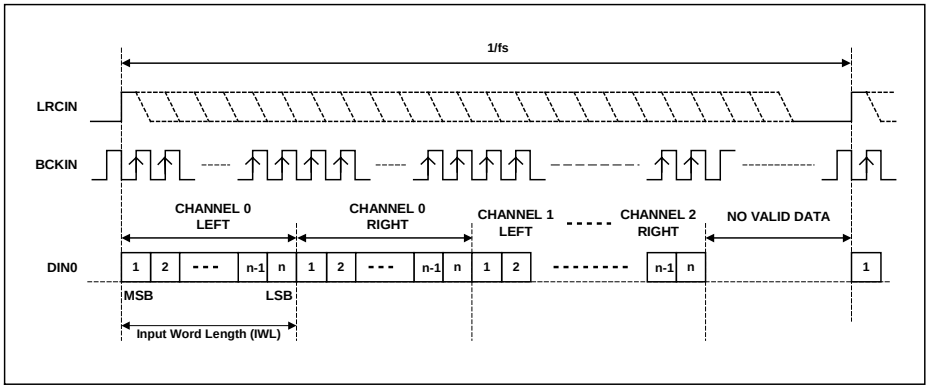


Figure 8 DSP Late Mode Timing Diagram

In both early and late DSP modes, DAC0 left is always sent first, followed immediately by data words for the other 5 channels. No BCKIN edges are allowed between the data words. The word order is DAC0 left, DAC0 right, DAC1 left, DAC1 right, DAC2 left, DAC2 right.

SPLIT RATE MODE

The WM8746 can be used with differing sample rates on the front and rear channels. This allows extremely high quality audio to be played on the front two channels whilst the other channels use normal high quality data streams.

This mode will only work with a front data rate of 192kHz and a rear rate of 96kHz but can be used with all the normal data formats **except** the two DSP modes and with the system at either 128fs or 192fs see Table 4.

When running in split rate mode all the channels are clocked in using a common BCKIN; the front channels using LRCIN and all the other channels using LRCIN2 see Figure 9.

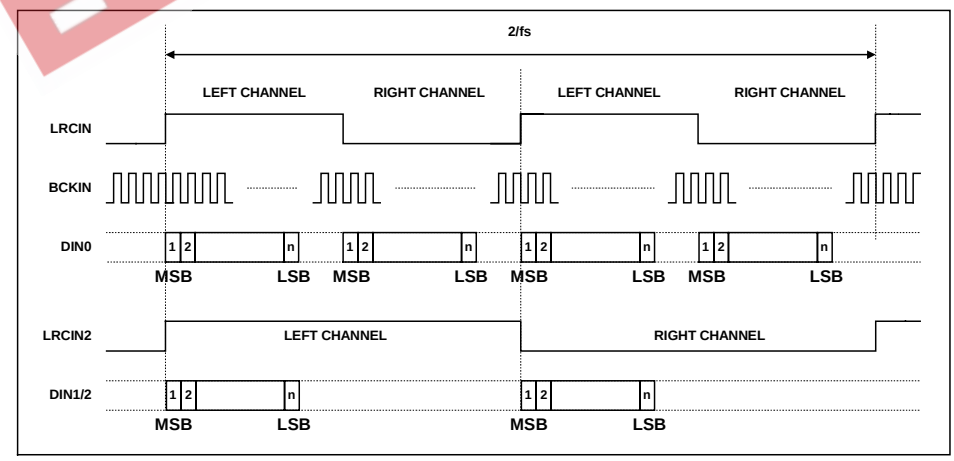


Figure 9 Split Rate Audio Mode Timing Diagram

Notes:

1. Figure 9 shows the timing for left justified however this is similar for right justified and I^2S.

2. The edges of LRCIN and LRCIN2 **must** be coincidental.

MODES OF OPERATION

Control of the various modes of operation for the WM8746 is either by software control over the serial interface ,or by hard-wired pin control. Selection of software or hardware mode is via the MODE pin. The following functions may be controlled either via the serial control interface or by hard wiring of the appropriate pins.

FUNCTION		SOFTWARE CONTROL DEFAULT VALUE PIN 8: MODE = 0	HARDWARE CONTROL BEHAVIOUR PIN 8: MODE = 1
	OPTIONS		
Input audio data format	Right justified Left justified I^2S format DSP formats	FMT = 00 (default) FMT = 01 FMT = 10 FMT = 11	Pin 12, 13: ML/I2S, MC/IWL = 00, 01 or 10 Not available in hardware mode Pin 12, 13: ML/I2S, MC/IWL = 11 Not available in hardware mode
Input word length	16 20 24 32	IWL[1:0] = 00 IWL[1:0] = 01 IWL[1:0] = 10 (default) IWL[1:0] = 11	Pin 12, 13: ML/I2S, MC/IWL = 00 (RJ) Pin 12, 13: ML/I2S, MC/IWL = 01 (RJ) Pin 12, 13: ML/I2S, MC/IWL = 10 (RJ) Pin 12, 13: ML/I2S, MC/IWL = 11 (I^2S)
De-emphasis selection	On Off	DEEMPH = 1 DEEMPH = 0 (Default)	Pin 14: MD/DM = 1 Pin 14: MD/DM = 0
Mute	On Off	MUTE = 1 MUTE = 0 (default)	Pin 9: MUTE = 1 Pin 9: MUTE = 0
Input LRCIN polarity	Normal Inverted	LRP = 0 (default) LRP = 1	Not available in hardware mode, default value set
Volume control	Lch, Rch individually Lch, Rch common	ATC = 0; 0dB (default) ATC = 1	Not available in hardware mode, gain defaults to 0dB
Infinite zero detect	On Off	IZD = 1 IZD = 0 (default)	Automute function controlled from MUTE pin low = never mute floating = automute enable high = mute
Power down	Chip on Chip off	PWDN = 0 (default) PWDN = 1	Run SCKI Stop SCKI
DAC output control	See Table 6 for all options	Default is PL[3:0] = 1001, stereo mode	Not available in hardware mode

Table 5 Control Function Summary

SOFTWARE CONTROL MODES

DIGITAL AUDIO INTERFACE CONTROL REGISTERS

Interface format is selected via the FMT[1:0] register bits:

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
0000011 Interface Control	1:0	FMT[1:0]	00	Interface format Select 00 : right justified mode 01: left justified mode 10: I^2S mode 11: DSP (early or late) mode

In left justified, right justified or I^2S modes, the LRP register bit controls the polarity of LRCIN. If this bit is set high, the expected polarity of LRCIN will be the opposite of that shown Figure 4, Figure 5 and Figure 6. Note that if this feature is used as a means of swapping the left and right channels, a 1 sample phase difference will be introduced.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
0000011 Interface Control	2	LRP	0	LRCIN Polarity 0 : normal LRCIN polarity 1: inverted LRCIN polarity

In DSP modes, the LRCIN register bit is used to select between early and late modes:

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
0000011 Interface Control	2	LRP	0	DSP Format 0 : Early DSP mode 1: Late DSP mode

By default, LRCIN and DIN0/1/2 are sampled on the rising edge of BCKIN and should ideally change on the falling edge. Data sources which change LRCIN and DIN0/1/2 on the rising edge of BCKIN can be supported by setting the BCP register bit. Setting BCP to 1 inverts the polarity of BCKIN to the inverse of that shown in Figure 4, Figure 5, Figure 6, Figure 7 and Figure 8.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
0000011 Interface Control	3	BCP	0	BCKIN Polarity 0 : normal BCKIN polarity 1: inverted BCKIN polarity

The IWL[1:0] bits are used to control the input word length.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
0000011 Interface Control	5:4	IWL[1:0]	10	Input Word Length 00 : 16 bit data 01: 20 bit data 10: 24 bit data 11: 32 bit data

Note: If 32-bit mode is selected in right justified mode, the WM8746 defaults to 24 bits.

In all modes, the data is signed 2's complement. The digital filters always input 24-bit data. If the DAC is programmed to receive 16 or 20 bit data, the WM8746 pads the unused LSBs with zeros. If the DAC is programmed into 32 bit mode, the 8 LSBs are ignored.

The PHASE bits control the orientation of the data output of the three stereo channels. By default all the channels are non-inverting.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
0000011 Interface Control	8:6	PHASE	000	Output phase direction 1 in bit 6 reverses OUT0L/R. 1 in bit 7 reverses OUT1L/R. 1 in bit 8 reverses OUT2L/R.

MUTE MODES

Setting the MUTE register bit will apply a 'soft' mute to the input of the digital filters:

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
0000010 DAC Channel Control	0	MUTE	0	Soft Mute select 0 : Normal Operation 1: Soft mute all channels

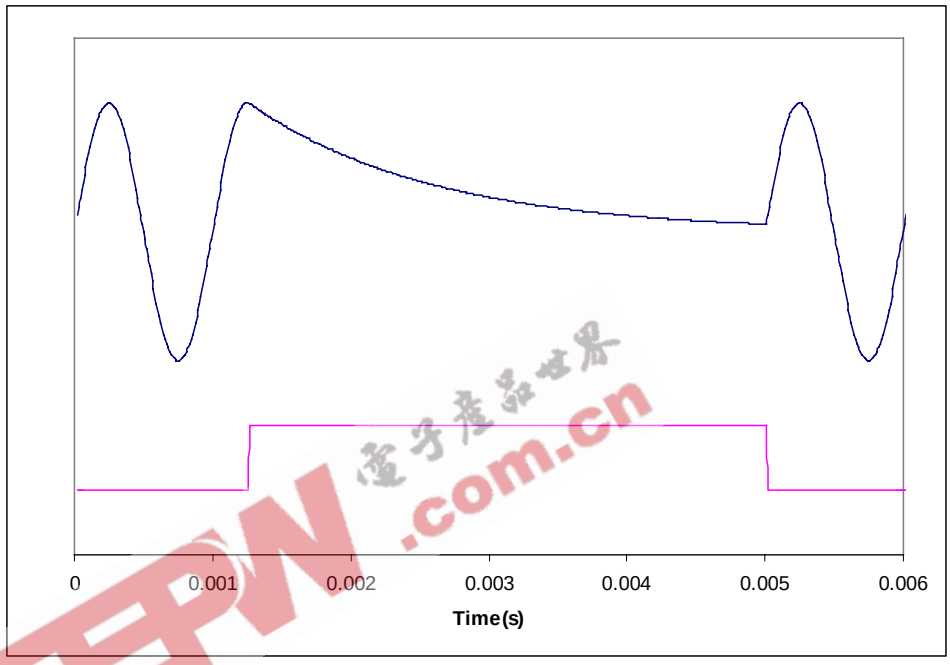


Figure 10 Application and Release of Soft Mute

Figure 10 shows the application and release of MUTE whilst a full amplitude sinusoid is being played at 48kHz sampling rate. When MUTE (lower trace) is asserted, the output (upper trace) begins to decay exponentially from the DC level of the last input sample. The output will decay towards V_{CAP} with a time constant of approximately 64 input samples. If MUTE is applied for 1024 or more input samples, the outputs will be connected directly to V_{CAP} - this feature can be disabled using the IZD (infinite zero detect) bit. When MUTE is de-asserted, the output will restart almost immediately from the current input sample.

Note that all other means of muting the DAC channels: setting the PL[3:0] bits to 0, setting the PWDN bit or setting attenuation to 0 will cause much more abrupt muting of the output.

Setting the IZD register bit will enable the infinite zero detect feature:

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
0000010 DAC Channel Control	4	IZD	0	Internal Analogue Mute Disable 0 : Disable Analogue Mute 1: Enable Analogue Mute

With IZD=1, applying MUTE for 1024 consecutive input samples will cause all outputs to be connected directly to V_{CAP}. This also happens if 2048 consecutive zero input samples are applied to all 6 channels, and IZD=0. It will be removed as soon as any channel receives a non-zero input.

The MUTE pin can be used as an input. In this case it performs the same function as the MUTE register bit. Driving the MUTE pin high will apply a 'soft' mute. Driving it low again, will remove the MUTE immediately. Note that this hardware mute feature doesn't require the MODE pin to be set high.

MUTE PIN	DESCRIPTION
0	Normal Operation
1	Mute all DAC channels
Floating	Enable IZD, Mute becomes an output to indicate when IZD occurs.

A diagram showing how the various Mute modes interact is shown below in Figure 11.

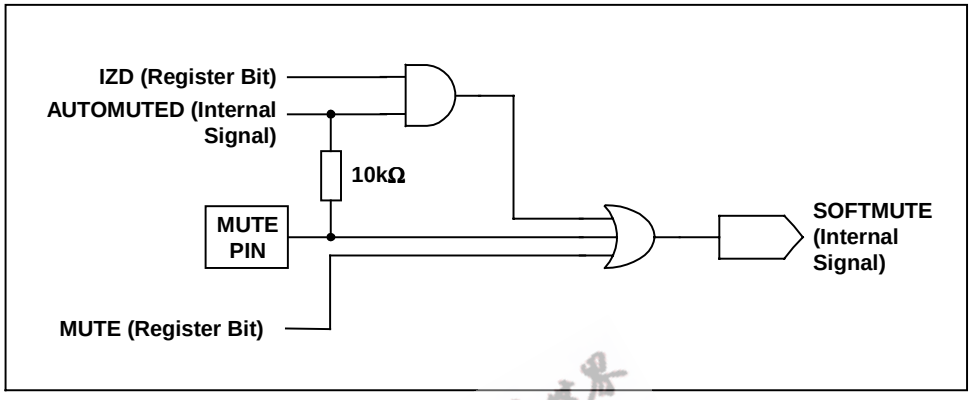


Figure 11 Selection Logic for MUTE Modes

The MUTE pin behaves as a bi-directional function, that is, as an input to select MUTE or NOT-MUTE, or as an output indication of automute operation. MUTE is active high; taking the pin high causes the filters to soft mute, ramping down the audio signal over a few milliseconds. Taking MUTE low again allows data into the filter.

The automute function detects a series of zero value audio samples of 1024 samples long being applied to all 6 channels. After such an event, a latch is set whose output (AUTOMUTED) is wire OR'ed through a 10kohm resistor to the MUTE pin. Thus if the MUTE pin is not being driven, the automute function will assert MUTE.

If MUTE is tied low, AUTOMUTED is overridden and will not mute. If MUTE is driven from a source follower, or diode, then both MUTE and automute functions are available. If MUTE is not driven, AUTOMUTED appears as a weak output (10k source impedance) so can be used to drive external mute circuits. The automute signal is AND'ed with IZD, this qualified mute signal then being OR'ed into the SOFTMUTE control. Therefore, in software mode, automute operation may be controlled with the IZD control bit.

DE-EMPHASIS MODE

Setting the DEEMPH register bit puts all the digital filters into de-emphasis mode:

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
0000010 DAC Channel Control	1	DEEMPH	0	De-emphasis mode select: 0 : Normal Mode 1: De-emphasis Mode

Refer to Figure 18 - Figure 23 for details of the De-Emphasis filtering effects at different sample rates.

In hardware mode (MODE=1) driving the MD/DM pin high has the same effect as setting the DEEMPH bit:

MODE PIN	MD/DM PIN	DESCRIPTION
0	ignored	De-Emphasis controlled from DEEMPH register bit
1	0	Normal Mode
1	1	De-Emphasis Mode

POWERDOWN MODE

Setting the PWDN register bit immediately connects all outputs to V_{CAP} and selects a low power mode. All trace of the previous input samples is removed, but all control register settings are preserved. When PWDN is cleared again the first 16 input samples will be ignored as the FIR will repeat it's power-on initialisation sequence.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
0000010 DAC Channel Control	2	PWDN	0	Power Down Mode Select: 0 : Normal Mode 1: Power Down Mode

ATTENUATOR CONTROL MODE

Setting the ATC register bit causes the left channel attenuation settings to be applied to both left and right channels for all three pairs of DACs from the next audio input sample. No update to the attenuation registers is required for ATC to take effect.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
0000010 DAC Channel Control	3	ATC	0	Attenuator Control Mode: 0 : Right channels use Right attenuations 1: Right Channels use Left Attenuations

DAC OUTPUT CONTROL

The DAC output control word determines how the left and right inputs to the audio Interface are applied to the left and right DACs:

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION		
0000010 DAC Control	8:5	PL[3:0]	1001	PL[3:0]	Left Output	Right Output
				0000	Mute	Mute
				0001	Left	Mute
				0010	Right	Mute
				0011	(L+R)/2	Mute
				0100	Mute	Left
				0101	Left	Left
				0110	Right	Left
				0111	(L+R)/2	Left
				1000	Mute	Right
				1001	Left	Right
				1010	Right	Right
				1011	(L+R)/2	Right
				1100	Mute	(L+R)/2
				1101	Left	(L+R)/2
				1110	Right	(L+R)/2
				1111	(L+R)/2	(L+R)/2

Table 6 Input to Output Control

ATTENUATION CONTROL

Each DAC channel can be attenuated digitally before being applied to the digital filter. Attenuation is 0dB by default but can be set between 0 and 127.5dB in 0.5dB steps using the 7 Attenuation control bits. All attenuation registers are double latched allowing new values to be pre-latched to several channels before being updated synchronously. Setting the UPDATE bit on any attenuation write will cause all pre-latched values to be immediately applied to the DAC channels. A master attenuation register is also included, allowing all attenuations to be set to the same value in a single write.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
0000000 Attenuation DACL0	7:0	L0A[7:0]	11111111 (0dB)	Attenuation data for DACL0 in 0.5dB steps, see Table 8.
	8	UPDATE	Not latched	Controls simultaneous update of all Attenuation Latches 0: Store DACL0 in intermediate latch (no change to output) 1: Store DACL0 and update attenuation on all channels.
0000001 Attenuation DACR0	7:0	R0A[7:0]	11111111 (0dB)	Attenuation data for DACR0 in 0.5dB steps, see Table 8.
	8	UPDATE	Not latched	Controls simultaneous update of all Attenuation Latches 0: Store DACR0 in intermediate latch (no change to output) 1: Store DACR0 and update attenuation on all channels.
0000100 Attenuation DACL1	7:0	L1A[7:0]	11111111 (0dB)	Attenuation data for DACL1 in 0.5dB steps, see Table 8.
	8	UPDATE	Not latched	Controls simultaneous update of all Attenuation Latches 0: Store DACL1 in intermediate latch (no change to output) 1: Store DACL1 and update attenuation on all channels.
0000101 Attenuation DACR1	7:0	R1A[7:0]	11111111 (0dB)	Attenuation data for DACR1 in 0.5dB steps, see Table 8.
	8	UPDATE	Not latched	Controls simultaneous update of all Attenuation Latches 0: Store DACR1 in intermediate latch (no change to output) 1: Store DACR1 and update attenuation on all channels.
0000110 Attenuation DACL2	7:0	L2A[7:0]	11111111 (0dB)	Attenuation data for DACL2 in 0.5dB steps, see Table 8.
	8	UPDATE	Not latched	Controls simultaneous update of all Attenuation Latches 0: Store DACL2 in intermediate latch (no change to output) 1: Store DACL2 and update attenuation on all channels.
0000111 Attenuation DACR2	7:0	R2A[7:0]	11111111 (0dB)	Attenuation data for DACR2 in 0.5dB steps, see Table 8.
	8	UPDATE	Not latched	Controls simultaneous update of all Attenuation Latches 0: Store DACR2 in intermediate latch (no change to output) 1: Store DACR2 and update attenuation on all channels.
0001000 Master Attenuation (all channels)	7:0	MASTA[7:0]	11111111 (0dB)	Attenuation data for all channels in 0.5dB steps, see Table 8.
	8	UPDATE	Not latched	Controls simultaneous update of all Attenuation Latches 0: Store MASTA[7:0] in all intermediate latches (no change to output) 1: Store MASTA[7:0] and update attenuation on all channels.

Table 7 Attenuation Register Map

Note:

The UPDATE bit is not latched. If UPDATE=0, the Attenuation value will be written to the pre-latch but not applied to the relevant DAC. If UPDATE=1, all pre-latched values will be applied from the next input sample. Writing to MASTA[7:0] overwrites any values previously sent to L0A[7:0], L1A[7:0], L2A[7:0], R0A[7:0], R1A[7:0], R2A[7:0].

DAC OUTPUT ATTENUATION

Register bits [7:0] of L0A and R0A control the left and right channel attenuation of DAC 0. Register bits [7:0] of L1A and R1A control the left and right channel attenuation of DAC 1. Register bits [7:0] of L2A and R2B control the left and right channel attenuation of DAC 2. Register bits [7:0] of MASTA are a register that can be used to control attenuation of all channels.

Table 8 shows how the attenuation levels are selected from the 8-bit words.

XA[7:0]	ATTENUATION LEVEL
00(hex)	-∞dB (mute)
01(hex)	-127.5dB
:	:
:	:
:	:
FE(hex)	-0.5dB
FF(hex)	0dB

Table 8 Attenuation Control Levels

EXTENDED INTERFACE CONTROL

It is possible to run the WM8746 channels at different rates with the front two channels running at twice the rate of the rear four channels. In this mode which is enabled by bit 0 of register 9, the interface runs at the faster data rate but pin 10 (LRCIN2) acts as the framing LRCIN for the rear channels see Figure 9.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
0001001 Split rate mode	0	2SPD	0	Activates the split rate mode 0: Normal operation 1: Split rate operation

When the WM8746 receives updates to the volume levels it will, by default, wait for the signal to pass through V_{CAP} before applying the change to the output. This ensures that minimal distortion is seen on the output when the volume is changed. This function applies individually to each channel.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
0001001 Zero crossing detect	1	ZCD	0	Controls the ZCD 0: Enabled 1: Disabled

HARDWARE CONTROL MODES

When the MODE pin is held high the following hardware modes of operation are available.

MUTE AND AUTOMUTE OPERATION

Pin 9 (MUTE) controls selection of MUTE directly, and can be used to enable and disable the automute function, or as an output of the automuted signal.

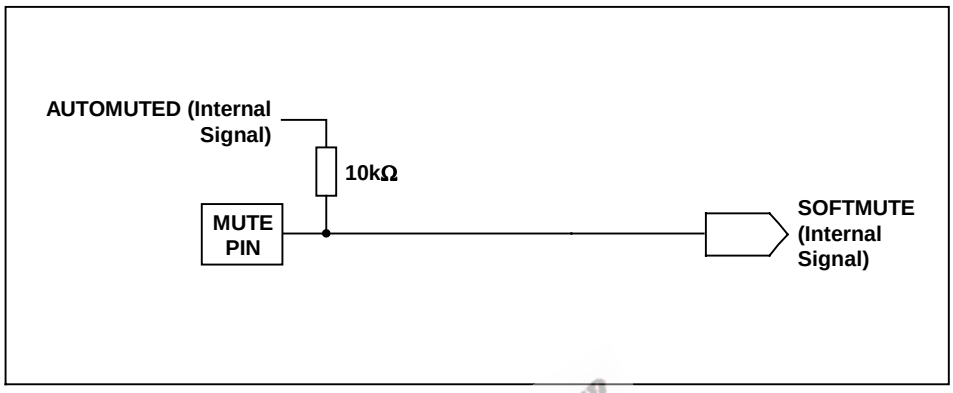


Figure 12 Mute Circuit Operation

The MUTE pin behaves as a bi-directional function, that is, as an input to select MUTE or NOT-MUTE, or as an output indication of automute operation. MUTE is active high; taking the pin high causes the filters to soft mute, ramping down the audio signal over a few milliseconds. Taking MUTE low again allows data into the filter.

The automute function detects a series of zero value audio samples of 1024 samples long being applied to all 6 channels. After such an event, a latch is set whose output (AUTOMUTED) is wire OR'ed through a 10kohm resistor to the MUTE pin. Thus if the MUTE pin is not being driven, the automute function will assert MUTE.

If MUTE is tied low, AUTOMUTED is overridden and will not mute. If MUTE is driven from a source follower, or diode, then both MUTE and automute functions are available. If MUTE is not driven, AUTOMUTED appears as a weak output (10k source impedance) so can be used to drive external mute circuits.

ML/I2S AND MC/IWL INPUT FORMAT SELECTION

In hardware mode, pins 12 and 13 become input controls for selection of input data format type and input data word length, see Table 5. I^2S mode is designed to support any word length provided enough bit clocks are sent.

ML/I2S	MC/IWL	INPUT DATA MODE
0	0	16-bit right justified
0	1	20-bit right justified
1	0	24-bit right justified
1	1	I^2S mode

Table 9 Control of Input Data Format Type and Input Data Word Length

MD/DM DE-EMPHASIS

In hardware mode, pin 14 becomes an input control for selection of de-emphasis filtering to be applied. See Table 5.

MD/DM	DE-EMPHASIS MODE
0	De-emphasis off
1	De-emphasis on

Table 10 De-emphasis Control

SOFTWARE CONTROL INTERFACE

The software control interface uses a 3-wire serial control interface. Selection of interface format is achieved by setting the state of the MODE pin.

MODE	INTERFACE FORMAT
0	Software Control Mode
1	Hardware Control Mode

Table 11 Control Interface Mode Selection

3-WIRE (SPI COMPATIBLE) SERIAL CONTROL MODE

The WM8746 can be controlled using a 3-wire serial interface. MD/DM is used for the program data, MC/IWL is used to clock in the program data and ML/I2S is use to latch in the program data. The 3-wire interface protocol is shown in Figure 13.

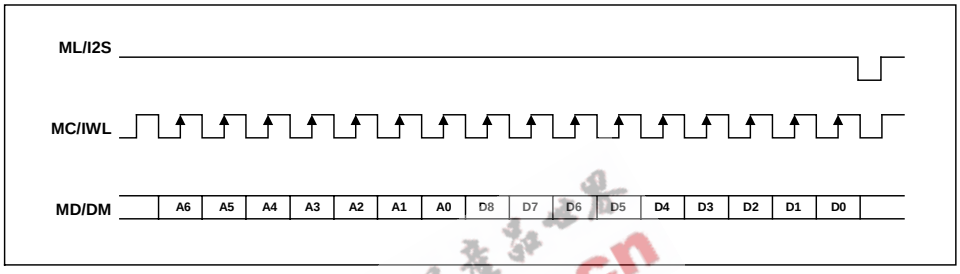


Figure 13 3-wire Serial Interface

Notes:

1. A[6:0] are Control Address Bits
2. D[8:0] are Control Data Bits

REGISTER MAP

The complete register map is shown below. The detailed description can be found in the relevant text of the device description. There are 9 registers with 9 bits per register. These can be controlled using the Control Interface.

	A6	A5	A4	A3	A2	A1	A0	D8	D7	D6	D5	D4	D3	D2	D1	D0
M0	0	0	0	0	0	0	0	UPDATE	L0A7	L0A 6	L0A 5	L0A 4	L0A 3	L0A 2	L0A 1	L0A 0
M1	0	0	0	0	0	0	1	UPDATE	R0A7	R0A 6	R0A 5	R0A 4	R0A 3	R0A 2	R0A 1	R0A 0
M2	0	0	0	0	0	1	0	PL3	PL2	PL1	PL0	IZD	ATC	PDWN	DEEMPH	MUTE
M3	0	0	0	0	0	1	1	REV2	REV1	REV0	IWL1	IWL0	BCP	LRP	FMT1	FMT0
M4	0	0	0	0	1	0	0	UPDATE	L1A7	L1A 6	L1A 5	L1A 4	L1A 3	L1A 2	L1A 1	L1A 0
M5	0	0	0	0	1	0	1	UPDATE	R1A7	R1A 6	R1A 5	R1A 4	R1A 3	R1A 2	R1A 1	R1A 0
M6	0	0	0	0	1	1	0	UPDATE	L2A7	L2A 6	L2A 5	L2A 4	L2A 3	L2A 2	L2A 1	L2A 0
M7	0	0	0	0	1	1	1	UPDATE	R2A7	R2A 6	R2A 5	R2A 4	R2A 3	R2A 2	R2A 1	R2A 0
M8	0	0	0	1	0	0	0	UPDATE	MASTA7	MASTA 6	MASTA 5	MASTA 4	MASTA 3	MASTA 2	MASTA 1	MASTA 0
M9	0	0	0	1	0	0	1	0	0	0	0	0	0	0	ZCD	2SPD

Table 12 Register Map

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
0000000 Attenuation DACL0	7:0	L0A[7:0]	11111111 (0dB)	Attenuation level of left channel DACL0 in 0.5dB steps, see Table 8.
	8	UPDATE	Not latched	Controls simultaneous update of all Attenuation Latches 0: Store DACL0 in intermediate latch (no change to output) 1: Store DACL0 and update attenuation on all channels.
0000001 Attenuation DACR0	7:0	R0A[7:0]	11111111 (0dB)	Attenuation level of left channel DACR0 in 0.5dB steps, see Table 8.
	8	UPDATE	Not latched	Controls simultaneous update of all Attenuation Latches 0: Store DACR0 in intermediate latch (no change to output) 1: Store DACR0 and update attenuation on all channels.

<table>
<tr><th>REGISTER ADDRESS</th><th>BIT</th><th>LABEL</th><th>DEFAULT</th><th>DESCRIPTION</th></tr>
<tr><td rowspan="9">0000010
DAC Control</td><td>0</td><td>MUTE</td><td>0</td><td>Left and Right DACs soft mute control
0: No Mute
1: Mute</td></tr>
<tr><td>1</td><td>DEEMPH</td><td>0</td><td>De-emphasis Control
0: Normal Response (see Figure 14 - Figure 17)
1: De-emphasis Response (see Figure 18 - Figure 23)</td></tr>
<tr><td>2</td><td>PWDN</td><td>0</td><td>Left and Right DACs Power-down Control
0: All DACs running, output is active
1: All DACs in power saving mode, output muted</td></tr>
<tr><td>3</td><td>ATC</td><td>0</td><td>Attenuator Control
0: All DACs use attenuations as programmed.
1: Right chan. DACs use corresponding left DAC attenuations</td></tr>
<tr><td>4</td><td>IZD</td><td>0</td><td>Infinite zero detection circuit control and automute control
0: Infinite zero detect disabled
1: Infinite zero detect enabled</td></tr>
<tr><td>8:5</td><td>PL[3:0]</td><td>1001</td><td>DAC Output Control
<table>
<tr><th>PL[3:0]</th><th>Left Output</th><th>Right Output</th><th>PL[3:0]</th><th>Left Output</th><th>Right Output</th></tr>
<tr><td>0000</td><td>Mute</td><td>Mute</td><td>1000</td><td>Mute</td><td>Right</td></tr>
<tr><td>0001</td><td>Left</td><td>Mute</td><td>1001</td><td>Left</td><td>Right</td></tr>
<tr><td>0010</td><td>Right</td><td>Mute</td><td>1010</td><td>Right</td><td>Right</td></tr>
<tr><td>0011</td><td>(L+R)/2</td><td>Mute</td><td>1011</td><td>(L+R)/2</td><td>Right</td></tr>
<tr><td>0100</td><td>Mute</td><td>Left</td><td>1100</td><td>Mute</td><td>(L+R)/2</td></tr>
<tr><td>0101</td><td>Left</td><td>Left</td><td>1101</td><td>Left</td><td>(L+R)/2</td></tr>
<tr><td>0110</td><td>Right</td><td>Left</td><td>1110</td><td>Right</td><td>(L+R)/2</td></tr>
<tr><td>0111</td><td>(L+R)/2</td><td>Left</td><td>1111</td><td>(L+R)/2</td><td>(L+R)/2</td></tr>
</table></td></tr>
<tr><td rowspan="5">0000011
Interface Control</td><td>1:0</td><td>FMT[1:0]</td><td>00</td><td>Interface format select
00: right justified mode
01: left justified mode
10: I^{2}S mode
11: DSP mode</td></tr>
<tr><td>2</td><td>LRP</td><td>0</td><td>LRCIN Polarity or LRCIN Phase
<table>
<tr><th>Left Justified / Right Justified / I^{2}S</th><th>DSP Mode</th></tr>
<tr><td>0: Standard LRCIN Polarity
1: Inverted LRCIN Polarity</td><td>0: DSP early mode
1: DSP late mode</td></tr>
</table></td></tr>
<tr><td>3</td><td>BCP</td><td>0</td><td>BCKIN Polarity
0: Normal (DIN[2:0] and LRCIN sampled on rising edge)
1: Inverted (DIN[2:0] and LRCIN sampled on falling edge)</td></tr>
<tr><td>5:4</td><td>WL[1:0]</td><td>0</td><td>Input Word Length
00: 16-bit Mode
01: 20-bit Mode
10: 24-bit Mode
11: 32-bit Mode (not supported in right justified mode)</td></tr>
<tr><td>8:6</td><td>PHASE</td><td>000</td><td>Controls the output phase of the three stereo channels
Bit 6 reverses the phase of data output on OUT0L/R.
Bit 7 reverses the phase of data output on OUT1L/R.
Bit 8 reverses the phase of data output on OUT2L/R.</td></tr>
</table>

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
0000100 Attenuation DACL1	7:0	L1A[7:0]	11111111 (0dB)	Attenuation level of left channel DACL1 in 0.5dB steps. See Table 8
	8	UPDATE	Not latched	Controls simultaneous update of all Attenuation Latches 0: Store DACL1 in intermediate latch (no change to output) 1: Store DACL1 and update attenuation on all channels.
0000101 Attenuation DACR1	7:0	R1A[7:0]	11111111 (0dB)	Attenuation level of right channel DACR1 in 0.5dB steps, see Table 8.
	8	UPDATE	Not latched	Controls simultaneous update of all Attenuation Latches 0: Store DACR1 in intermediate latch (no change to output) 1: Store DACR1 and update attenuation on all channels.
0000110 Attenuation DACL2	7:0	L2A[7:0]	11111111 (0dB)	Attenuation level of left channel DACL2 in 0.5dB steps, see Table 8.
	8	UPDATE	Not latched	Controls simultaneous update of all Attenuation Latches 0: Store DACL2 in intermediate latch (no change to output) 1: Store DACL2 and update attenuation on all channels.
0000111 Attenuation DACR2	7:0	R2A[7:0]	11111111 (0dB)	Attenuation level of right channel DACR2 in 0.5dB steps, see Table 8.
	8	UPDATE	Not latched	Controls simultaneous update of all Attenuation Latches 0: Store DACR2 in intermediate latch (no change to output) 1: Store DACR2 and update attenuation on all channels.
0001000 Master Attenuation (all channels)	7:0	MASTA[7:0]	11111111 (0dB)	Attenuation data for all channels in 0.5dB steps, see Table 8.
	8	UPDATE	Not latched	Controls simultaneous update of all Attenuation Latches 0: Store MASTA[7:0] in all intermediate latches (no change to output) 1: Store DACR0 and update attenuation on all channels
0001001 Extended interface control	0	2SPD	0	Activates the split rate mode where the front channels run at 192kHz and the rear four channels run at 96kHz. 0: Normal operation. 1: Split rate operation.
	1	ZCD	0	Controls the operation of the zero crossing detect mechanism which ensures that the volume is only updated on each channel when the signal passes through midrail. 0: Enable zero detect. 1: Disable zero detect.

Table 13 Register Map Description

DIGITAL FILTER CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Passband		±0.05 dB	0.444fs			dB
Stopband		-3dB		0.487fs		
Passband Ripple					±0.05	dB
Stopband Attenuation		f > 0.555fs			-60	dB

Table 14 Digital Filter Characteristics

DAC FILTER RESPONSES

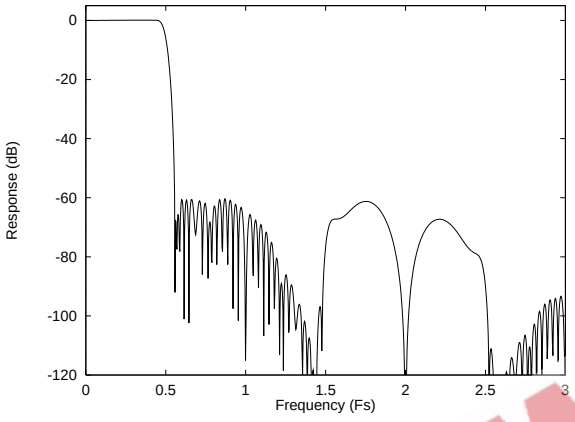


Figure 14 DAC Digital Filter Frequency Response – 44.1, 48 and 96kHz

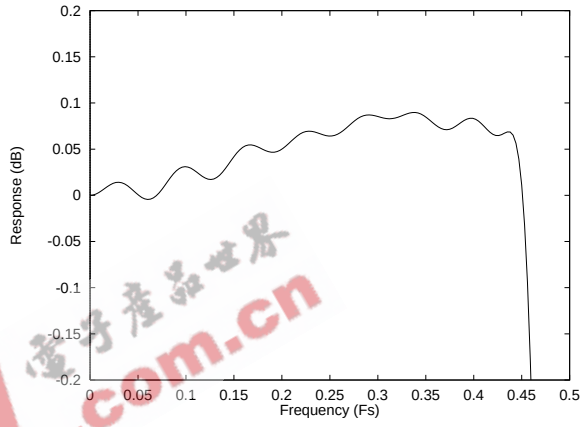


Figure 15 DAC Digital Filter Ripple –44.1, 48 and 96kHz

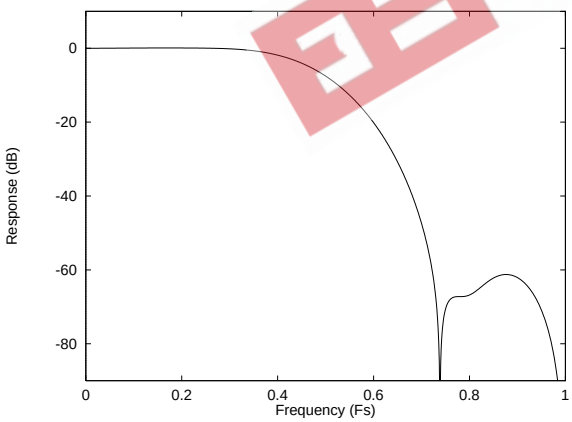


Figure 16 DAC Digital Filter Frequency Response – 192kHz

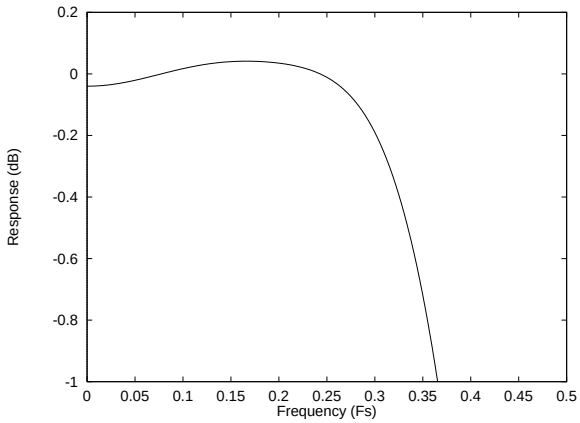


Figure 17 DAC Digital Filter Ripple – 192 kHz

DIGITAL DE-EMPHASIS CHARACTERISTICS

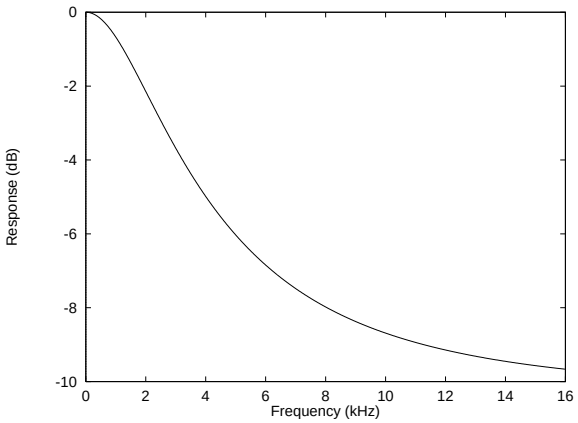


Figure 18 De-Emphasis Frequency Response (32kHz)

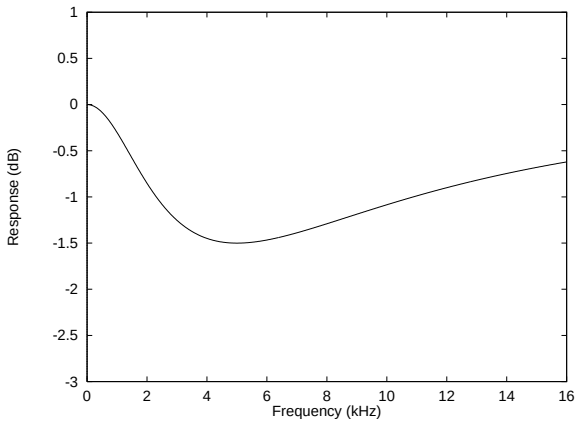


Figure 19 De-Emphasis Error (32kHz)

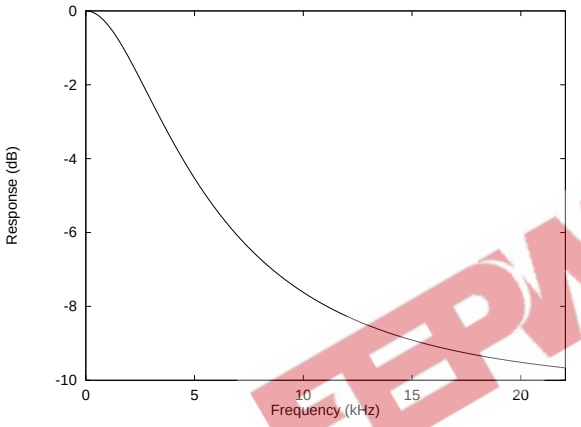


Figure 20 De-Emphasis Frequency Response (44.1kHz)

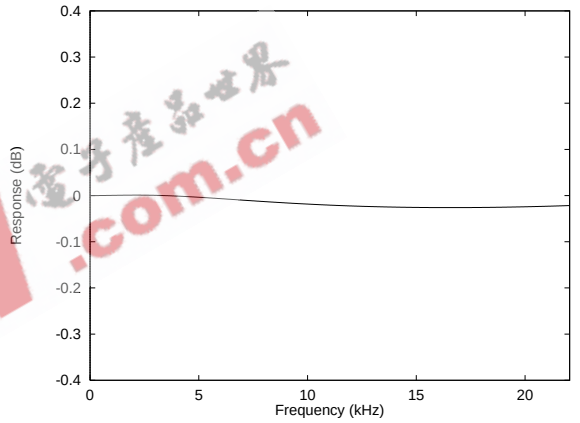


Figure 21 De-Emphasis Error (44.1kHz)

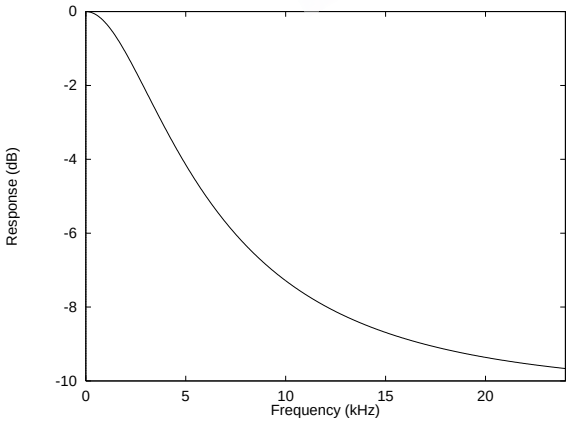


Figure 22 De-Emphasis Frequency Response (48kHz)

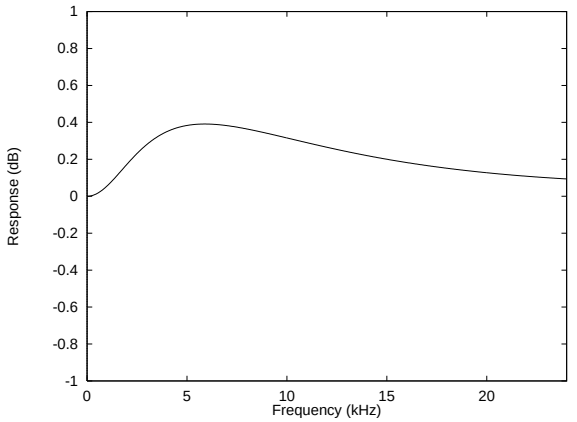
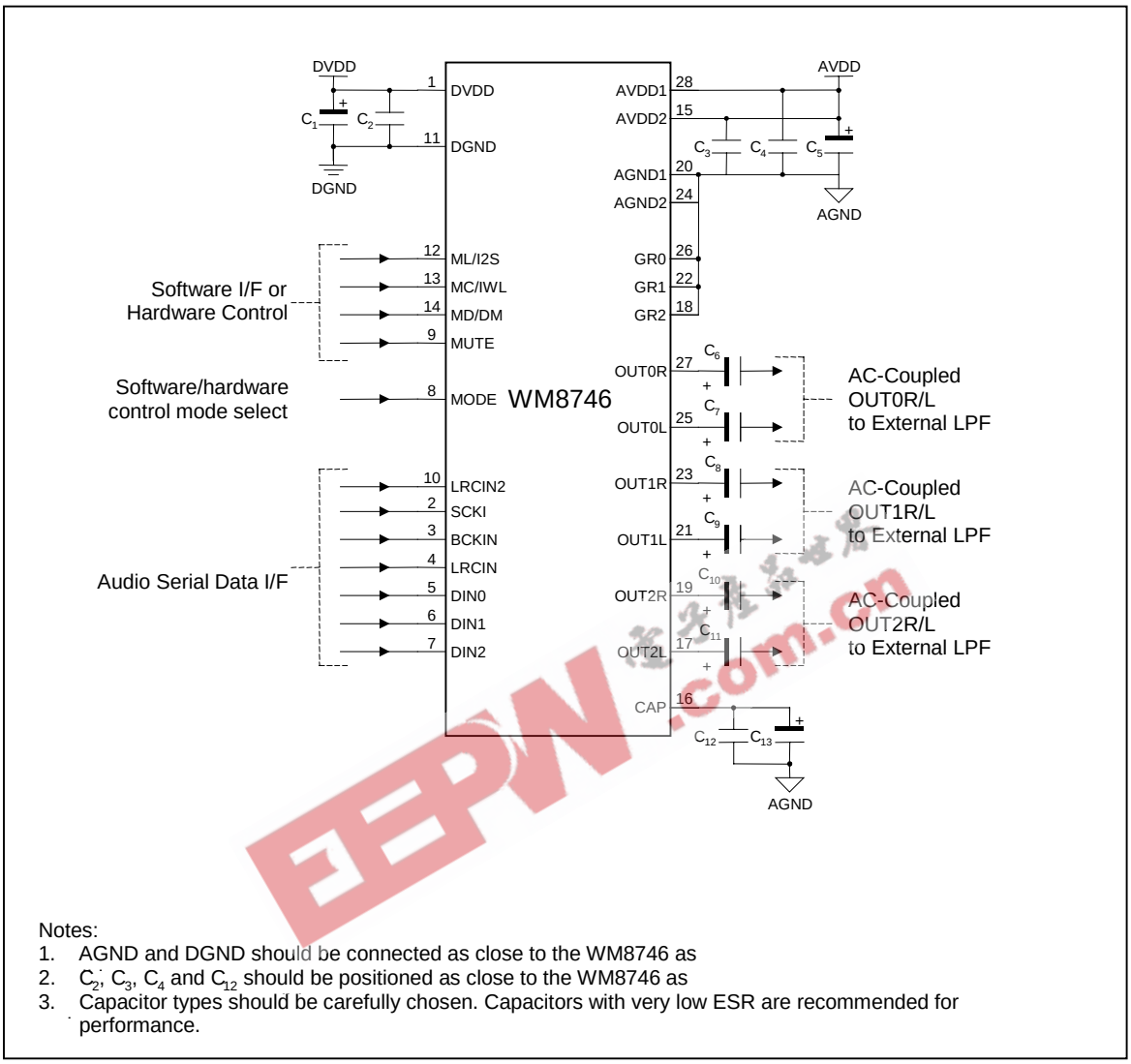


Figure 23 De-Emphasis Error (48kHz)

RECOMMENDED EXTERNAL COMPONENTS



Notes:
1. AGND and DGND should be connected as close to the WM8746 as
2. C_2, C_3, C_4 and C_{12} should be positioned as close to the WM8746 as
3. Capacitor types should be carefully chosen. Capacitors with very low ESR are recommended for performance.

Figure 24 External Components Diagram

RECOMMENDED EXTERNAL COMPONENTS VALUES

COMPONENT REFERENCE	SUGGESTED VALUE	DESCRIPTION
C1 and C5	10µF	De-coupling for DVDD and AVDD.
C2 to C4	0.1µF	De-coupling for DVDD and AVDD.
C6 to C11	10µF	Output AC coupling caps to remove midrail DC level from outputs.
C12	0.1µF	Reference de-coupling capacitors for CAP pin.
C13	10µF	

Table 15 External Components Description

RECOMMENDED ANALOGUE LOW PASS FILTER (OPTIONAL)

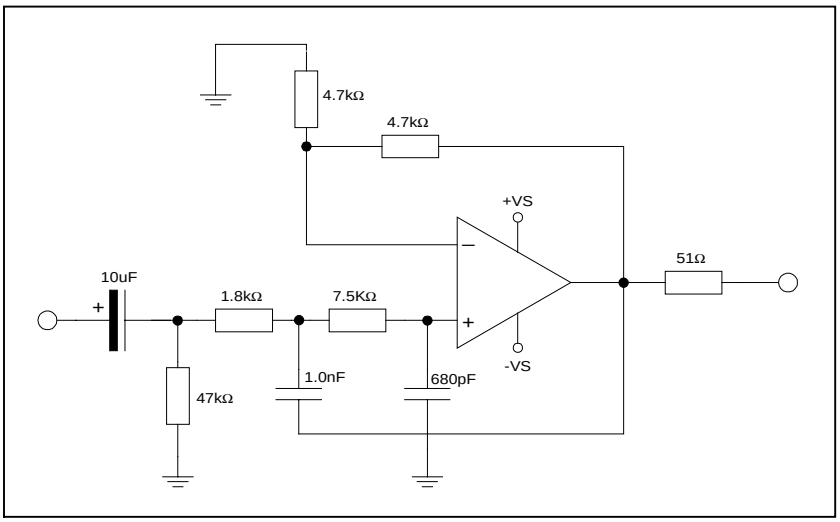
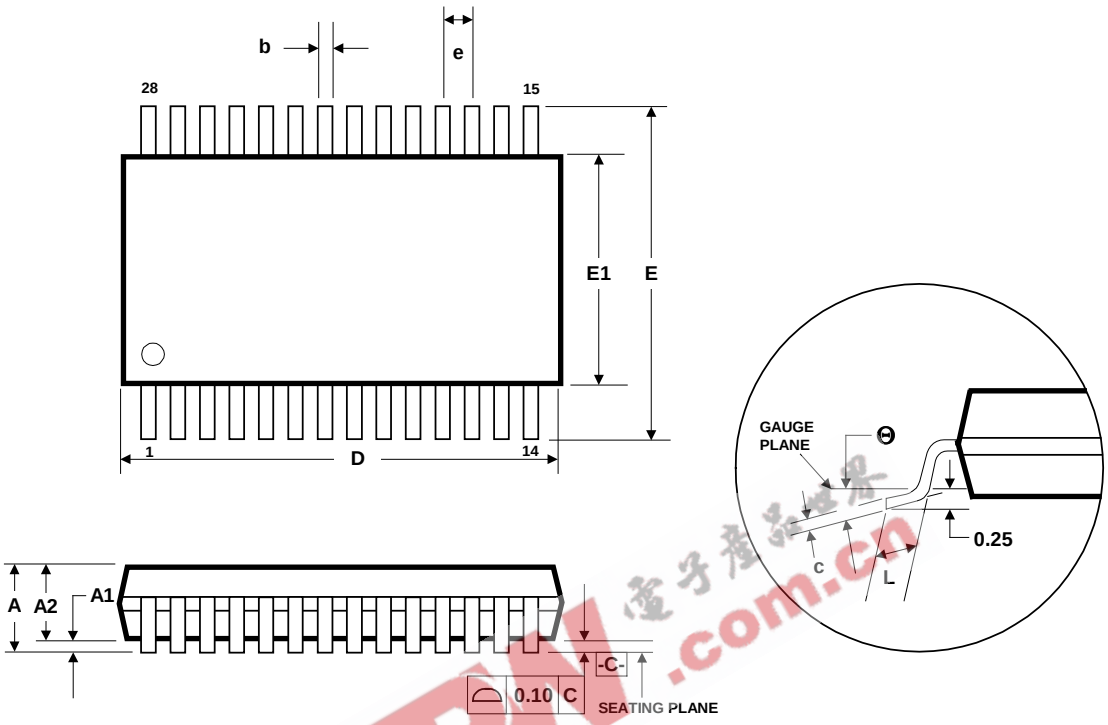


Figure 25 Recommended Low Pass Filter (Optional)

PACKAGE DIMENSIONS

DS: 28 PIN SSOP (10.2 x 5.3 x 1.75 mm) **DM007.C**



Symbols	Dimensions (mm)		
	MIN	NOM	MAX
A	-----	-----	2.0
A_1	0.05	-----	-----
A_2	1.62	1.75	1.85
b	0.22	-----	0.38
c	0.09	-----	0.25
D	9.90	10.20	10.50
e		0.65 BSC	
E	7.40	7.80	8.20
E_1	5.00	5.30	5.60
L	0.55	0.75	0.95
θ	0^o	4^o	8^o
REF:	JEDEC.95, MO-150		

NOTES:
A. ALL LINEAR DIMENSIONS ARE IN MILLIMETERS.
B. THIS DRAWING IS SUBJECT TO CHANGE WITHOUT NOTICE.
C. BODY DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSION, NOT TO EXCEED 0.20MM.
D. MEETS JEDEC.95 MO-150, VARIATION = AH. REFER TO THIS SPECIFICATION FOR FURTHER DETAILS.

REVISION HISTORY

Revision	Originator	Change Date	History
1.4	SP	13/11/2001	AVDD pin assignments were incorrect. AVDD1 is pin 28 and AVDD2 is pin 15

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