TRANSWITCH

MRT Devi
6-, 8-, 34- Mbit/s Line Interfa
TXC-0205

DATA SHE

FEATURES

- 6312/8448/34368 kbit/s line interface
- AGC and equalizer
- Line quality monitor (10^{-6} error rate threshold)
- Receive loss of signal and transmit loss of clock alarms
- Selectable HDB3 encoder/decoder
- Two loopbacks:
  - Receive to transmit
  - Transmit to receive
- Receive and Transmit AIS generators
- Rail or NRZ terminal side I/O
- Coding violation monitor
- Meets ITU-T Rec. G.703 pulse masks
- Meets ITU-T Rec. G.823 and JT-670,3 jitter requirements
- 44-pin plastic leaded chip carrier

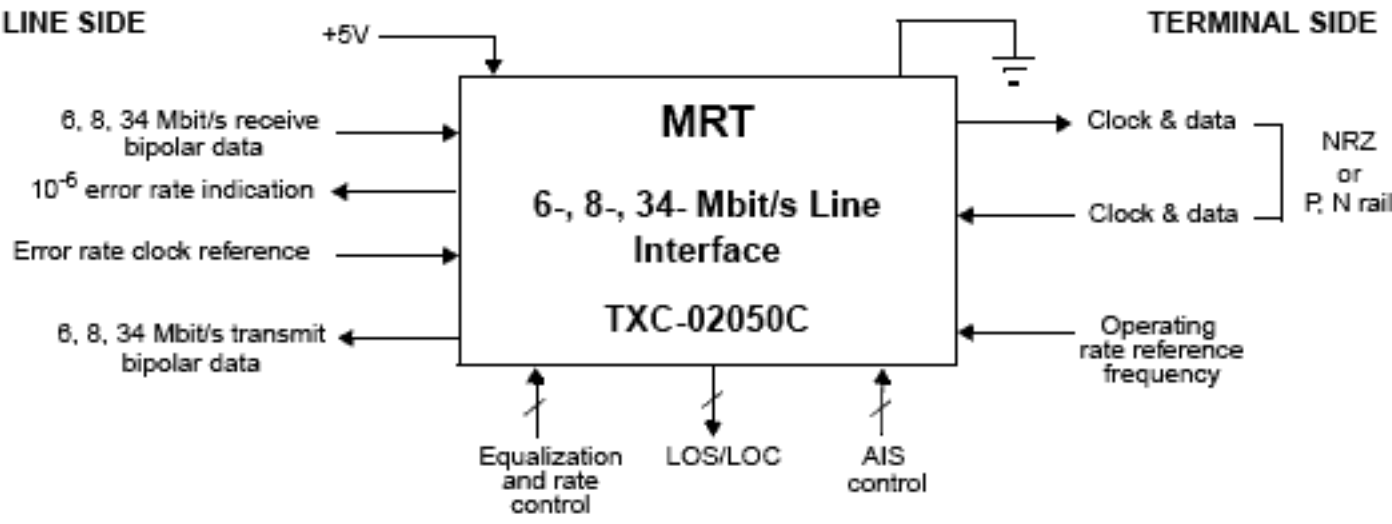
DESCRIPTION

The TranSwitch Multi-rate Receive/Transmit (MRT) L
Interface is a CMOS VLSI device that provides
functions needed for terminating two ITU-T line rat
8448 and 34368 kbit/s, or a 6312 kbit/s rate which
specified in the Japanese NTT Technical Reference
High Speed Digital Leased Circuits. For 8448 and 343
kbit/s operation, the MRT provides a selectable HD
codec.

The MRT is equipped with a receive equalizer circuit a
AGC. The MRT also provides a rail or NRZ interfa
HDB3 error rate monitor, alarm detection, and A
generators. Testing capability is provided by trans
and receive loopbacks.

APPLICATIONS

- Digital cross-connect equipment
- Remote terminals
- Terminal interface for multiplexers/demultiplexers
- Switching systems
- CSU/DSU



Document Numb
TXC-02050C-
Ed. 1, May 20

TranSwitch Corporation • 3 Enterprise Drive • Shelton, Connecticut 06484 • USA
Tel: 203-929-8810 • Fax: 203-926-9453 • www.transwitch.com

TABLE OF CONTENTS

* Please note that TranSwitch provides documentation for all of its products. Current editions of many documents are available from the Products page of the TranSwitch Web site at www.transwitch.com. Customers who are using a TranSwitch Product, or planning to do so, should register with the TranSwitch Marketing Department to receive relevant updated and supplemental documentation as it is issued. They should also contact the Applications Engineering Department to ensure that they are provided with the latest available information about the product, especially before undertaking development of new designs incorporating the product.

LIST OF FIGURES

BLOCK DIAGRAM

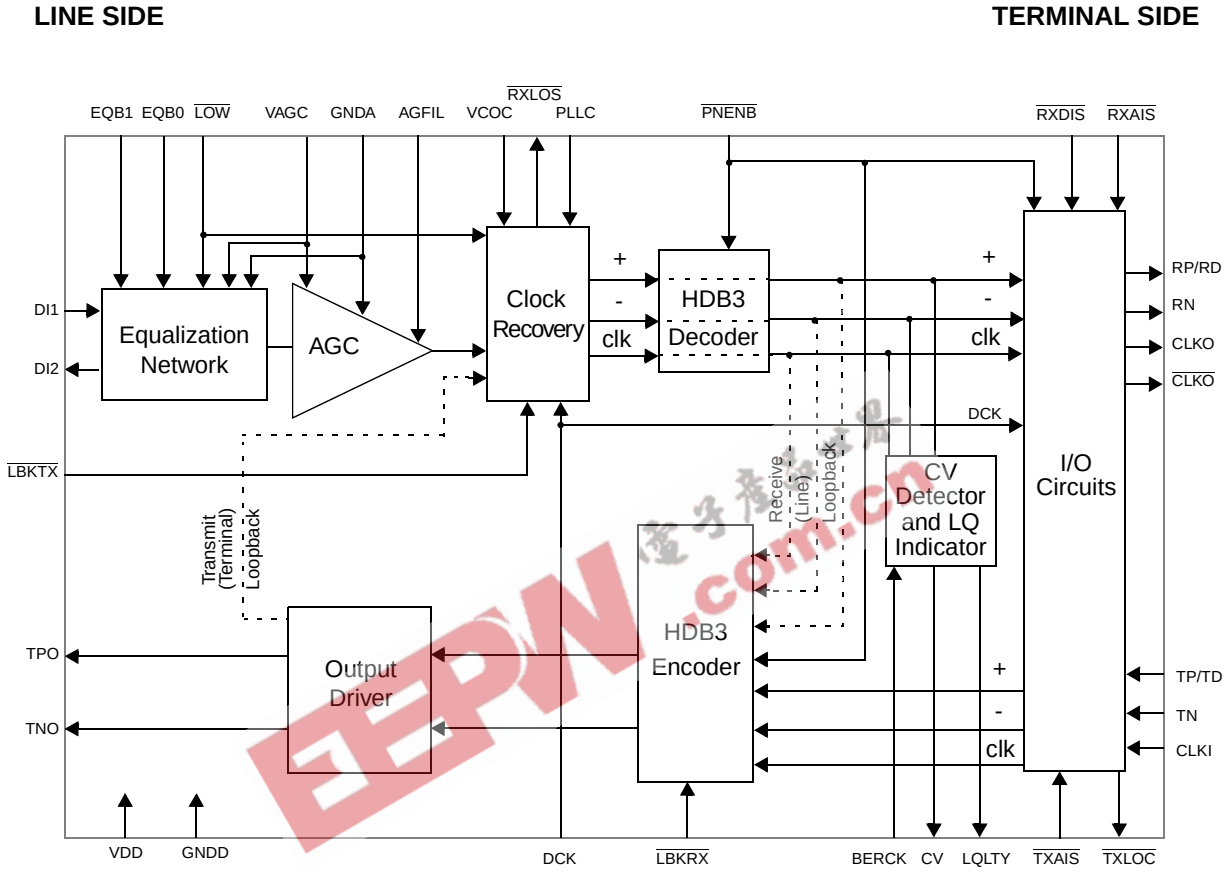


Figure 1. MRT TXC-02050C Block Diagram

BLOCK DIAGRAM DESCRIPTION

On the Line Side, a symmetrical bipolar signal is applied to the input signal pin (DI1), which requires an external 75Ω termination. DI2 is a DC reference voltage output which serves as an AC ground.

Equalization for various lengths of cable having a $\sqrt{f}$ attenuation characteristic is compensated by setting the states of the EQB0 and EQB1 signal leads. The Equalization Network Block is connected to an AGC Block which has approximately a 20 dB dynamic range. The AGC has separate voltage and ground leads for noise immunity, and uses an external capacitor as part of an AGC filter. The AGC output is connected to the Clock Recovery Block.

The Clock Recovery Block contains a phase-locked loop and supporting logic to generate a clock signal from the line signal. The signal lead $\overline{\text{LOW}}$ selects the appropriate circuit in the Clock Recovery Block for the operating frequency and provides input attenuation for the receive line signal. The line input is monitored for loss of signal, with an alarm indication provided on the $\overline{\text{RXLOS}}$ signal lead. The Clock Recovery Block requires an external reference clock at the operating frequency (DCK). The reference clock is also used for generating and sending a receive Alarm Indication Signal (AIS). The generation and sending of AIS for recovered data is controlled by the $\overline{\text{RXAIS}}$ signal lead.

The output of the Clock Recovery Block is connected to the HDB3 Decoder Block, when enabled, or directly to the I/O Circuits Block. When the decoder is enabled, indications of coding violation errors, other than the normal HDB3 zero substitution codes, are provided as pulses on the signal lead labeled CV by the CV Detector and LQ Indicator Block. Examples of HDB3 coding and violations are shown in Figure 19. An external clock (BERCK) is used to generate a 10-second sampling window for detecting a 10^{-6} or greater error rate. The resulting line quality indication is provided on the output signal lead LQLTY.

Two Terminal Side interfaces are provided, a positive and negative rail (RP and RN) or NRZ (RD) interface. The selection is determined by the state placed on the input signal lead $\overline{\text{PNENB}}$. When a low is applied to this signal lead, the HDB3 Decoder and HDB3 Encoder Blocks are bypassed, and the terminal side I/O is a positive and negative rail interface. When a high is applied to the signal lead, an NRZ interface is provided. Data is clocked out of the MRT on negative edges of the clock output signal (CLKO). Receive data and the clock signals are disabled, and forced to a high impedance state, by placing a low on the receive disable input lead ($\overline{\text{RXDIS}}$). For a receive positive and negative rail interface, an inverted clock output signal ($\overline{\text{CLKO}}$) is also provided.

The terminal side interface for the transmitter can either be positive and negative rail (TP and TN) or NRZ (TD) data depending on the state of the common control input lead $\overline{\text{PNENB}}$ (see Figure 20 for examples). Data is clocked into the MRT on positive transitions of the clock signal (CLKI). The input clock is monitored for the loss of clock. When the input clock remains high or low, $\overline{\text{TXLOC}}$ will be set low. The MRT also provides the capability to generate and insert AIS (all ones signal), independent of the transmit data. A low placed on the $\overline{\text{TXAIS}}$ input lead enables the transmit AIS generator.

Two loopbacks are provided, transmit loopback and receive loopback. Transmit loopback connects the data path from the transmitter Output Driver Block to the Clock Recovery Block, and disables the external receiver input. Transmit loopback is activated by placing a low on the $\overline{\text{LBKTX}}$ input signal lead. Receive loopback connects the receive data path to the transmit output circuits and disables the transmit input. Receive loopback is activated by placing a low on the $\overline{\text{LBKRX}}$ input signal lead.

For 6 Mbit/s operation, the MRT should be operated in the P and N rail mode, bypassing the HDB3 Decoder/Encoder. When the MRT is used with the TranSwitch JT2F device at this bit rate, the JT2F can provide either B6ZS or B8ZS encoding and decoding.

PIN DIAGRAM

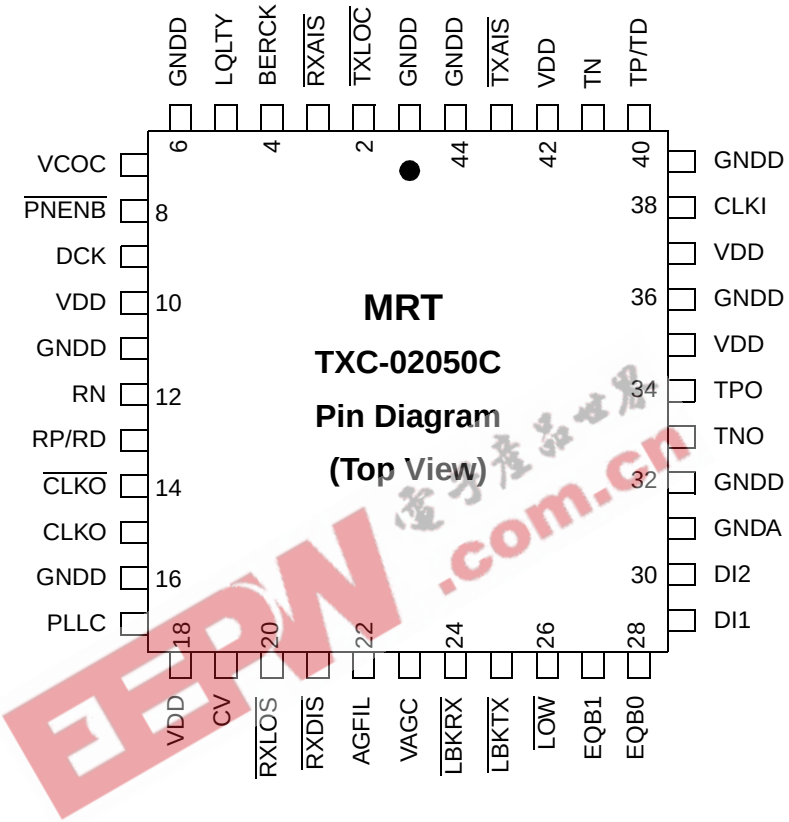


Figure 2. MRT TXC-02050C Pin Diagram

PIN DESCRIPTIONS

Power Supply and Ground

Symbol	Pin No.	I/O/P*	Type	Name/Function
VDD	10,18,35, 37,42	P		**VDD:** V_{DD}, +5 volt supply, ±5%.
GNDD	1,6,11,16,32, 36,39,44	P		**Digital Ground:** 0 volts reference.
VAGC	23	P		**AGC VDD:** +4.3 volt supply, derived from V_{DD} using 1N914 or 1N4148 diode (see Figure 10).
GNDA	31	P		**Analog Ground**: 0 volts reference.

*Note: I = Input; O = Output; P = Power.

Line Side I/O

Symbol	Pin No.	I/O/P	Type *	Name/Function
DI1	29	I	Analog	**Data In 1:** HDB3 or B8ZS encoded bipolar receive data input.
DI2	30	O	Analog	**Data In 2:** DC Voltage Reference for Data Input DI1. The MRT uses an internally generated voltage reference as an AC ground for the received data input. An external 0.1 µF capacitor, in parallel with a 10 µF/6.3 V tantalum capacitor, is connected between this pin and ground. No other connection should be made to this pin.
TNO	33	O	TTL24mA	**Transmit Negative Out:** Line transmit negative; output is active high.
TPO	34	O	TTL24mA	**Transmit Positive Out:** Line transmit positive; output is active high.

* See Input and Output Parameters section for digital Type definitions.

Terminal Side I/O

Symbol	Pin No.	I/O/P	Type	Name/Function
RN	12	O	TTL4mA (Tristate)	**Receive Negative:** When $\overline{\text{PNENB}}$ is low, the HDB3 codec is bypassed and N-rail (RN) data is provided on this pin. When $\overline{\text{PNENB}}$ is high or $\overline{\text{RXDIS}}$ is low, this pin is forced to a high impedance state (disabled).
RP/RD	13	O	TTL4mA (Tristate)	**Receive Positive/Receive Data:** When $\overline{\text{PNENB}}$ is low, the HDB3 codec is bypassed and P-Rail (RP) data is provided on this pin. When $\overline{\text{PNENB}}$ is high, NRZ data (RD) is provided. When $\overline{\text{RXDIS}}$ is low, this pin is forced to a high impedance state (disabled).

Symbol	Pin No.	I/O/P	Type	Name/Function
$\overline{\text{CLKO}}$	14	O	CMOS8mA (Tristate)	**Clock Out Inverted:** Receive inverted clock output. Positive and negative rail receive data is clocked out on the rising edge. When $\overline{\text{PNENB}}$ is high or $\overline{\text{RXDIS}}$ is low, this pin is forced to a high impedance state (disabled).
CLKO	15	O	CMOS8mA (Tristate)	**Clock Out:** Receive clock output. Receive positive and negative rail and NRZ data is clocked out on the falling edge. When $\overline{\text{RXDIS}}$ is low, this pin is forced to a high impedance state (disabled).
CLKI	38	I	TTLr	**Clock In:** Transmit clock input for P and N rail and NRZ data. Transmit data is clocked into the MRT on the rising edge. This clock must have a frequency accuracy of ± 20 ppm for the 34368 kbit/s operation and ± 30 ppm for the 6312/8448 kbit/s operation (ref: ITU-T recommendation G.703). The duty cycle requirement for this clock signal is (50 ± 5) %, measured at the 1.4V TTL threshold level.
TP/TD	40	I	TTL	**Transmit Positive/Transmit Data:** When $\overline{\text{PNENB}}$ is low, the HDB3 codec is bypassed and transmit P-rail (TP) data is applied to this pin. When $\overline{\text{PNENB}}$ is high, NRZ transmit data (TD) is applied.
TN	41	I	TTL	**Transmit Negative:** When $\overline{\text{PNENB}}$ is low, the HDB3 codec is bypassed and transmit N-Rail (TN) is applied to this pin. When $\overline{\text{PNENB}}$ is high, this input is disabled.

Alarm Signal Outputs

Symbol	Pin No.	I/O/P	Type	Name/Function
$\overline{\text{TXLOC}}$	2	O	TTL2mA	**Transmit Loss Of Clock:** Active low output. A transmit loss of clock alarm occurs when the transmit clock input (CLKI) is stuck high or low for about 500 clock cycles. Recovery occurs on the first input clock transition. DCK is required for proper operation.
LQLTY	5	O	TTL2mA	**Line Quality:** This signal represents an estimate of the line quality which is determined by counting coding violations for 34 (8) Mbit/s operation. If the line error rate exceeds a 10^{-6} threshold during a 10 (40) second interval, LQLTY goes active high. LQLTY is active low when coding violations do not exceed the 10^{-6} threshold in a 10 (40) second interval. The output on this pin is only valid when the appropriate clock signal is applied to BERCK. It should be disregarded in the P and N mode of operation or in 6 Mbit/s operation.

Symbol	Pin No.	I/O/P	Type	Name/Function
CV	19	O	TTL2mA	**Coding Violation:** Active high output. A coding violation pulse occurs when an HDB3 coding violation is detected in the received line data input. A coding violation is not part of the HDB3 zero-substitution code. A coding violation occurs because of noise or other impairments affecting the line signal. The output of this pin should be disregarded in the P and N mode.
$\overline{\text{RXLOS}}$	20	O	TTL2mA	**Receive Loss Of Signal:** Active low output. A receive loss of signal occurs when the input data is zero for 40-50 µs. Recovery occurs when the receive signal returns.

MRT Control Leads

Symbol	Pin No.	I/O/P	Type	Name/Function
$\overline{\text{RXAIS}}$	3	I	CMOSr	**Receive Alarm Indication Signal:** When $\overline{\text{RXAIS}}$ is low, the MRT generates AIS (all ones signal) for the terminal side receive output data. The line side receive data path is disabled. The reference clock (DCK) provides the clock source required for generating AIS.
BERCK	4	I	TTLr	**Bit Error Rate Clock:** This clock establishes the time base for estimating the coding violation error rate. For 34 Mbit/s operation the clock frequency must be 6 kHz, and for 8 Mbit/s operation the clock frequency must be 1.5 kHz. This pin should be left open for P and N mode operation.
$\overline{\text{PNENB}}$	8	I	CMOSr	**P And N Enable:** When $\overline{\text{PNENB}}$ is low, the P and N rail interface is enabled, and the HDB3 codec is bypassed. When $\overline{\text{PNENB}}$ is high, the terminal side I/O data is NRZ and the HDB3 codec is enabled. This pin must be held low for 6 Mbit/s operation.
DCK	9	I	TTL	**Reference Clock:** Operating frequency reference clock. For receive signal clock recovery, ± 200 ppm frequency accuracy is adequate. If the transmit and receive AIS features are used, the frequency accuracy must be ± 20 ppm for 34368 kbit/s and ± 30 ppm for 8448 and 6312 kbit/s operation. The duty cycle requirement for this clock signal is (50 ± 5) % as measured at the 1.4V TTL threshold level.
$\overline{\text{RXDIS}}$	21	I	CMOSr	**Receive Disable:** When $\overline{\text{RXDIS}}$ is low, the receive side of the MRT is disabled and the RN, RP/RD, CLKO and $\overline{\text{CLKO}}$ output leads are forced to a high impedance state.

Symbol	Pin No.	I/O/P	Type	Name/Function
$\overline{\text{LBKRX}}$	24	I	CMOSr	**Loopback Receive:** When $\overline{\text{LBKRX}}$ is low, the MRT loops back receive data as transmit data. The receive data is also sent to the terminal side, but the transmit data input on the terminal side is disabled (see Note 1).
$\overline{\text{LBKTX}}$	25	I	CMOSr	**Loopback Transmit:** When $\overline{\text{LBKTX}}$ is low, the MRT loops back transmit data as receive data. The transmit data is sent on the line side, but the receive data input on the line side is disabled (see Note 1).

Note 1: Setting $\overline{\text{LBKTX}}$ and $\overline{\text{LBKRX}}$ low simultaneously will cause invalid outputs at the receive terminal and transmit line ports.

$\overline{\text{LOW}}$	26	I	CMOSr	**Low Frequency:** When $\overline{\text{LOW}}$ is low, the MRT enables equalization and input attenuator settings for 6312 or 8448 kbit/s operation. When $\overline{\text{LOW}}$ is high, the settings for 34368 kbit/s operation are enabled. This lead also controls the clock recovery high/low frequency range circuit.
EQB1 EQB0	27 28	I I	CMOSr	**Equalizer Bit 1:** MSB of equalizer setting. **Equalizer Bit 0:** LSB of equalizer setting. The equalizer setting depends on cable length (attenuation) as shown in the following tables. For 34 Mbit/s operation: EQB1 EQB0 Cable Attenuation @ f * Equivalent ATT 734A Cable 1 1 0dB < cable < 5.7dB 0 - 550 ft. 1 0 4.1dB < cable < 12dB 400 - 1150 ft. 0 0 5.7dB < cable < 14dB 550 - 1350 ft. 0 1 6.8dB < cable <14 dB 650 - 1350 ft. For 8 Mbit/s operation: 1 1 0dB < cable < 3.5dB 0 - 550 ft. 1 0 3.0dB < cable < 6.5dB 500 - 1100 ft. 0 0 3.6dB < cable < 6.8dB 700 - 1350 ft. For 6 Mbit/s operation (see Note 2): Equivalent ATT 734A Cable 1 1 0dB < cable < 2.4dB 0 - 550 ft. 1 0 2.4dB < cable < 5.1dB 500 - 1100 ft. 0 0 3.1dB < cable < 6.0dB 700 - 1350 ft * f = 1/2 the bit rate
$\overline{\text{TXAIS}}$	43	I	CMOSr	**Transmit AIS:** When $\overline{\text{TXAIS}}$ is low, the MRT sends an AIS (all ones signal) for the line side transmit output data. The terminal side transmit data path is disabled. The reference clock (DCK) provides the clock required for generating AIS. equivalent

Note 2: For 6 Mbit/s operation, setting the equalizer for long cable length while having a short cable will cause an error in the recovered clock frequency. The recovered clock frequency will not be 6.312 MHz.

Pins With External Components

Symbol	Pin No.	I/O/P	Type	Name/Function
VCOC	7	I	Analog	**Voltage Controlled Oscillator Capacitor:** For 6, 8, and 34 Mbit/s operation, a 470 ohm ± 5% 1/8 watt resistor is connected in series with a 0.1 µF ± 10% capacitor from this pin to ground. This component is used in the phase-locked loop filter.
PLLC	17	I	Analog	**Phase-Locked Loop Capacitor:** 0.1 µF ± 10% ceramic disk capacitor connected to ground.
AGFIL	22	I	Analog	**Automatic Gain Filter:** For 6 , 8, and 34 Mbit/s operation, a 0.1 µF ± 10% ceramic disk capacitor is connected from this pin to ground.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min *	Max *	Unit
Supply voltage	V_{DD}	-0.3	+7.0	V
AGC Supply Voltage	V_{AGC}	-0.5	+6.5	V
DC input voltage	V_{IN}	-0.5	V_{DD} + 0.5	V
Continuous power dissipation	P_C		750	mW
Ambient operating temperature	T_A	-40	85	^oC
Operating junction temperature	T_J		125	^oC
Storage temperature range	T_S	-55	150	^oC

*Note: Operating conditions exceeding those listed in Absolute Maximum Ratings may cause permanent failure. Exposure to absolute maximum ratings for extended periods may impair device reliability.

THERMAL CHARACTERISTICS

Parameter	Min	Typ	Max	Unit	Test Conditions
Thermal Resistance: junction to ambient			46	$^oC/W$	0 ft/min linear airflow

POWER REQUIREMENTS

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{DD}	4.75	5.0	5.25	V	
V_{AGC}	V_{DD} - 0.3		V_{DD} - 0.62	V	Derived from V_{DD} via a 1N914 or 1N4148 diode.
I_{DD}			100	mA	V_{DD} = 5.25V
I_{AGC}			20	mA	V_{AGC} = 4.63V
P_{DD}			525	mW	V_{DD} = 5.25V *
P_{AGC}			93	mW	V_{AGC} = 4.75V *

* with inputs switching and outputs terminated.

INPUT AND OUTPUT PARAMETERS

Input Parameters For TTL

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}	2.0		V_{DD}+0.3	V	4.75 ≤V_{DD} ≤ 5.25
V_{IL}	-0.3		0.8	V	4.75 ≤V_{DD} ≤ 5.25
Input leakage current			10	µA	V_{DD} = 5.25
Input capacitance		5.5		pF	

Input Parameters For TTLr

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}	2.0		V_{DD}+0.3	V	4.75 ≤V_{DD} ≤ 5.25
V_{IL}	-0.3		0.8	V	4.75 ≤V_{DD} ≤ 5.25
Input leakage current		50	120	µA	V_{DD} = 5.25
Input capacitance		5.5		pF	

Note: Input has a 100K (nominal) internal pull-up resistor.

Input Parameters For CMOSr

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}	2.0		V_{DD}+0.3	V	4.75 ≤V_{DD} ≤ 5.25
V_{IL}	-0.3		0.8	V	4.75 ≤V_{DD} ≤ 5.25
Input leakage current		50	120	µA	V_{DD} = 5.25
Input capacitance		5.5		pF	

Note: Input has a 100K (nominal) internal pull-up resistor.

Output Parameters For TTL2mA

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{OH}	V_{DD} - 0.5			V	V_{DD} = 4.75; I_{OH} = -1.0 mA
V_{OL}			0.4	V	V_{DD} = 4.75; I_{OL} = 2.0 mA
I_{OL}			2.0	mA	
I_{OH}			-1.0	mA	

Parameter	Min	Typ	Max	Unit	Test Conditions
t_{RISE}	5.5	12.5	18.2	ns	C_{LOAD} = 15pF
t_{FALL}	2.3	4.4	6.5	ns	C_{LOAD} = 15pF

Output Parameters For TTL4mA

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{OH}	V_{DD} - 0.5			V	V_{DD} = 4.75; I_{OH} = -2.0 mA
V_{OL}			0.4	V	V_{DD} = 4.75; I_{OL} = 4.0 mA
I_{OL}			4.0	mA	
I_{OH}			-2.0	mA	
t_{RISE}	2.8	6.5	9.2	ns	C_{LOAD} = 15 pF
t_{FALL}	1.3	2.3	3.4	ns	C_{LOAD} = 15 pF

Output Parameters For TTL24mA

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{OH}	V_{DD} - 0.5			V	V_{DD} = 4.75; I_{OH} = -12.0 mA
V_{OL}			0.4	V	V_{DD} = 4.75; I_{OL} = 24.0 mA
I_{OL}			24.0	mA	
I_{OH}			-12.0	mA	
t_{RISE}	0.8	1.4	1.8	ns	C_{LOAD} = 25 pF
t_{FALL}	0.5	0.8	1.0	ns	C_{LOAD} = 25 pF

Output Parameters For CMOS8mA

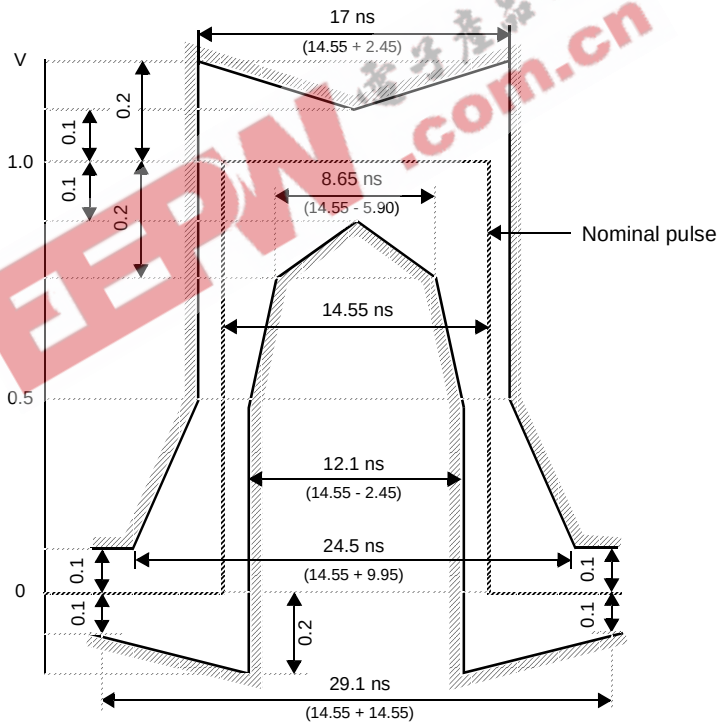
Parameter	Min	Typ	Max	Unit	Test Conditions
V_{OH}	V_{DD} - 0.5			V	V_{DD} = 4.75; I_{OH} = -8.0 mA
V_{OL}			0.4	V	V_{DD} = 4.75; I_{OL} = 8.0 mA
I_{OL}			8.0	mA	
I_{OH}			-8.0	mA	
t_{RISE}	1.3	2.4	3.8	ns	C_{LOAD} = 25 pF
t_{FALL}	1.1	1.8	2.5	ns	C_{LOAD} = 25 pF

TIMING CHARACTERISTICS

Detailed timing diagrams for the MRT are illustrated in Figures 3 through 9. All output times are measured with maximum load capacitance appropriate for the pin type. Timing parameters are measured at voltage levels of $(V_{IH} + V_{IL})/2$ for input signals or $(V_{OH} + V_{OL})/2$ for output signals.

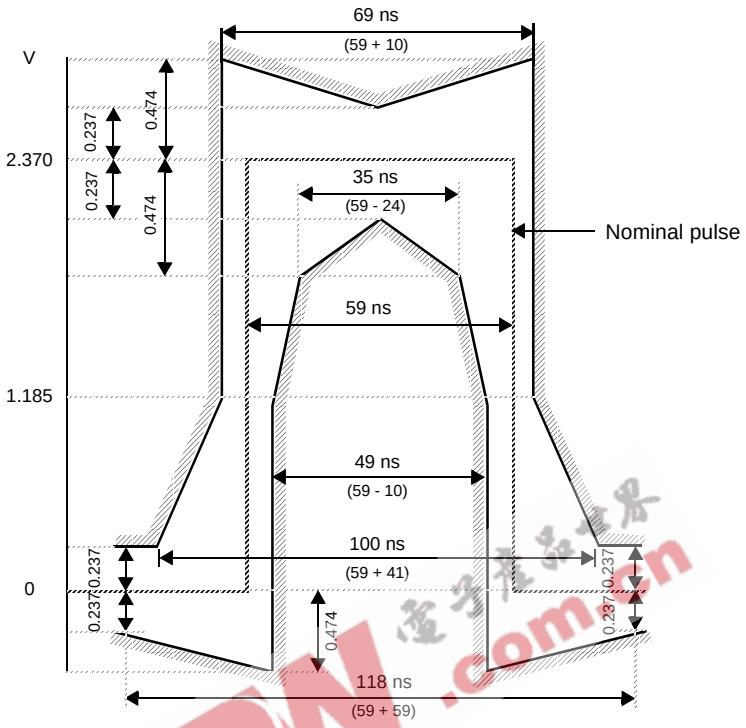
Line Side Timing Characteristics

The line side timing characteristics of the MRT are designed so that the line output at the transformer output meets the pulse shapes specified in ITU-T Rec. G.703 for 34 and 8 Mbit/s operation and the NTT Technical Reference for High-Speed Digital Leased Circuit Services for 6 Mbit/s operation. The pulse masks for each of the three modes of operation are shown in Figures 3, 4, and . Refer to the corresponding standard cited in each case for further details regarding the interface. The output circuits to be used are shown in Figures 12, 13 and 14.



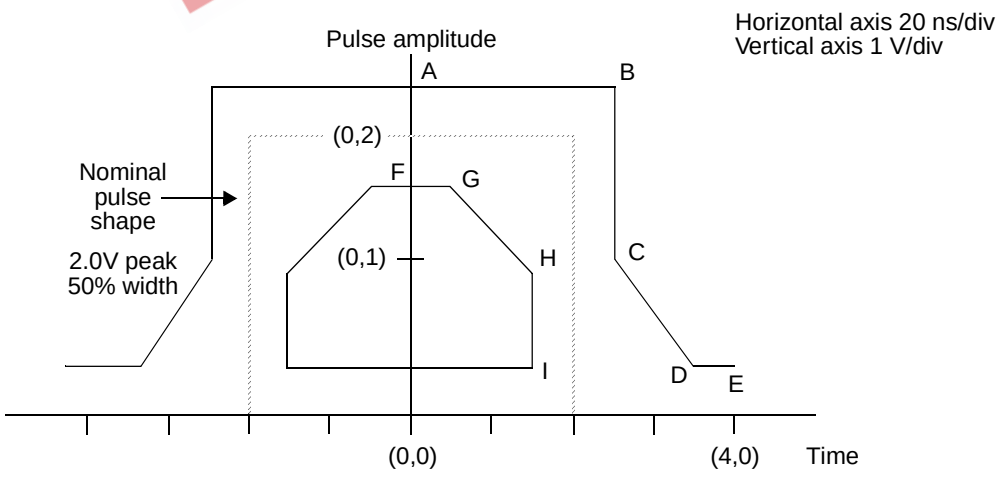
Reference: ITU-T Recommendation G.703

Figure 3. Pulse Mask at the 34368 kbit/s Interface



Reference: ITU-T Recommendation G.703

Figure 4. Pulse Mask at the 8448 kbit/s Interface



Coordinates of each point

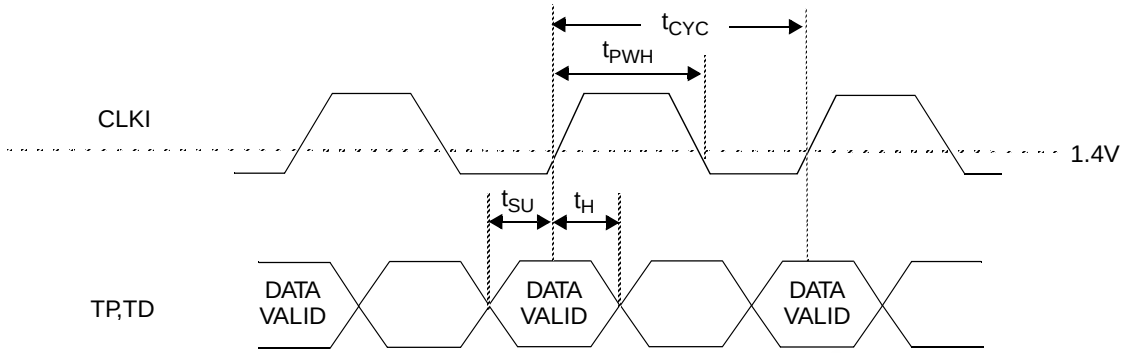
A : (0.0, 2.3)	F : (0.0, 1.7)
B : (2.4, 2.3)	G : (0.4, 1.7)
C : (2.4, 1.0)	H : (1.6, 0.9)
D : (3.2, 0.3)	I : (1.6, 0.3)
E : (4.0, 0.3)	

Reference: NTT Technical Reference for High-Speed Digital Leased Circuit Services (Third edition, 1990)

Figure 5. Pulse Mask at the 6312 kbit/s Interface

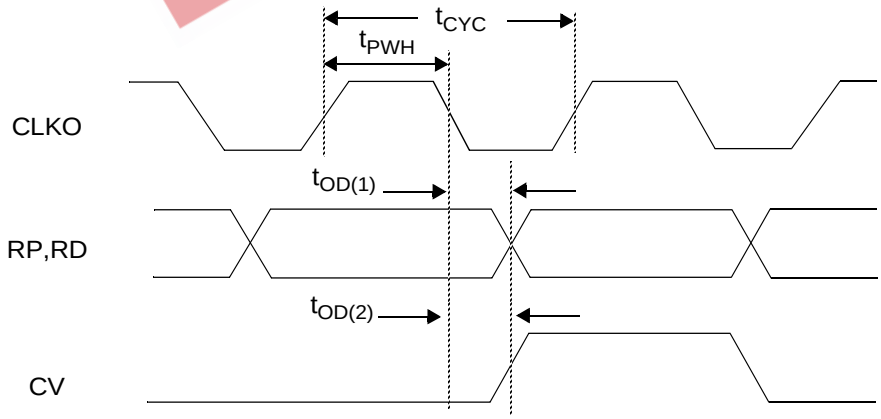
Terminal Side Timing Characteristics

Figure 6. NRZ Transmit Input Timing



Parameter	Symbol	Min	Typ	Max	Unit
CLKI clock period	t_{CYC}		(Note 2)		ns
CLKI duty cycle (t_{PWH}/t_{CYC}) (Note 1)	--	45		55	%
TP,TD set-up time to CLKI↑	t_{SU}	3			ns
TP,TD hold time after CLKI↑	t_H	2			ns

Figure 7. NRZ Receive Output Timing



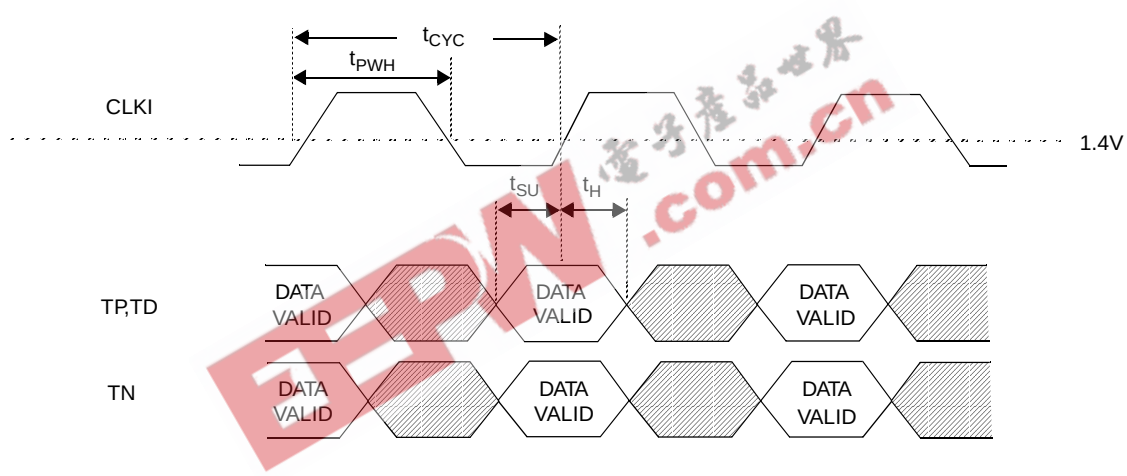
Parameter	Symbol	Min	Typ	Max	Unit
CLKO clock period	t_{CYC}		(Note 2)		ns
CLKO duty cycle (t_{PWH}/t_{CYC}) (Note 1)	--	45		55	%
RP,RD output delay after CLKO↓	$t_{OD(1)}$	-5		5	ns
CV output delay after CLKO↓ (Note 3)	$t_{OD(2)}$	-5		5	ns

See Notes on next page.

Notes:

1. CLKO symmetry is measured about the 50% amplitude point.
2. 158.4 ns for 6312 kbit/s; 118.4 ns for 8448 kbit/s; 29.10 ns for 34368 kbit/s.
3. The CV pulse occurs at the same time as the errored bit is presented at the output.

Figure 8. P and N Rail Transmit Input Timing

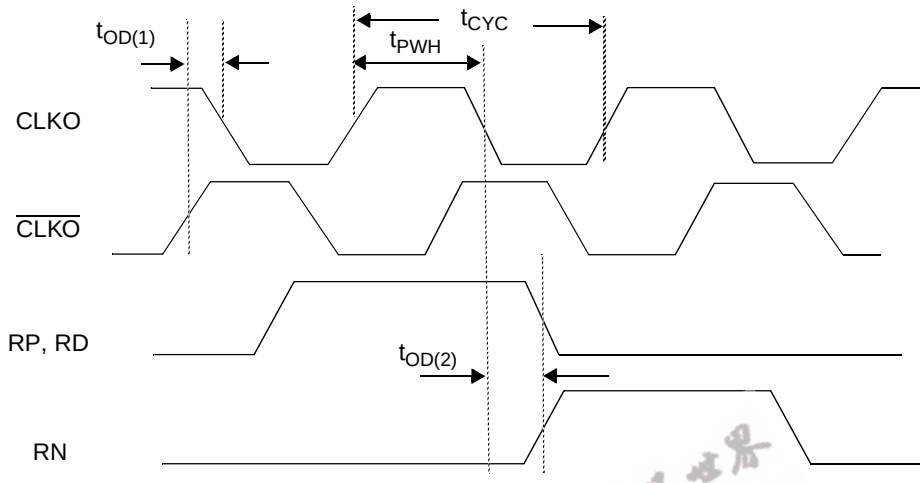


Parameter	Symbol	Min	Typ	Max	Unit
CLKI clock period	t_{CYC}		(Note 2)		ns
CLKI duty cycle (t_{PWH}/t_{CYC}) (Note 1)	--	45		55	%
TP,TD & TN set-up time to CLKI↑	t_{SU}	3			ns
TP,TD & TN hold time after CLKI↑	t_H	2			ns

Notes:

1. CLKI symmetry is measured about the 1.4VDC threshold in order to assure symmetric output waveforms.
2. 158.4 ns for 6312 kbit/s; 118.4 ns for 8448 kbit/s; 29.10 ns for 34368 kbit/s.

Figure 9. P and N Rail Receive Output Timing



Parameter	Symbol	Min	Typ	Max	Unit
CLKO clock period	t_{CYC}		(Note 2)		ns
CLKO duty cycle (t_{PWH}/t_{CYC}) (Note 1)	--	45		55	%
CLKO↓ output delay after $\overline{CLKO}$↑	$t_{OD(1)}$			2	ns
RP, RD and RN output delay after CLKO↓	$t_{OD(2)}$	-5		6	ns

Notes:

1. CLKO symmetry is measured about the 50% amplitude point.
2. 158.4 ns for 6312 kbit/s; 118.4 ns for 8448 kbit/s; 29.10 ns for 34368 kbit/s.

OPERATION

POWER SUPPLY, GROUND AND PLL CONNECTIONS

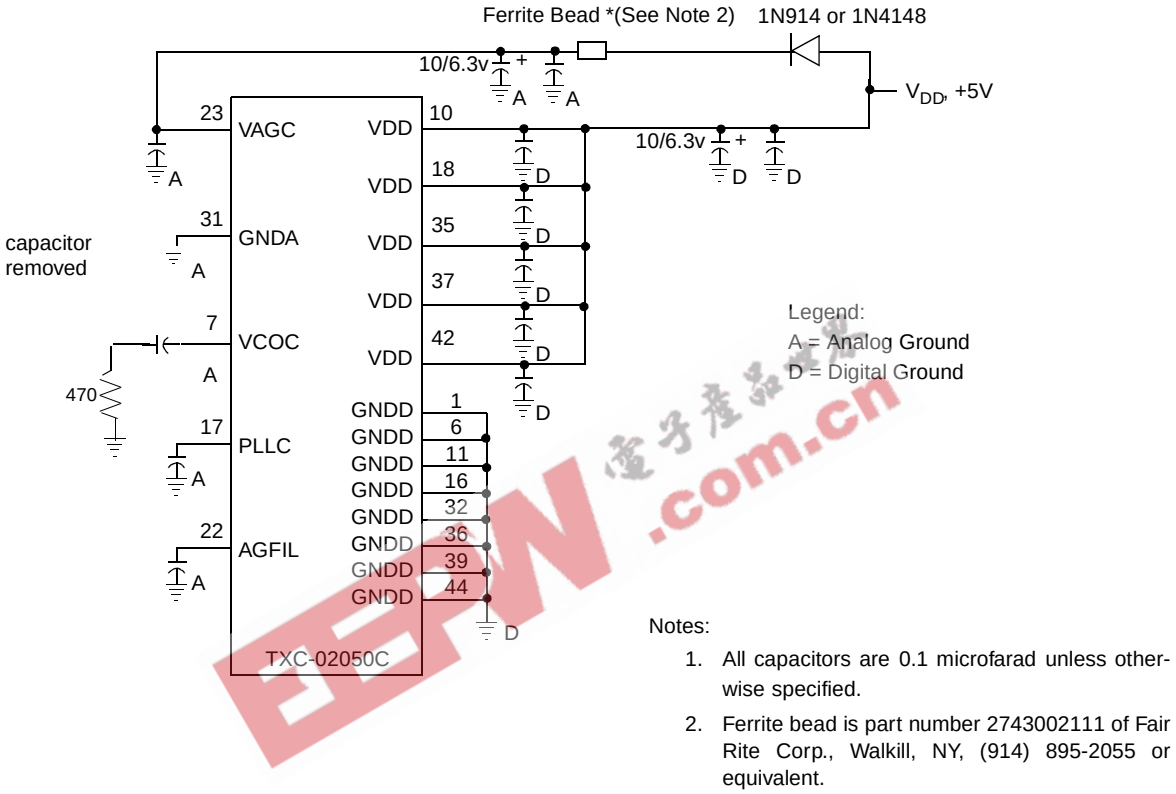
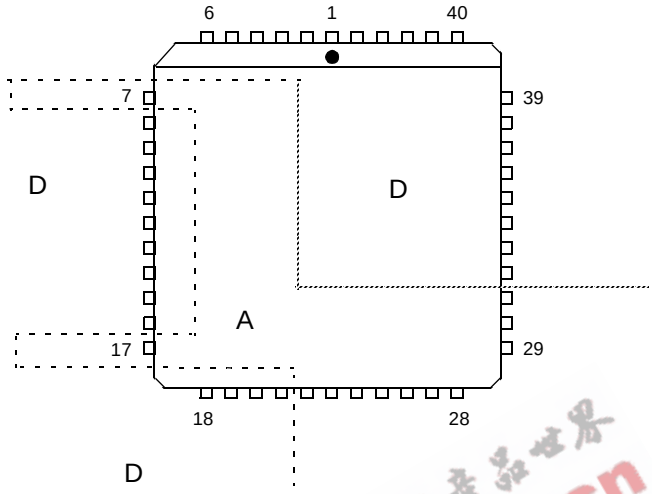


Figure 10. MRT Power Supply, Ground and PLL Connections

The MRT device has separate power supply pins labeled VDD and VAGC. The VAGC supply pin is connected to the internal AGC amplifier and is derived from the VDD supply as indicated in Figure 10. Separate bypass networks must be used for connecting the VDD and VAGC supply pins on the MRT to +5V. The bypass network on the VAGC pin consists of a 1N4148 or 1N914 diode, a ferrite bead and a 10 microfarad 6.3 volt (tantalum) capacitor connected to analog ground in parallel with a 0.1 microfarad capacitor, as shown in Figure 10. TranSwitch recommends that the 0.1 microfarad decoupling capacitors be of RF quality and that they be connected in close proximity to the device.

The recommended ground plane for the MRT device is a common ground plane for both analog and digital ground. The ground plane beneath and approximately 0.25" beyond the physical dimensions of the MRT needs to be separated into analog and digital grounds by notching approximately 25 mils of the copper ground plane, as shown in Figure 11. Additional MRT application design considerations are discussed in TranSwitch Application Note AN-517 “Design Considerations for use of the MRT device with the E2/E3F Device.”



Legend: --- 25 mil notching of ground plane under device to separate analog (A) and digital (D) ground areas

Figure 11. Ground Plane of Application Circuit Board

OVERVIEW

Line Side Input Impedance

The input impedance of the MRT is a function of the state of the $\overline{\text{LOW}}$ lead and the operating rate. The table below lists the input impedance of the MRT at the operating line rates (which are 1/2 the bit rates).

MRT Input Impedance

Condition	Minimum Input Impedance, | Z |
$\overline{\text{LOW}}$ = 1, line rate = 17184 kHz (E3)	1260 ohms
$\overline{\text{LOW}}$ = 0, line rate = 4224 kHz (E2)	2390 ohms
$\overline{\text{LOW}}$ = 0, line rate = 3156 kHz (JT2)	3670 ohms

Line Side Input Sensitivity

The input voltage sensitivity of the MRT depends on the state of the $\overline{\text{LOW}}$ lead as shown in the table below.

MRT Input Sensitivity

$\overline{\text{LOW}}$ Lead	Rate, Mbit/s	Input Sensitivity (peak volts) Min	Max
0	6/8 (JT2/E2)	0.5	2.7
1	34 (E3)	0.15	1.1

Line Side Input Circuit

The circuit shown in Figure 12 illustrates the components required for operating the MRT device at 34368, 8448 or 6312 kbit/s. The 1:1 transformer should have a frequency response of 0.2 MHz ≤ f ≤ 80 MHz with an insertion loss of 1 dB, maximum (suitable devices include Coilcraft part no. WB-1010 and Pulse Engineering part no. PE-65966). This gives return loss and isolation voltage values that meet or exceed requirements.

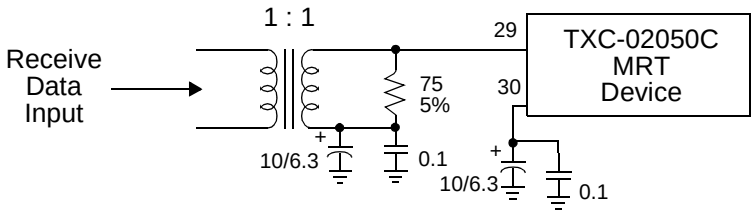


Figure 12. Line Side Input Circuit

Line Side Output Characteristics

The line side output of the MRT switches from “rail to rail” on both of its output leads, TPO and TNO. This provides the maximum voltage swing, and makes the output voltage depend on the +5 volt power supply input to the chip. The external circuit design must therefore be done with care in order to assure meeting the amplitude requirements.

Line Side Output Circuits

Figure 13 illustrates the output circuit required for operating the MRT device in a 34368 kbit/s application without a socket. The transformer and resistors shown assure that the output waveform meets the ITU-T mask for 34368 kbit/s transmission and that the MRT device is operated within the current limits of the TTL24mA output parameters. The 1:2 transformer should have a frequency response of 0.2 MHz ≤ f ≤ 80 MHz with an insertion loss of 1dB, maximum (suitable devices include Coilcraft part no. WB-1040 and Pulse Engineering part no. PE-65969).

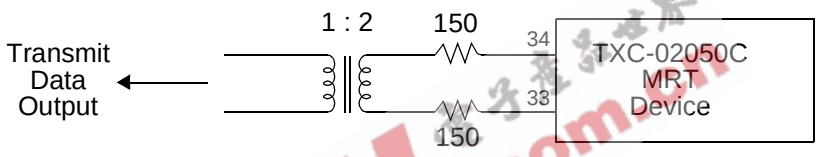


Figure 13. Line Side Output Circuit Outline - No Socket (34368 kbit/s)

Figure 14 shows a variation of the circuit in Figure 13. This circuit improves performance in applications when a plastic device is mounted in a socket. The additional low-pass filter compensates for possible overshoot caused by inductance created by the device/socket interface. The 1:2 transformer should have a frequency response of 0.2 MHz ≤ f ≤ 80 MHz with an insertion loss of 1dB, maximum (suitable devices include Coilcraft part no. WB-1040 and Pulse Engineering part no. PE-65969).

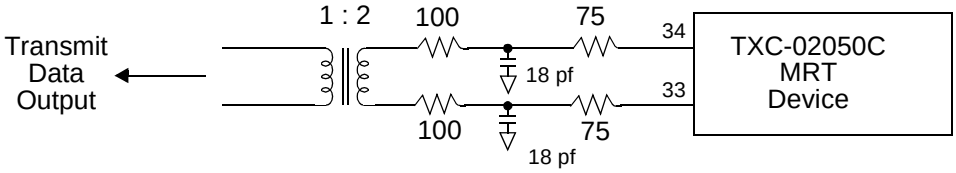


Figure 14. Line Side Output Circuit Outline - Socket (34368 kbit/s)

The peak voltage and current output requirements for 6312 and 8448 kbit/s operation are different from those for 34368 kbit/s operation. Figure 15 illustrates the output circuit required for 6312 kbit/s and 8448 kbit/s operation. The 1:1 transformer should have a frequency response of 0.2 MHz ≤ f ≤ 80 MHz with an insertion loss of 1dB, maximum (suitable devices include Coilcraft part no. WB-1010 and Pulse Engineering part no. PE-65966). The transformer, drivers and resistors assure that the output waveform meets the pulse mask requirements for these rates and that the MRT device is operated within the current limits of the TTL24mA output parameters.

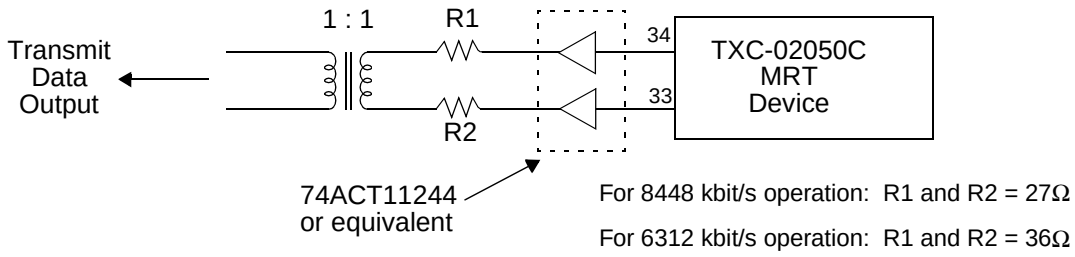


Figure 15. Line Side Output Circuit Outline (8448 and 6312 kbit/s)

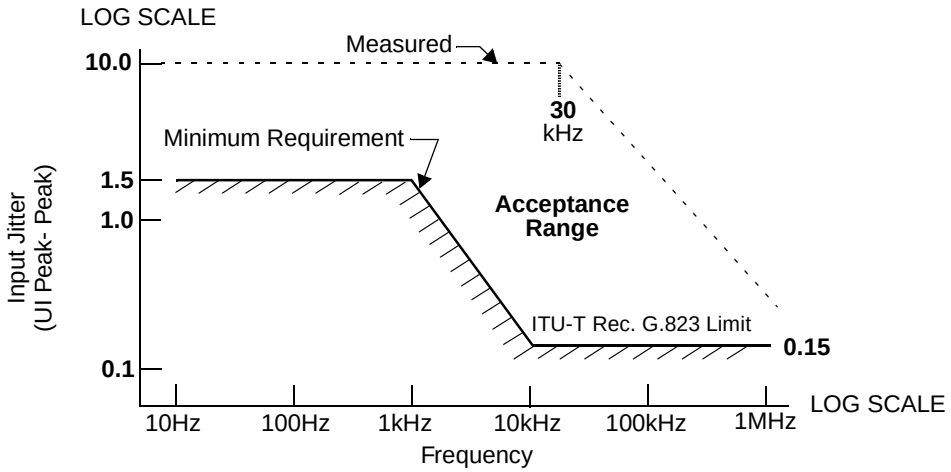
JITTER AND INTERFERING TONE TOLERANCES

The jitter measurements described in this subsection are performed using an ANRITSU model ME502B Digital Transmission Analyzer, or equivalent.

Jitter Tolerance

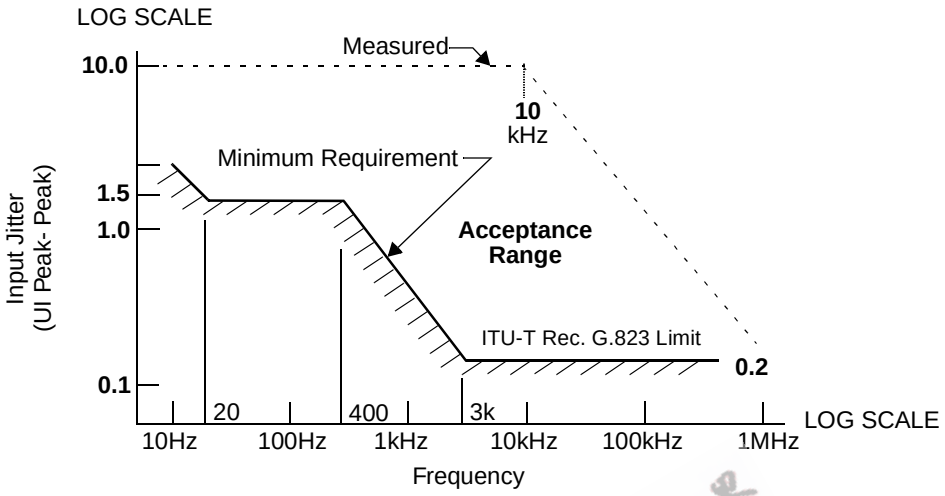
ITU-T Recommendations G.823 and JT-G703 specify that network equipment must be able to accommodate and tolerate levels of jitter up to certain specified limits. The MRT accommodates and tolerates more input jitter than the level of input jitter specified by these Recommendations.

With input jitter applied to the MRT line side receive input DI1 (pin 29), the MRT properly recovers clock, decodes the signal, and outputs error-free NRZ data over (and beyond) the ITU-T ranges specified for jitter input and frequency. Performance characteristics are shown below in Figure 16 (34368 kbit/s operation), Figure 17 (8448 kbit/s operation) and Figure 18 (6312 kbit/s operation).



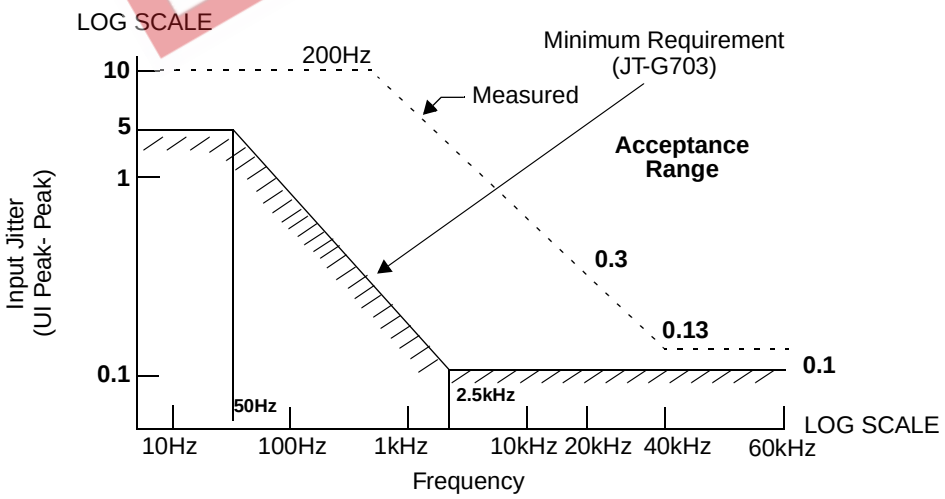
Notes: Unit Interval (UI) = 1/(System Clock Frequency) = 29.10 ns
Test conditions: V_{DD}=5V, T_A=25°C, HDB3 coding, 2^{23}-1 data pattern

Figure 16. MRT Jitter Tolerance at 34368 kbit/s



Notes: Unit Interval (UI) = 1/(System Clock Frequency) = 118.4 ns
Test conditions: V_{DD}=5V, T_A=25°C, HDB3 coding, 2^{15}-1 data pattern

Figure 17. MRT Jitter Tolerance at 8448 kbit/s



Notes: Unit Interval (UI) = 1/(System Clock Frequency) = 158.4 ns
Test conditions: V_{DD}=5V, T_A=25°C, B8ZS coding, 2^{15}-1 data pattern

Figure 18. MRT Jitter Tolerance at 6312 kbit/s

Maximum Output Jitter In Absence of Input Jitter

ITU-T Recommendation G.823 specifies that it is necessary to restrict the amount of jitter generated by individual equipment at an output port. The amount of jitter allowed is dependent on the application in which the equipment is used. For example, in a repeater application the recovered clock will be used for the transmit clock. The recovered clock will have jitter due to the sending transmitter and to clock recovery of distorted data. The jitter will be additive through each repeater. Therefore, it would be necessary to add a dejitter buffer (a PLL with a very low bandwidth, usually using a VCXO) to reduce the jitter in the recovered clock before using it as a transmit clock.

For the MRT in non-repeater applications, the maximum output jitter measurement is made on the transmit path. The recovered clock output jitter is unimportant as long as proper clocking of following devices in possible (with the exception of the above-mentioned repeater applications). The transmit clock in these cases is coming from a device such as a framer whose clock is derived from the local oscillator on the board. To make this measurement, apply a signal with known jitter characteristics to the transmitter inputs and measure the jitter at the transmitter outputs.

In the absence of applied jitter, the transmit path of the MRT introduces a maximum 0.05 Unit Intervals (UIs) peak-to-peak jitter over the following frequency ranges:

At 6.312 Mbit/s: 10 Hz to 160 kHz

At 8448 kbit/s: 20 Hz to 400 kHz

At 34368 kbit/s: 100 Hz to 800 kHz

This operation is with the MRT terminated by the external components (and component values) specified in the Pin Description Table for pin 7 (VCOC), pin 17 (PLLC), and pin 22 (AGFIL).

Jitter Transfer

Transfer of jitter through individual equipment is characterized by the relationship between the applied input jitter and the resulting output jitter as a function of frequency. ITU-T Recommendation G.823 specifies that it is important to restrict jitter gain. Figure 4 of G.823 shows a typical jitter transfer characteristic. Note that a small jitter gain is allowed. British Standard 6328: Section 8.1, 1990 gives the allowable gain as 0.5 dB.

With applied input jitter at the MRT receive input terminals, the maximum MRT receive output jitter is not greater than the level of input jitter plus a maximum of 0.05 UI peak-to-peak jitter in the range of 10 Hz to 160 kHz for 6 Mbit/s, 20 Hz to 400 kHz for 8 Mbit/s, and 100 Hz to 800 kHz for 34 Mbit/s. These values are measured by applying a controlled, sinusoidal jitter signal to pins DI1 and DI2, then measuring the jitter at the receiver output (i.e., CLKO).

This operation is with the same MRT external terminations as described in the Maximum Output Jitter section above.

Interfering Tone Tolerance

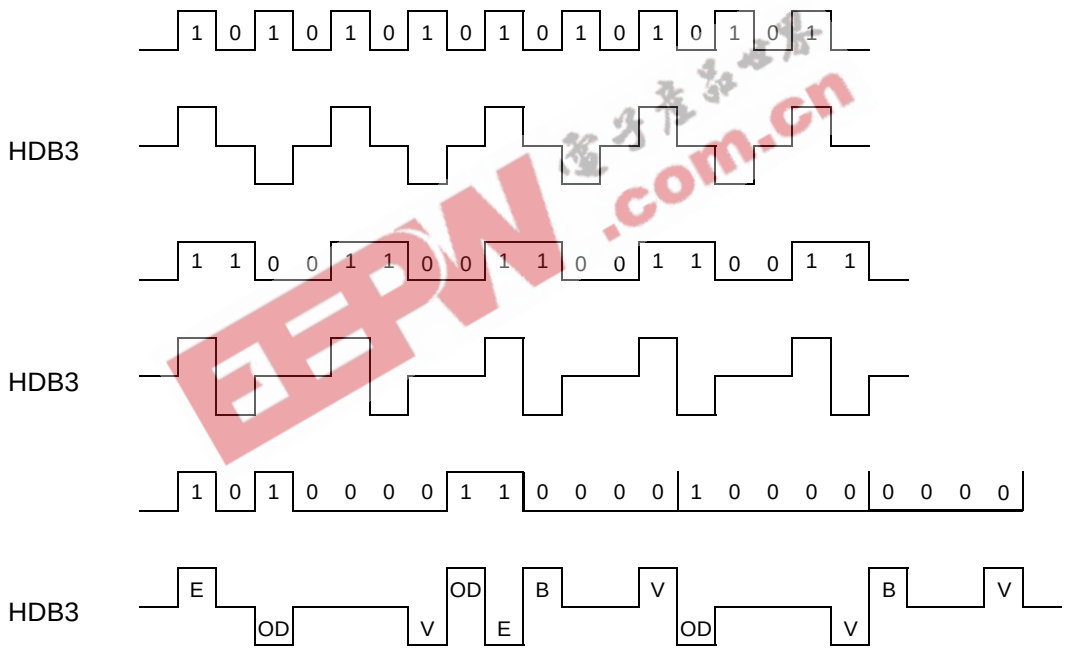
The MRT will properly recover clock and present error-free output to the receive terminal side interface in the presence of a PRBS interfering tone with the same data sequence as the data input while operating at 6, 8 or 34 Mbit/s, as specified in the following table:

PRBS* Interfering Tone Tolerance

Data Rate (kbit/s)	Tone Rate (kbit/s)	Maximum Tone Level	Data Sequence	Requirement
34368	34368 ± 100ppm	-11.5 dB	2^{23} - 1	- 20
8448	8448 ± 100ppm	-14.5 dB	2^{15} - 1	- 18.5

*PRBS = Pseudo-Random Binary Sequence

HDB3 PATTERNS



E = indicates even number of pulses since last violation (V)

OD = indicates odd number of pulses since last violation (V)

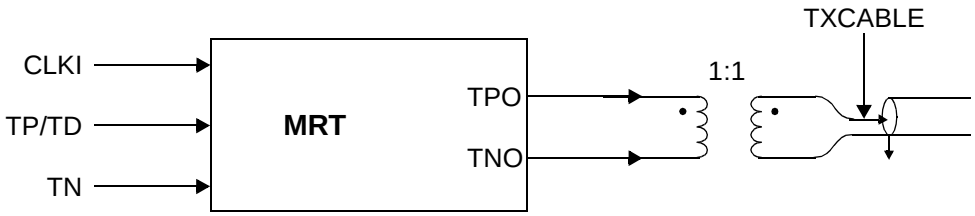
V = intentional violation of alternating plus and minus pulses used for 1's

B = pulse that follows the normal alternating Bipolar coding scheme

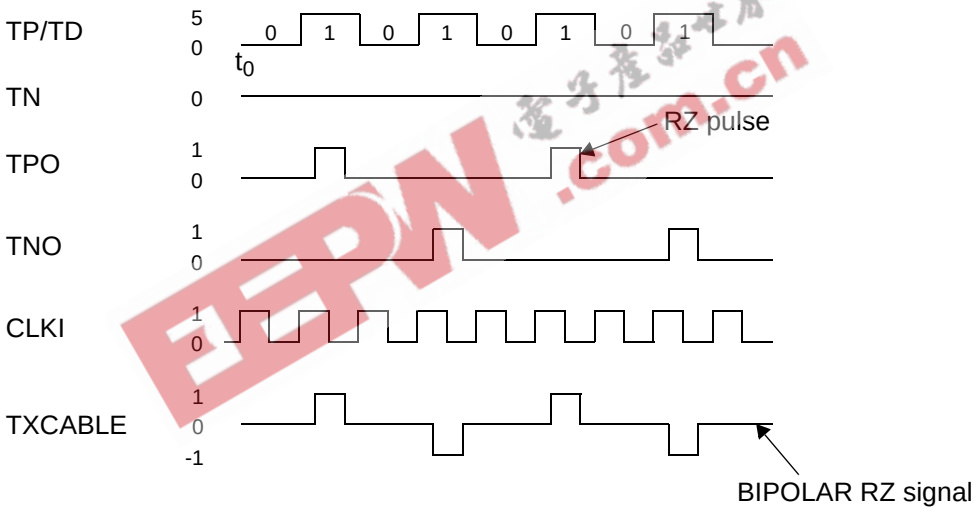
- four zeros are replaced with B00V or 000V; the substitution choice is made so that the number of pulses between violations (V's) is odd; note that sequential violations are of opposite polarity so the net charge on the transmission medium is zero.

Figure 19. Examples of HDB3 Coding

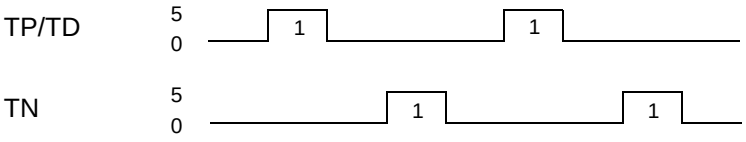
EXAMPLES OF TRANSMIT INPUT AND OUTPUT DATA (34368 KBIT/S OPERATION)



Unencoded NRZ Data (0 1 0 1 0 .....)



Encoded NRZ P & N Data (0 1 0 1 0 ....)



TPO, TNO, CLKI and TXCABLE are the same as in the unencoded NRZ case.

Figure 20. Examples of Transmit Input and Output Data (34368 kbit/s operation)

PACKAGING

The MRT device is packaged in a 44-pin plastic leaded chip carrier suitable for socket or surface mounting, as illustrated in Figure 21. All dimensions shown are in inches and are nominal unless otherwise noted.

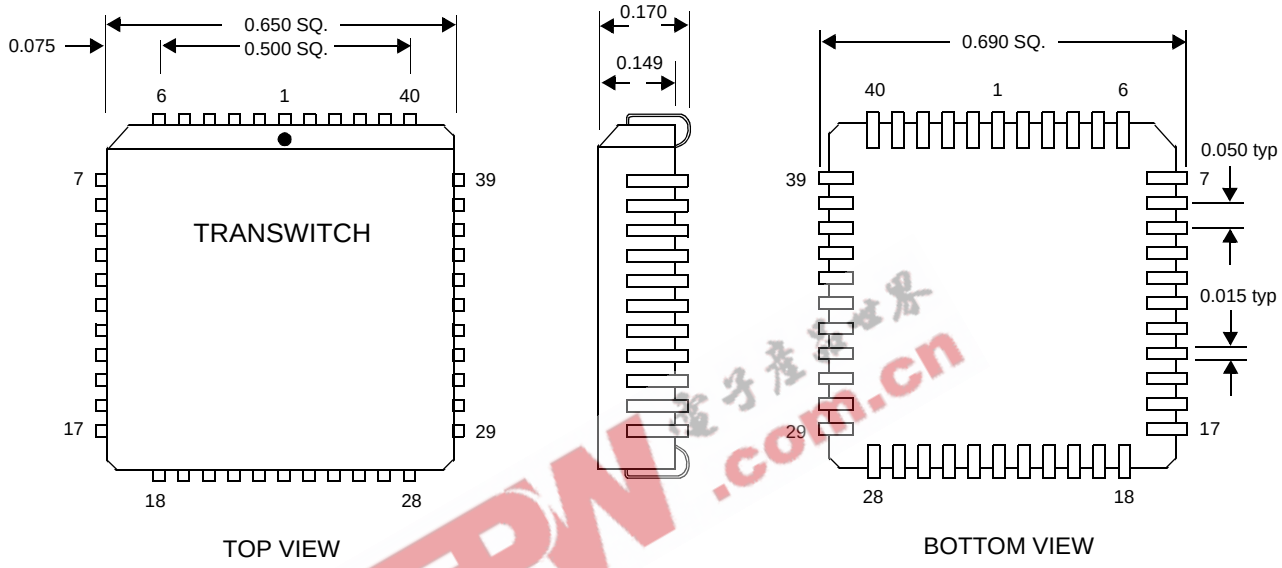


Figure 21. MRT TXC-02050C 44-Pin Plastic Lead Chip Carrier

ORDERING INFORMATION

Part Number: TXC-02050CIPL 44-pin Plastic Leaded Chip Carrier

RELATED PRODUCTS

TXC-03701 E2/E3F Framer VLSI device. The E2/E3 Framer directly interfaces with the MRT and provides multi-mode framing for ITU-T Rec. G.751/G.753 (34368 kbit/s) or ITU-T Rec. G.742/G.745 (8448 kbit/s) signals.

TXC-03702 JT2F Framer VLSI device. The JT2F Framer directly interfaces with the MRT and provides framing for ITU-T Rec. G.704 (6312 kbit/s) signals.

TXC-06125 XBERT VLSI device (Bit Error Rate Generator / Receiver). Programmable multi-rate test pattern generator and receiver in a single chip with bit-serial, nibble-parallel or byte-parallel interface capability.

TXC-21055 MRT Evaluation Board. A complete ready-to-use single board that demonstrates the functions and features of the MRT line interface VLSI device.

STANDARDS DOCUMENTATION SOURCES

Telecommunication technical standards and reference documentation may be obtained from the following organizations:

ANSI (U.S.A.):

American National Standards Institute
25 West 43rd Street
New York, New York 10036
Tel: (212) 642-4900
Fax: (212) 398-0023
Web: www.ansi.org

The ATM Forum (U.S.A., Europe, Asia):

404 Balboa Street
San Francisco, CA 94118
Tel: (415) 561-6275
Fax: (415) 561-6120
Web: www.atmforum.com

ATM Forum Europe Office

Kingsland House - 5th Floor
361-373 City Road
London EC1 1PQ, England
Tel: 20 7837 7882
Fax: 20 7417 7500

ATM Forum Asia-Pacific Office

Hamamatsucho Suzuki Building 3F
1-2-11, Hamamatsucho, Minato-ku
Tokyo 105-0013, Japan
Tel: 3 3438 3694
Fax: 3 3438 3698

Bellcore (See Telcordia)

CCITT (See ITU-T)

EIA (U.S.A.):

Electronic Industries Association
Global Engineering Documents
15 Inverness Way East
Englewood, CO 80112
Tel: (800) 854-7179 (within U.S.A.)
Tel: (303) 397-7956 (outside U.S.A.)
Fax: (303) 397-2740
Web: www.global.ihs.com

ETSI (Europe):

European Telecommunications Standards Institute
650 route des Lucioles
06921 Sophia-Antipolis Cedex, France
Tel: 4 92 94 42 00
Fax: 4 93 65 47 16
Web: www.etsi.org

GO-MVIP (U.S.A.):

The Global Organization for Multi-Vendor Integration Protocol (GO-MVIP)
3220 N Street NW, Suite 360
Washington, DC 20007

Tel: (800) 669-6857 (within U.S.A.)
Tel: (903) 769-3717 (outside U.S.A.)
Fax: (903) 769-3818
Web: www.mvip.org

ITU-T (International):

Publication Services of International Telecommunication Union
Telecommunication Standardization Sector
Place des Nations, CH 1211
Geneve 20, Switzerland

Tel: 22 730 5852
Fax: 22 730 5853
Web: www.itu.int

MIL-STD (U.S.A.):

DODSSP Standardization Documents Ordering Desk
Building 4 / Section D
700 Robbins Avenue
Philadelphia, PA 19111-5094

Tel: (215) 697-2179
Fax: (215) 697-1462
Web: www.dodssp.daps.mil

PCI SIG (U.S.A.):

PCI Special Interest Group
5440 SW Westgate Dr., #217
Portland, OR 97221

Tel: (800) 433-5177 (within U.S.A.)
Tel: (503) 291-2569 (outside U.S.A.)
Fax: (503) 297-1090
Web: www.pcisig.com

Telcordia (U.S.A.):

Telcordia Technologies, Inc.
Attention - Customer Service
8 Corporate Place Rm 3A184
Piscataway, NJ 08854-4157

Tel: (800) 521-2673 (within U.S.A.)
Tel: (732) 699-2000 (outside U.S.A.)
Fax: (732) 336-2559
Web: www.telcordia.com

TTC (Japan):

TTC Standard Publishing Group of the Telecommunication Technology Committee
Hamamatsu-cho Suzuki Building
1-2-11, Hamamatsu-cho, Minato-ku
Tokyo 105-0013, Japan

Tel: 3 3432 1551
Fax: 3 3432 1553
Web: www.ttc.or.jp

LIST OF DATA SHEET CHANGES

This change list identifies those areas within the updated MRT Data Sheet that have technical differences relative to the superseded MRT Data Sheet:

Updated MRT "C" Data Sheet: Edition 1, May 2002

Superseded MRT Data Sheet: Edition 3, April 1994

The page numbers indicated below of the updated data sheet include changes relative to the superseded data sheet.

Page Number of Updated Data Sheet	Summary of the Change
All	Changed edition number and date.
All	Changed GND to GNDD.
1	Made changes to items 3, 5, 6, 7 and 10 of the Feature list.
1	Added items 9, 11 and 12 to the Feature list.
1	Modified the first paragraph of Description section. Changed Patent information.
2	Added Table of Contents and List of Figures.
3	Modified Figure 1 and added product number to the figure title.
4	Made changes to Block Diagram Description section.
5	Added product number to the Figure title 2.
6	Made changes to Name/Function column for VDD, GNDD, VAGC, GNDA, TNO and TPO.
6	Added a Note below the table to explain Type column heading for 'Line Side I/O' section.
6-7	Made changes to Type and Name/Function columns for RN, RP/RD, $\overline{\text{CLKO}}$ and CLKO.
7-10	Made changes to Name/Function column for CLKI, $\overline{\text{TXLOC}}$, LQLTY, $\overline{\text{RXLOS}}$, DCK, $\overline{\text{LOW}}$, EQB1, EQB0, VCOC and AGFIL.
10	Made changes to I/O/P column for VCOC, PLLC, AGFIL and added Note below the table.
11	Added Test Conditions column to the second table. Made changes to V_{AGC} row of the last table. Changed Test Condition for I_{AGC} and changed Max for P_{AGC} to the last table. Changed in first table Max. Operating Junction Temperature. Added a note below the table.

Page Number of Updated Data Sheet	Summary of the Change
12	Added Max for V_{IH} and Min for V_{IL} of the first three tables.
14-18	Made changes to Timing Characteristics section.
19-24	Made changes to Operation section. Removed capacitor from pin 31 and Note 3 from Figure 10. Updated Jitter requirements in Figure 18.
28	Made minor changes to Packaging section.
29	Added item 3 to the Related Products section.
30-31	Updated the Standards Documentation Sources section.
32-33	Updated List of Data Sheet Changes.
35	Added Documentation Update Registration Form.

DOCUMENTATION UPDATE REGISTRATION FORM

If you would like to receive updated documentation for selected devices as it becomes available, please provide the information requested below (print clearly or type) then tear out this page, fold and mail it to the Marketing Communications Department at TranSwitch. Marketing Communications will ensure that the relevant Product Information Sheets, Data Sheets, Application Notes, Technical Bulletins and other publications are sent to you. You may also choose to provide the same information by fax **(203.926.9453)**, or by e-mail **(info@txc.com)**, or by telephone **(203.929.8810)**. Most of these documents will also be made immediately available for direct download as Adobe PDF files from the TranSwitch World Wide Web Site (**www.transwitch.com**).

Name: _____

Company: _____ Title: _____

Dept./Mailstop: _____

Street: _____

City/State/Zip: _____

If located outside U.S.A., please add - Country: _____ Postal Code: _____

Telephone: _____ Ext.: _____ Fax: _____

E-mail: _____

Please provide the following details for the managers in charge of the following departments at your company location.

Department	Title	Name
Company/Division	_____	_____
Engineering	_____	_____
Marketing	_____	_____

Please describe briefly your intended application(s) and indicate whether you would like to have a TranSwitch applications engineer contact you to provide further assistance:

_____

_____

_____

_____

If you are also interested in receiving updated documentation for other TranSwitch device types, please list them below rather than submitting separate registration forms:

_____ _____ _____ _____ _____ _____ _____

_____ _____ _____ _____ _____ _____ _____

Please fold, tape and mail this page (see other side) or fax it to Marketing Communications at 203.926.9453.

TRANSWITCH®

Engines for Global Connectivity

(Fold back on this line second, then tape closed, stamp and mail.)

TRANSWITCH

3 Enterprise Drive
Shelton, CT 06484-4694
U.S.A.

First Class Postage Required

TranSwitch Corporation
Attention: Marketing Communications Dept.
3 Enterprise Drive
Shelton, CT 06484-4694
U.S.A.

(Fold back on this line first.)

Please complete the registration form on this back cover sheet, and fax or mail it, if you wish to receive updated documentation on this TranSwitch product as it becomes available.