

74F74 Dual D-Type Positive Edge-Triggered Flip-Flop

General Description

The F74 is a dual D-type flip-flop with Direct Clear and Set inputs and complementary (Q, \bar{Q}) outputs. Information at the input is transferred to the outputs on the positive edge of the clock pulse. Clock triggering occurs at a voltage level of the clock pulse and is not directly related to the transition time of the positive-going pulse. After the Clock Pulse input threshold voltage has been passed, the Data input is locked out and information present will not be transferred to

the outputs until the next rising edge of the Clock Pulse input.

Asynchronous Inputs:

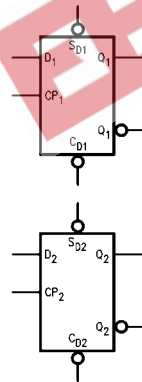
- LOW input to \bar{S}_D sets Q to HIGH level
- LOW input to \bar{C}_D sets Q to LOW level
- Clear and Set are independent of clock
- Simultaneous LOW on \bar{C}_D and \bar{S}_D makes both Q and \bar{Q} HIGH

Ordering Code:

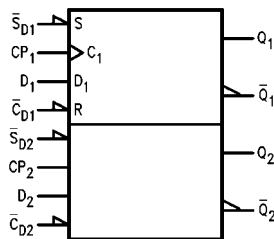
| Order Number | Package Number | Package Description |
|--------------|----------------|---|
| 74F74SC | M14A | 14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150 Narrow |
| 74F74SJ | M14D | 14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide |
| 74F74PC | N14A | 14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide |

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

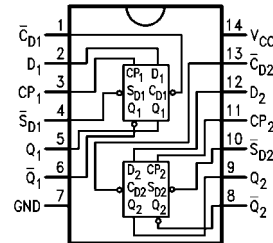
Logic Symbols



IEEE/IEC



Connection Diagram



Unit Loading/Fan Out

| Pin Names | Description | U.L. | |
|--|---|----------|---|
| | | HIGH/LOW | Input I_{IH}/I_{IL} Output I_{OH}/I_{OL} |
| D_1, D_2 | Data Inputs | 1.0/1.0 | 20 μ A/-0.6 mA |
| CP_1, CP_2 | Clock Pulse Inputs (Active Rising Edge) | 1.0/1.0 | 20 μ A/-0.6 mA |
| $\overline{C}_{D1}, \overline{C}_{D2}$ | Direct Clear Inputs (Active LOW) | 1.0/3.0 | 20 μ A/-1.8 mA |
| $\overline{S}_{D1}, \overline{S}_{D2}$ | Direct Set Inputs (Active LOW) | 1.0/3.0 | 20 μ A/-1.8 mA |
| $Q_1, \overline{Q}_1, Q_2, \overline{Q}_2$ | Outputs | 50/33.3 | -1 mA/20 mA |

Truth Table

| Inputs | | | | Outputs | |
|------------------|------------------|------------|---|---------|------------------|
| \overline{S}_D | \overline{C}_D | CP | D | Q | \overline{Q} |
| L | H | X | X | H | L |
| H | L | X | X | L | H |
| L | L | X | X | H | H |
| H | H | \nearrow | h | H | L |
| H | H | \searrow | l | L | H |
| H | H | L | X | Q_0 | \overline{Q}_0 |

H (h) = HIGH Voltage Level

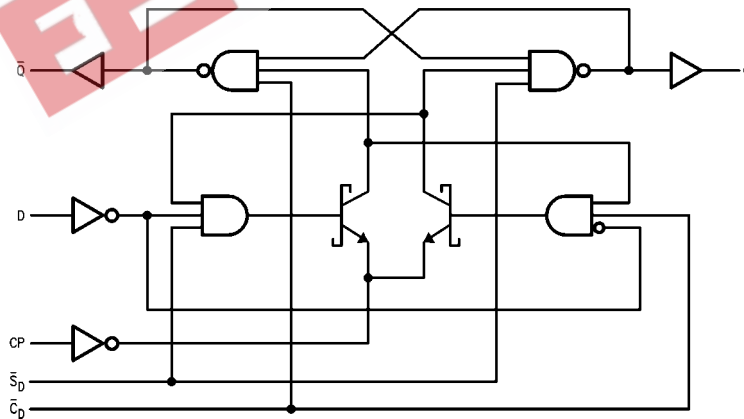
L (l) = LOW Voltage Level

X = Immaterial

 Q_0 = Previous Q (\overline{Q}) before LOW-to-HIGH Clock Transition

Lower case letters indicate the state of the referenced input or output one setup time prior to the LOW-to-HIGH clock transition.

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

| Absolute Maximum Ratings (Note 1) | | Recommended Operating Conditions | |
|--|--------------------------------------|----------------------------------|----------------|
| Storage Temperature | -65°C to +150°C | Free Air Ambient Temperature | 0°C to +70°C |
| Ambient Temperature under Bias | -55°C to +125°C | Supply Voltage | +4.5V to +5.5V |
| Junction Temperature under Bias | -55°C to +150°C | | |
| V _{CC} Pin Potential to Ground Pin | -0.5V to +7.0V | | |
| Input Voltage (Note 2) | -0.5V to +7.0V | | |
| Input Current (Note 2) | -30 mA to +5.0 mA | | |
| Voltage Applied to Output in HIGH State (with V _{CC} = 0V) | | | |
| Standard Output | -0.5V to V _{CC} | | |
| 3-STATE Output | -0.5V to +5.5V | | |
| Current Applied to Output in LOW State (Max) | twice the rated I _{OL} (mA) | | |
| ESD Last Passing Voltage (Min) | 4000V | | |

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

DC Electrical Characteristics

| Symbol | Parameter | Min | Typ | Max | Units | V _{CC} | Conditions |
|------------------|-----------------------------------|---------------------|------|------|-------|-----------------|--|
| V _{IH} | Input HIGH Voltage | 2.0 | | | V | | Recognized as a HIGH Signal |
| V _{IL} | Input LOW Voltage | | | 0.8 | V | | Recognized as a LOW Signal |
| V _{CD} | Input Clamp Diode Voltage | | | -1.2 | V | Min | I _{IN} = -18 mA |
| V _{OH} | Output HIGH Voltage | 10% V _{CC} | 2.5 | | V | Min | I _{OH} = -1 mA |
| | | 5% V _{CC} | 2.7 | | | | I _{OH} = -1 mA |
| V _{OL} | Output LOW Voltage | 10% V _{CC} | | 0.5 | V | Min | I _{OL} = 20 mA |
| I _{IH} | Input HIGH Current | | | 5.0 | μA | Max | V _{IN} = 2.7V |
| I _{BVI} | Input HIGH Current Breakdown Test | | | 7.0 | μA | Max | V _{IN} = 7.0V |
| I _{CEx} | Output HIGH Leakage Current | | | 50 | μA | Max | V _{OUT} = V _{CC} |
| V _{ID} | Input Leakage Test | 4.75 | | | V | 0.0 | I _{ID} = 1.9 μA All Other Pins Grounded |
| I _{OD} | Output Leakage Circuit Current | | | 3.75 | μA | 0.0 | V _{IOD} = 150 mV All Other Pins Grounded |
| I _{IL} | Input LOW Current | | | -0.6 | mA | Max | V _{IN} = 0.5V (D, CP) V _{IN} = 0.5V (\overline{C}_D , \overline{S}_D) |
| | | | | -1.8 | | | |
| I _{OS} | Output Short-Circuit Current | -60 | | -150 | mA | Max | V _{OUT} = 0V |
| I _{CC} | Power Supply Current | | 10.5 | 16.0 | mA | Max | |

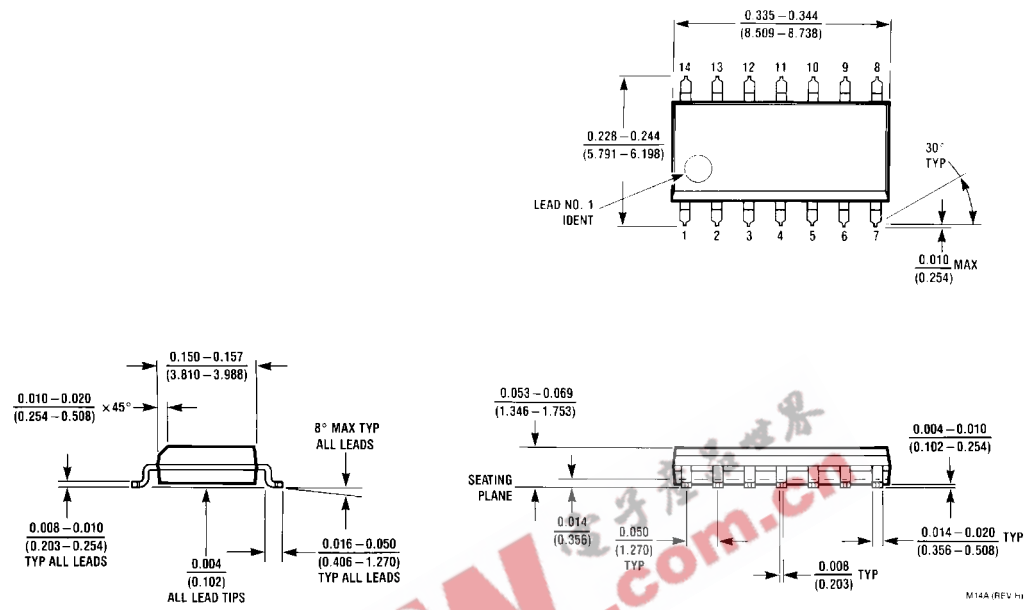
AC Electrical Characteristics

| Symbol | Parameter | T _A = +25°C V _{CC} = +5.0V C _L = 50 pF | | | T _A = 0°C to +70°C V _{CC} = +5.0V C _L = 50 pF | | Units |
|------------------|---|---|-----|-----|--|------|-------|
| | | Min | Typ | Max | Min | Max | |
| t _{MAX} | Maximum Clock Frequency | 100 | 125 | | 100 | | MHz |
| t _{PLH} | Propagation Delay | 3.8 | 5.3 | 6.8 | 3.8 | 7.8 | ns |
| t _{PHL} | CP _n to Q _n or \bar{Q}_n | 4.4 | 6.2 | 8.0 | 4.4 | 9.2 | |
| t _{PLH} | Propagation Delay | 3.2 | 4.6 | 6.1 | 3.2 | 7.1 | ns |
| t _{PHL} | \bar{C}_{Dn} or \bar{S}_{Dn} to Q _n or \bar{Q}_n | 3.5 | 7.0 | 9.0 | 3.5 | 10.5 | |

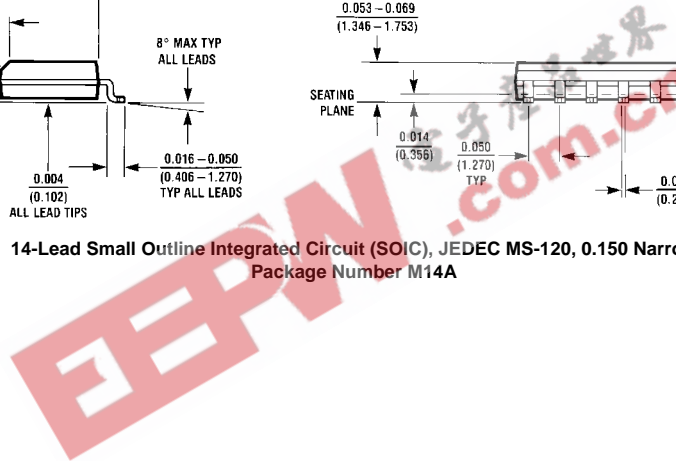
AC Operating Requirements

| Symbol | Parameter | T _A = +25°C V _{CC} = +5.0V | | T _A = 0°C to +70°C V _{CC} = +5.0V | | Units |
|--------------------|---|---|-----|--|-----|-------|
| | | Min | Max | Min | Max | |
| t _S (H) | Setup Time, HIGH or LOW | 2.0 | | 2.0 | | ns |
| t _S (L) | D _n to CP _n | 3.0 | | 3.0 | | |
| t _H (H) | Hold Time, HIGH or LOW | 1.0 | | 1.0 | | ns |
| t _H (L) | D _n to CP _n | 1.0 | | 1.0 | | |
| t _W (H) | CP _n Pulse Width | 4.0 | | 4.0 | | ns |
| t _W (L) | HIGH or LOW | 5.0 | | 5.0 | | |
| t _W (L) | \bar{C}_{Dn} or \bar{S}_{Dn} Pulse Width LOW | 4.0 | | 4.0 | | ns |
| t _{REC} | Recovery Time \bar{C}_{Dn} or \bar{S}_{Dn} to CP | 2.0 | | 2.0 | | ns |

Physical Dimensions inches (millimeters) unless otherwise noted



**14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150 Narrow
Package Number M14A**



Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

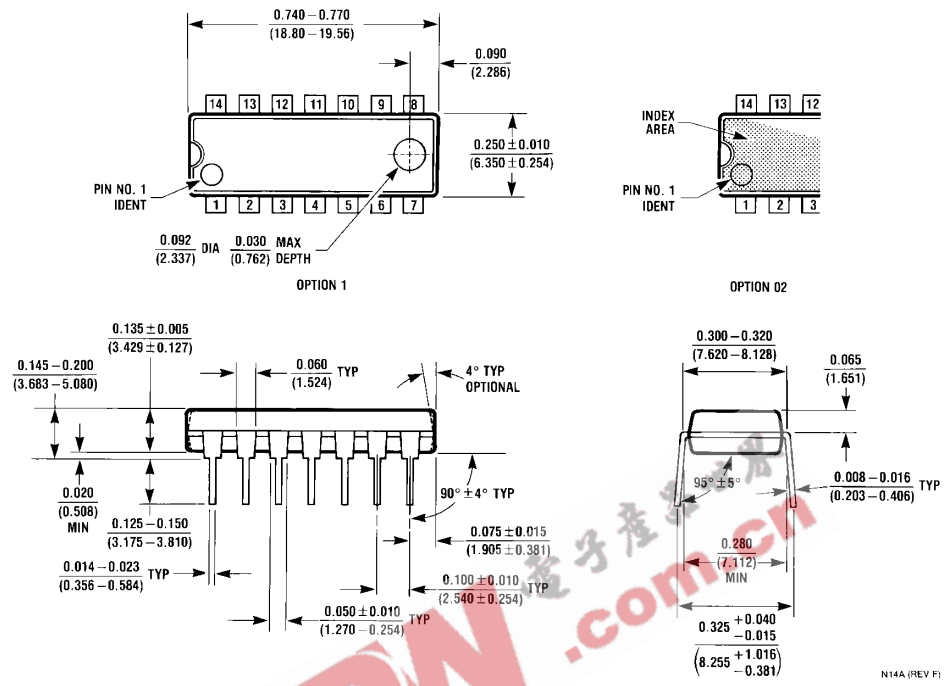


- NOTES:
 A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.
 B. DIMENSIONS ARE IN MILLIMETERS.
 C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

M14DRevB1

**14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
 Package Number M14D**

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide Package Number N14A

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