



SCCS067 - July 1994 - Revised March 2000

CY74FCT16841T CY74FCT162841T

20-Bit Latches

Features

- FCT-C speed at 5.5 ns (FCT16841T Com'l)
- Power-off disable outputs permits live insertion
- Edge-rate control circuitry for significantly improved noise characteristics
- Typical output skew < 250 ps
- ESD > 2000V
- TSSOP (19.6-mil pitch) and SSOP (25-mil pitch) packages
- Industrial temperature range of -40°C to +85°C
- V_{CC} = 5V ± 10%

CY74FCT16841T Features:

- 64 mA sink current, 32 mA source current
- Typical V_{OLP} (ground bounce) < 1.0V at V_{CC} = 5V, T_A = 25°C

CY74FCT162841T Features:

- Balanced 24 mA output drivers
- Reduced system switching noise
- Typical V_{OLP} (ground bounce) < 0.6V at V_{CC} = 5V, T_A = 25°C

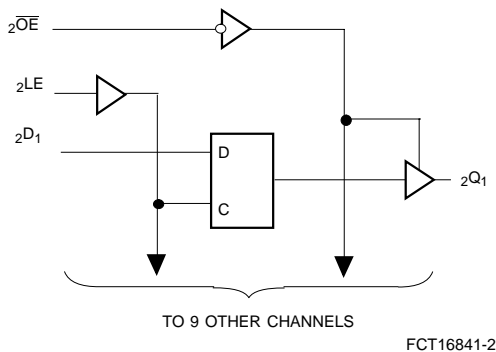
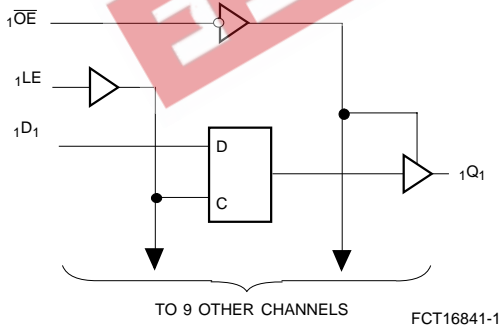
Functional Description

The CY74FCT16841T and CY74FCT162841T are 20-bit D-type latches designed for use in bus applications requiring high speed and low power. These devices can be used as two independent 10-bit latches, or as a single 20-bit latch, or as a single 10-bit latch, or as a single 20-bit latch by connecting the Output Enable (\overline{OE}) and Latch (LE) inputs. Flow-through pinout and small shrink packaging aid in simplifying board layout. The output buffers are designed with a power-off disable feature to allow live insertion of boards.

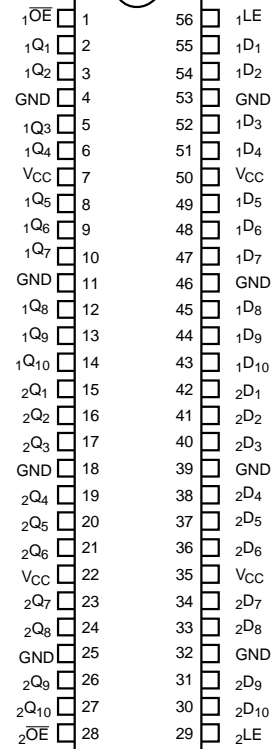
The CY74FCT16841T is ideally suited for driving high-capacitance loads and low-impedance backplanes.

The CY74FCT162841T has 24-mA balanced output drivers with current limiting resistors in the outputs. This reduces the need for external terminating resistors and provides for minimal undershoot and reduced ground bounce. The CY74FCT162841T is ideal for driving transmission lines.

Logic Block Diagrams



Pin Configuration SSOP/TSSOP Top View



Pin Description

Name	Description
D	Data Inputs
LE	Latch Enable Input (Active HIGH)
\overline{OE}	Output Enable Input (Active LOW)
O	Three-State Outputs

Function Table^[1]

Inputs			Outputs
D	LE	\overline{OE}	Q
H	H	L	H
L	H	L	L
X	L	L	Q ^[2]
X	X	H	Z

Maximum Ratings^[3, 4]

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	-55°C to +125°C
Ambient Temperature with Power Applied	-55°C to +125°C
DC Input Voltage	-0.5V to +7.0V
DC Output Voltage	-0.5V to +7.0V
DC Output Current (Maximum Sink Current/Pin)	-60 to +120 mA

Power Dissipation	1.0W
Static Discharge Voltage.....	>2001V (per MIL-STD-883, Method 3015)

Operating Range

Range	Ambient Temperature	V _{CC}
Industrial	-40°C to +85°C	5V ± 10%

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	Min.	Typ. ^[5]	Max.	Unit
V _{IH}	Input HIGH Voltage	Logic HIGH Level	2.0			V
V _{IL}	Input LOW Voltage	Logic LOW Level			0.8	V
V _H	Input Hysteresis ^[6]			100		mV
V _{IK}	Input Clamp Diode Voltage	V _{CC} =Min., I _{IN} =-18 mA		-0.7	-1.2	V
I _{IH}	Input HIGH Current	V _{CC} =Max., V _I =V _{CC}			±1	µA
I _{IL}	Input LOW Current	V _{CC} =Max., V _I =GND			±1	µA
I _{OZH}	High Impedance Output Current (Three-State Output pins)	V _{CC} =Max., V _{OUT} =2.7V			±1	µA
I _{OZL}	High Impedance Output Current (Three-State Output pins)	V _{CC} =Max., V _{OUT} =0.5V			±1	µA
I _{OS}	Short Circuit Current ^[7]	V _{CC} =Max., V _{OUT} =GND	-80	-140	-200	mA
I _O	Output Drive Current ^[7]	V _{CC} =Max., V _{OUT} =2.5V	-50		-180	mA
I _{OFF}	Power-Off Disable	V _{CC} =0V, V _{OUT} ≤4.5V ^[8]			±1	µA

Notes:

1. H = HIGH Voltage Level. L = LOW Voltage Level. X = Don't Care. Z = HIGH Impedance.
2. Output level before LE HIGH-to-LOW Transition.
3. Operation beyond the limits set forth may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.
4. Unused inputs must always be connected to an appropriate logic voltage level, preferably either V_{CC} or ground.
5. Typical values are at V_{CC}= 5.0V, T_A= +25°C ambient.
6. This parameter is specified but not tested.
7. Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parametric tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
8. Tested at +25°C.

Output Drive Characteristics for CY74FCT16841T

Parameter	Description	Test Conditions	Min.	Typ. ^[5]	Max.	Unit
V _{OH}	Output HIGH Voltage	V _{CC} =Min., I _{OH} =-3 mA	2.5	3.5		V
		V _{CC} =Min., I _{OH} =-15 mA	2.4	3.5		
		V _{CC} =Min., I _{OH} =-32 mA	2.0	3.0		
V _{OL}	Output LOW Voltage	V _{CC} =Min., I _{OL} =64 mA		0.2	0.55	V

Output Drive Characteristics for CY74FCT162841T

Parameter	Description	Test Conditions	Min.	Typ. ^[5]	Max.	Unit
I _{ODL}	Output LOW Current ^[7]	V _{CC} =5V, V _{IN} =V _{IH} or V _{IL} , V _{OUT} =1.5V	60	115	150	mA
I _{ODH}	Output HIGH Current ^[7]	V _{CC} =5V, V _{IN} =V _{IH} or V _{IL} , V _{OUT} =1.5V	-60	-115	-150	mA
V _{OH}	Output HIGH Voltage	V _{CC} =Min., I _{OH} =-24 mA	2.4	3.3		V
V _{OL}	Output LOW Voltage	V _{CC} =Min., I _{OL} =24 mA		0.3	0.55	V

Capacitance^[6] (T_A = +25°C, f = 1.0 MHz)

Symbol	Description	Conditions	Typ. ^[5]	Max.	Unit
C _{IN}	Input Capacitance	V _{IN} = 0V	4.5	6.0	pF
C _{OUT}	Output Capacitance	V _{OUT} = 0V	5.5	8.0	pF

Power Supply Characteristics

Parameter	Description	Test Conditions	Min.	Typ. ^[5]	Max.	Unit	
I _{CC}	Quiescent Power Supply Current	V _{CC} =Max., V _{IN} ≤0.2V V _{IN} ≥V _{CC} -0.2V	—	5	500	μA	
ΔI _{CC}	Quiescent Power Supply Current (TTL inputs HIGH)	V _{CC} =Max., V _{IN} =3.4V ^[9]	—	0.5	1.5	mA	
I _{CCD}	Dynamic Power Supply Current ^[10]	V _{CC} =Max., One Input Toggling, 50% Duty Cycle, Outputs Open, OE=GND	—	60	100	μA/MHz	
I _C	Total Power Supply Current ^[11]	V _{CC} =Max., f ₁ =10 MHz, 50% Duty Cycle, Outputs Open, One Bit Toggling, OE=GND LE = V _{CC}	V _{IN} =V _{CC} or V _{IN} =GND	—	0.6	1.5	mA
			V _{IN} =3.4V or V _{IN} =GND	—	0.9	2.3	
		V _{CC} =Max., f ₁ =2.5 MHz, 50% Duty Cycle, Outputs Open, Twenty Bits Toggling, OE=GND	V _{IN} =V _{CC} or V _{IN} =GND	—	3.0	5.5 ^[12]	
			V _{IN} =3.4V or V _{IN} =GND	—	8.0	20.5 ^[12]	

Notes:

9. Per TTL driven input (V_{IN}=3.4V); all other inputs at V_{CC} or GND.
10. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
11. I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}
I_C = I_{CC} + ΔI_{CC}D_HN_T + I_{CCD}(f₀/2 + f₁N₁)
I_{CC} = Quiescent Current with CMOS input levels
ΔI_{CC} = Power Supply Current for a TTL HIGH input (V_{IN}=3.4V)
D_H = Duty Cycle for TTL inputs HIGH
N_T = Number of TTL inputs at D_H
I_{CCD} = Dynamic Current caused by an input transition pair (HLH or LHL)
f₀ = Clock frequency for registered devices, otherwise zero
f₁ = Input signal frequency
N₁ = Number of inputs changing at f₁
All currents are in milliamps and all frequencies are in megahertz.
12. Values for these conditions are examples of the I_{CC} formula. These limits are specified but not tested.

Switching Characteristics Over the Operating Range^[13]

Parameter	Description	Condition ^[14]	74FCT16841AT		74FCT16841CT 74FCT162841CT		Unit	Fig. No. ^[15]
			Min.	Max.	Min.	Max.		
t _{PLH} t _{PHL}	Propagation Delay D to Q (LE=HIGH)	C _L =50 pF R _L =500Ω	1.5	9.0	1.5	5.5	ns	1, 5
		C _L =300 pF ^[16] R _L =500Ω	1.5	13.0	1.5	13.0		
t _{PLH} t _{PHL}	Propagation Delay LE to Q	C _L =50 pF R _L =500Ω	1.5	12.0	1.5	6.4	ns	1, 5
		C _L =300 pF ^[16] R _L =500Ω	1.5	16.0	1.5	15.0		
t _{PHZ} t _{PZL}	Output Enable Time OE to Q	C _L =50 pF R _L =500Ω	1.5	11.5	1.5	6.5	ns	1, 7, 8
		C _L =300 pF ^[16] R _L =500Ω	1.5	23.0	1.5	12.0		
t _{PHZ} t _{PLZ}	Output Disable Time OE to Q	C _L =5 pF ^[16] R _L =500Ω	1.5	7.0	1.5	5.7	ns	1, 7, 8
		C _L =50 pF R _L =500Ω	1.5	8.0	1.5	6.0		
t _{SU}	Set-Up Time HIGH or LOW, D to LE	C _L =50 pF R _L =500Ω	2.5	—	2.0	—	ns	9
t _H	Hold Time HIGH or LOW, D to LE		2.5	—	1.5	—	ns	9
t _W	LE Pulse Width HIGH		4.0 ^[17]	—	4.0 ^[17]	—	ns	5
t _{SK(O)}	Output Skew ^[18]		—	0.5	—	0.5	ns	—

Notes:

13. Minimum limits are specified but not tested on Propagation Delays.
14. See test circuit and waveform.
15. See "Parameter Measurement Information" in the General Information section.
16. These conditions are specified but not tested.
17. These limits are specified but not tested.
18. Skew between any two outputs of the same package switching in the same direction. This parameter is ensured by design.

Ordering Information for CY74FCT16841T

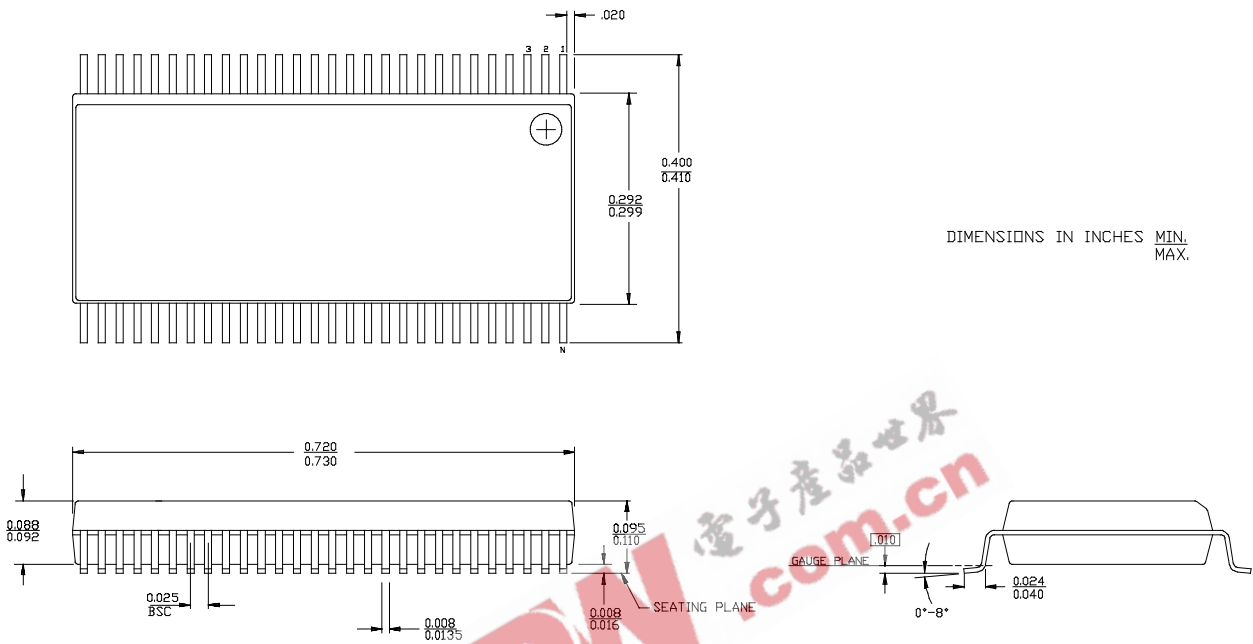
Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
5.5	CY74FCT16841CTPVC/PVCT	O56	56-Lead (300-Mil) SSOP	Industrial
6.5	CY74FCT16841ATPVC/PVCT	O56	56-Lead (300-Mil) SSOP	

Ordering Information CY74FCT162841T

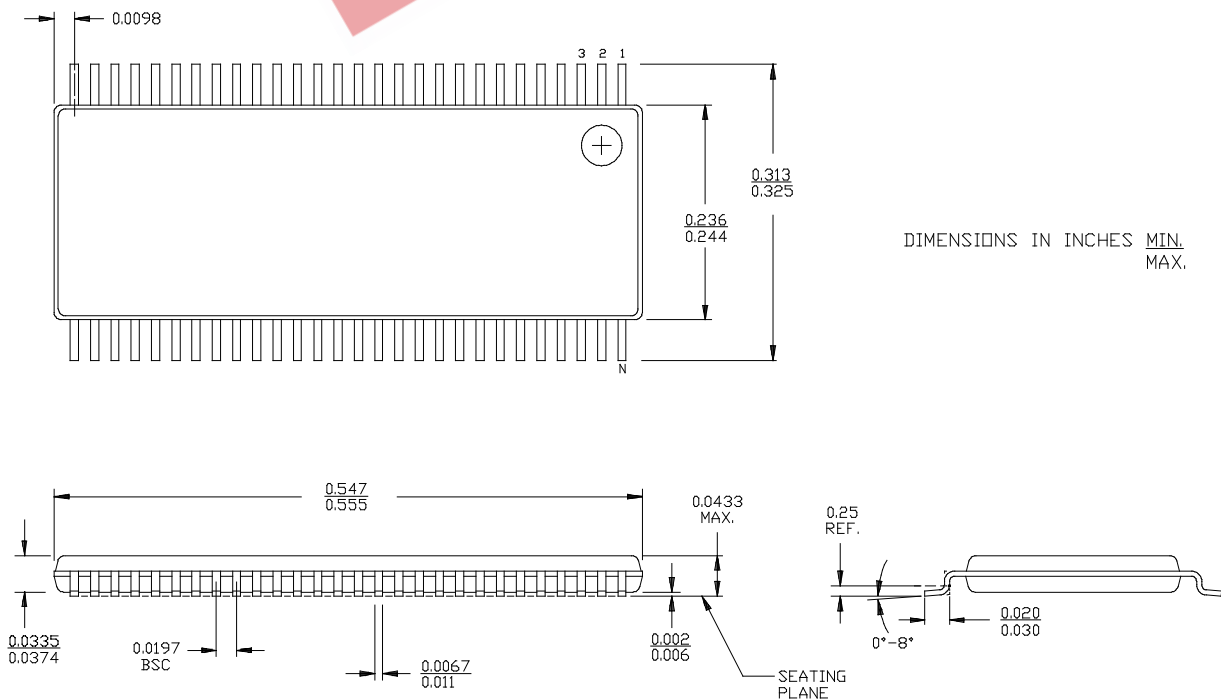
Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
5.5	74FCT162841CTPACT	Z56	56-Lead (240-Mil) TSSOP	Industrial
	CY74FCT162841CTPVC	O56	56-Lead (300-Mil) SSOP	
	74FCT162841CTPVCT	O56	56-Lead (300-Mil) SSOP	

Package Diagrams

56-Lead Shrunk Small Outline Package O56



56-Lead Thin Shrunk Small Outline Package Z56



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