

# 74FST3383

## 10-Bit Low Power Bus Exchange

The ON Semiconductor 74FST3383 is a 10-bit low power bus exchange. The device is CMOS TTL compatible when operating between 4 and 5.5 Volts. The device exhibits extremely low  $R_{ON}$  and adds nearly zero propagation delay. The device adds no noise or ground bounce to the system.

### Features

- $R_{ON} < 4 \Omega$  Typical
- Less Than 0.25 ns–Max Delay Through Switch
- Nearly Zero Standby Current
- No Circuit Bounce
- Control Inputs are TTL/CMOS Compatible
- Pin-For-Pin Compatible With QS3383, FST3383, CBT3383
- All Popular Packages: SOIC–24, TSSOP–24, QSOP–24
- All Devices in Package TSSOP are Inherently Pb-Free\*

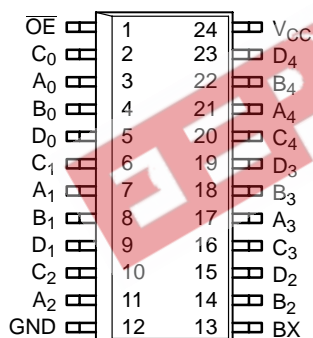


Figure 1. 24-Lead Pinout

### TRUTH TABLE

OE	BX	A <sub>0</sub> –A <sub>4</sub>	B <sub>0</sub> –B <sub>4</sub>	Function
H	X	HIGH–Z State	HIGH–Z State	Disconnect
L	L	C <sub>0</sub> –C <sub>4</sub>	D <sub>0</sub> –D <sub>4</sub>	Connect
L	H	D <sub>0</sub> –D <sub>4</sub>	C <sub>0</sub> –C <sub>4</sub>	Exchange

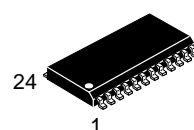
NOTE: H = HIGH Voltage Level, L = LOW Voltage Level, X = Don't Care



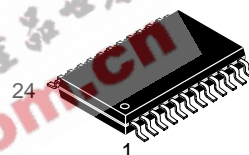
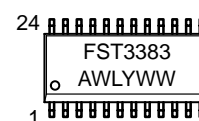
ON Semiconductor®

<http://onsemi.com>

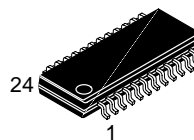
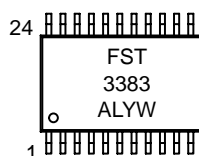
### MARKING DIAGRAMS



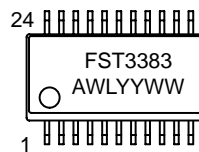
SOIC–24  
DW SUFFIX  
CASE 751E



TSSOP–24  
DT SUFFIX  
CASE 948H



QSOP–24  
QS SUFFIX  
CASE 492B



A = Assembly Location  
L, WL = Wafer Lot  
Y, YY = Year  
W, WW = Work Week

### PIN NAMES

Pin	Description
OE	Bus Switch Enable
BX	Bus Exchange
A <sub>0</sub> –A <sub>4</sub> , B <sub>0</sub> –B <sub>4</sub>	Buses A, B
C <sub>0</sub> –C <sub>4</sub> , D <sub>0</sub> –D <sub>4</sub>	Buses C, D

### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

## 74FST3383

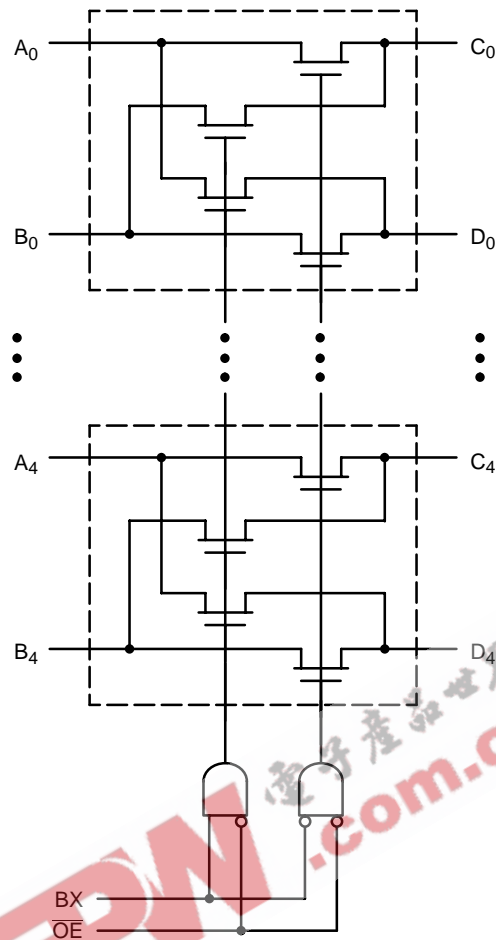


Figure 2. Logic Diagram

### ORDERING INFORMATION

Device Order Number	Package	Shipping†
74FST3383DW	SOIC-24	48 Units / Rail
74FST3383DWR2	SOIC-24	2500 Units / Tape & Reel
74FST3383DT	TSSOP-24* (Pb-Free)	96 Units / Rail
74FST3383DTR2	TSSOP-24* (Pb-Free)	2500 Units / Tape & Reel
74FST3383QS	QSOP-24	96 Units / Rail
74FST3383QSR	QSOP-24	2500 Units / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

\*This package is inherently Pb-Free.

## 74FST3383

### MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
$V_{CC}$	DC Supply Voltage	-0.5 to +7.0	V
$V_I$	DC Input Voltage	-0.5 to +7.0	V
$V_O$	DC Output Voltage	-0.5 to +7.0	V
$I_{IK}$	DC Input Diode Current $V_I < \text{GND}$	-50	mA
$I_{OK}$	DC Output Diode Current $V_O < \text{GND}$	-50	mA
$I_O$	DC Output Sink Current	128	mA
$I_{CC}$	DC Supply Current per Supply Pin	$\pm 100$	mA
$I_{GND}$	DC Ground Current per Ground Pin	$\pm 100$	mA
$T_{STG}$	Storage Temperature Range	-65 to +150	$^{\circ}\text{C}$
$T_L$	Lead Temperature, 1 mm from Case for 10 Seconds	260	$^{\circ}\text{C}$
$T_J$	Junction Temperature Under Bias	+150	$^{\circ}\text{C}$
$\theta_{JA}$	Thermal Resistance SOIC TSSOP QSOP	125 170 200	$^{\circ}\text{C}/\text{W}$
MSL	Moisture Sensitivity	Level 1	
$F_R$	Flammability Rating Oxygen Index: 28 to 34	UL 94 V-0 @ 0.125 in	
$V_{ESD}$	ESD Withstand Voltage Human Body Model (Note 1) Machine Model (Note 2) Charged Device Model (Note 3)	> 2000 > 200 N/A	V
$I_{Latchup}$	Latchup Performance Above $V_{CC}$ and Below GND at 85 $^{\circ}\text{C}$ (Note 4)	$\pm 500$	mA

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

1. Tested to EIA/JESD22-A114-A.
2. Tested to EIA/JESD22-A115-A.
3. Tested to JESD22-C101-A.
4. Tested to EIA/JESD78.

### RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
$V_{CC}$	Supply Voltage Operating, Data Retention Only	4.0	5.5	V
$V_I$	Input Voltage (Note 5)	0	5.5	V
$V_O$	Output Voltage (HIGH or LOW State)	0	5.5	V
$T_A$	Operating Free-Air Temperature	-40	+85	$^{\circ}\text{C}$
$\Delta t/\Delta V$	Input Transition Rise or Fall Rate Switch I/O Switch Control Input $V_{CC} = 5.0 \text{ V} \pm 0.5 \text{ V}$	0	DC 5	ns/V

5. Unused control inputs may not be left open. All control inputs must be tied to a high or low logic input voltage level.

# 74FST3383

## DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Conditions	V <sub>CC</sub> (V)	T <sub>A</sub> = -40°C to +85°C			Unit
				Min	Typ*	Max	
V <sub>IK</sub>	Clamp Diode Resistance	I <sub>IN</sub> = -18mA	4.5			-1.2	V
V <sub>IH</sub>	High-Level Input Voltage		4.0 to 5.5	2.0			V
V <sub>IL</sub>	Low-Level Input Voltage		4.0 to 5.5			0.8	V
I <sub>I</sub>	Input Leakage Current	0 ≤ V <sub>IN</sub> ≤ 5.5 V	5.5			±1.0	μA
I <sub>OZ</sub>	OFF-STATE Leakage Current	0 ≤ A, B ≤ V <sub>CC</sub>	5.5			±1.0	μA
R <sub>ON</sub>	Switch On Resistance (Note 6)	V <sub>IN</sub> = 0 V, I <sub>IN</sub> = 64 mA	4.5		4	7	Ω
		V <sub>IN</sub> = 0 V, I <sub>IN</sub> = 30 mA	4.5		4	7	
		V <sub>IN</sub> = 2.4 V, I <sub>IN</sub> = 15 mA	4.5		8	15	
		V <sub>IN</sub> = 2.4 V, I <sub>IN</sub> = 15 mA	4.0		11	20	
I <sub>CC</sub>	Quiescent Supply Current	V <sub>IN</sub> = V <sub>CC</sub> or GND, I <sub>OUT</sub> = 0	5.5			3	μA
ΔI <sub>CC</sub>	Increase In I <sub>CC</sub> per Input	One input at 3.4 V, Other inputs at V <sub>CC</sub> or GND	5.5			2.5	mA

\*Typical values are at V<sub>CC</sub> = 5.0 V and T<sub>A</sub> = 25°C.

6. Measured by the voltage drop between A and B pins at the indicated current through the switch. On resistance is determined by the lower of the voltages on the two (A or B) pins.

## AC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Conditions	T <sub>A</sub> = -40°C to +85°C C <sub>L</sub> = 50 pF, R <sub>U</sub> = R <sub>D</sub> = 500 Ω				Unit
			V <sub>CC</sub> = 4.5-5.5 V		V <sub>CC</sub> = 4.0 V		
			Min	Max	Min	Max	
t <sub>PHL</sub> , t <sub>PLH</sub>	Prop Delay Bus to Bus (Note 7)	V <sub>I</sub> = OPEN		0.25		0.25	ns
	Prop Delay, BX to An, Bn, Cn or Dn		1.0	5.8		6.5	
t <sub>PZH</sub> , t <sub>PZL</sub>	Output Enable Time, BX to An, Bn, Cn or Dn	V <sub>I</sub> = 7 V for t <sub>PZL</sub>	1.0	5.8		6.5	ns
	Output Enable Time, I <sub>OE</sub> to An, Bn, Cn or Dn	V <sub>I</sub> = OPEN for t <sub>PZH</sub>	1.0	5.8		6.5	
t <sub>PHZ</sub> , t <sub>PLZ</sub>	Output Disable Time, BX to An, Bn, Cn or Dn	V <sub>I</sub> = 7 V for t <sub>PLZ</sub>	1.0	5.3		6.2	ns
	Output Disable Time, I <sub>OE</sub> to An, Bn, Cn or Dn	V <sub>I</sub> = OPEN for t <sub>PHZ</sub>	1.0	5.3		6.2	

7. This parameter is guaranteed by design but is not tested. The bus switch contributes no propagation delay other than the RC delay of the typical On resistance of the switch and the 50 pF load capacitance, when driven by an ideal voltage source (zero output impedance).

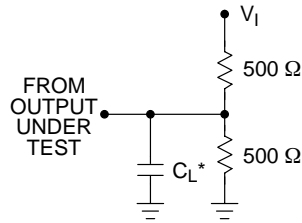
## CAPACITANCE (Note 8)

Symbol	Parameter	Conditions	Typ	Max	Unit
C <sub>IN</sub>	Control Pin Input Capacitance	V <sub>CC</sub> = 5.0 V	6		pF
C <sub>I/O</sub>	Port Input/Output Capacitance	V <sub>CC</sub> , $\overline{OE}$ = 5.0 V	13		pF

8. T<sub>A</sub> = +25°C, f = 1 MHz, Capacitance is characterized but not tested.

# 74FST3383

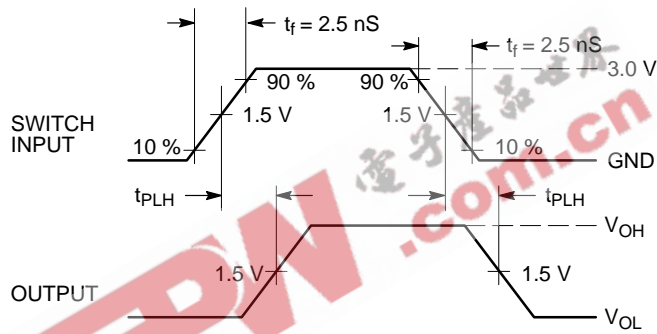
## AC Loading and Waveforms



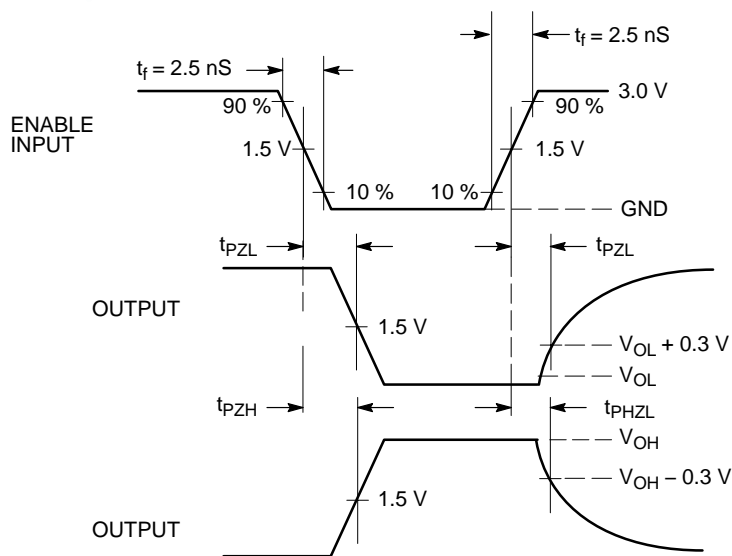
**NOTES:**

1. Input driven by 50  $\Omega$  source terminated in 50  $\Omega$ .
  2.  $C_L$  includes load and stray capacitance.
- \* $C_L = 50$  pF

**Figure 3. AC Test Circuit**



**Figure 4. Propagation Delays**

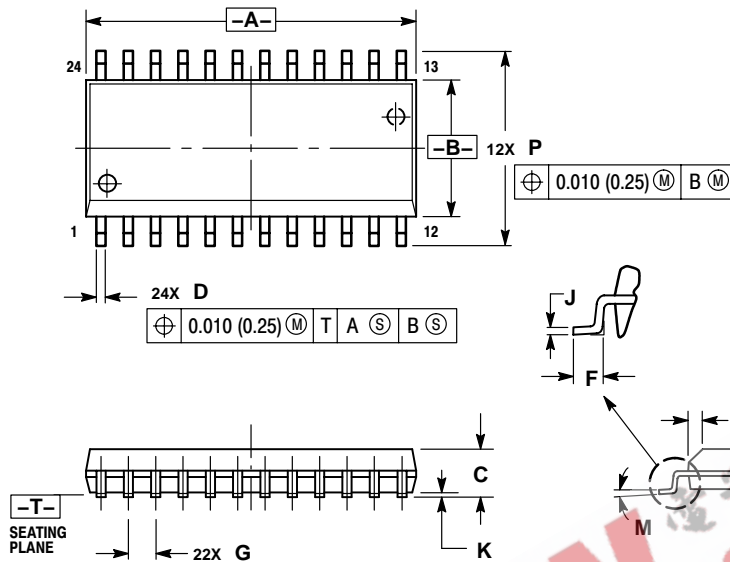


**Figure 5. Enable/Disable Delays**

# 74FST3383

## PACKAGE DIMENSIONS

SOIC-24  
D SUFFIX  
CASE 751E-04  
ISSUE E



### NOTES:

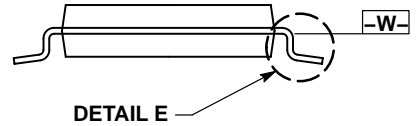
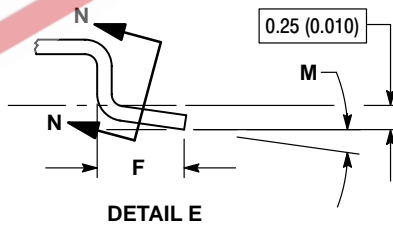
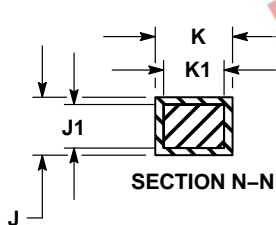
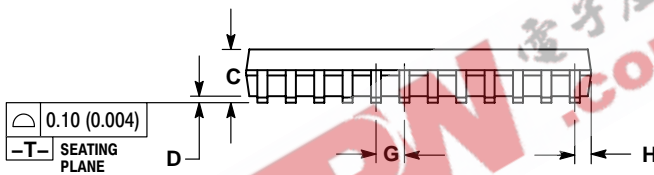
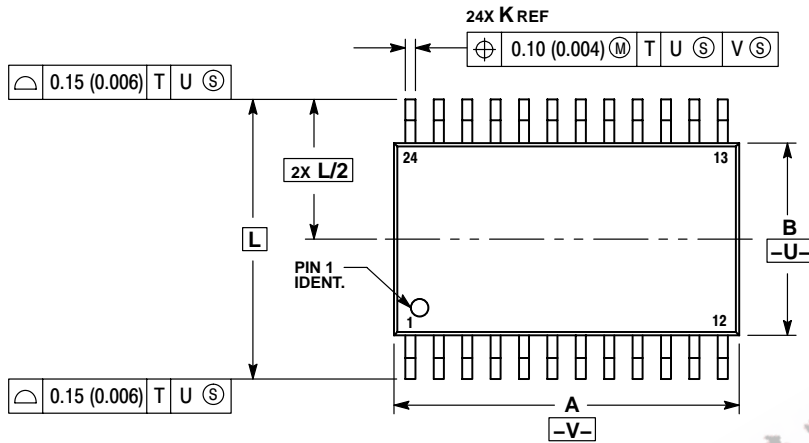
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN EXCESS OF D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	15.25	15.54	0.601	0.612
B	7.40	7.60	0.292	0.299
C	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.41	0.90	0.016	0.035
G	1.27 BSC		0.050 BSC	
J	0.23	0.32	0.009	0.013
K	0.13	0.29	0.005	0.011
M	0°	8°	0°	8°
P	10.05	10.55	0.395	0.415
R	0.25	0.75	0.010	0.029

# 74FST3383

## PACKAGE DIMENSIONS

TSSOP-24  
DT SUFFIX  
CASE 948H-01  
ISSUE A



### NOTES:

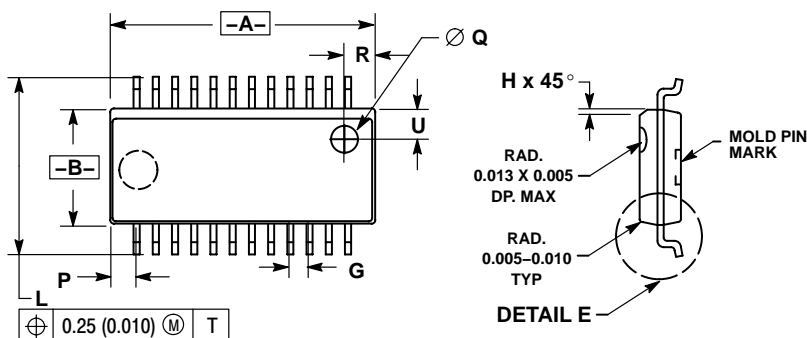
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	7.70	7.90	0.303	0.311
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.27	0.37	0.011	0.015
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

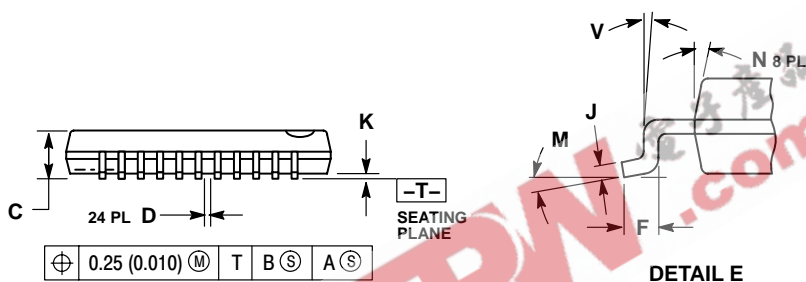
# 74FST3383

## PACKAGE DIMENSIONS

QSOP-24  
QS SUFFIX  
CASE 492B-01  
ISSUE O



⊕	0.25 (0.010)	Ⓜ	T
---	--------------	---	---



⊕	0.25 (0.010)	Ⓜ	T	B Ⓢ	A Ⓢ
---	--------------	---	---	-----	-----

### NOTES:

- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
- CONTROLLING DIMENSION: INCH.
- THE BOTTOM PACKAGE SHALL BE BIGGER THAN THE TOP PACKAGE BY 4 MILS (NOTE: LEAD SIDE ONLY). BOTTOM PACKAGE DIMENSION SHALL FOLLOW THE DIMENSION STATED IN THIS DRAWING.
- PLASTIC DIMENSIONS DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 6 MILS PER SIDE.
- BOTTOM EJECTOR PIN WILL INCLUDE THE COUNTRY OF ORIGIN (COO) AND MOLD CAVITY I.D.

DIM	INCHES		MILLIMETERS	
	MAX	MIN	MAX	MIN
A	0.337	0.344	8.56	8.74
B	0.150	0.157	3.81	3.99
C	0.061	0.068	1.55	1.73
D	0.008	0.012	0.20	0.31
F	0.016	0.035	0.41	0.89
G	0.025 BSC		0.64 BSC	
H	0.008	0.018	0.20	0.46
J	0.0098	0.0075	0.249	0.191
K	0.004	0.010	0.10	0.25
L	0.230	0.244	5.84	6.20
M	0°	8°	0°	8°
N	0°	7°	0°	7°
P	0.027	0.037	0.69	0.94
Q	0.035 DIA		0.89 DIA	
R	0.035	0.045	0.89	1.14
U	0.035	0.045	0.89	1.14
V	0°	8°	0°	8°

ON Semiconductor and are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

### PUBLICATION ORDERING INFORMATION

#### LITERATURE FULFILLMENT:

Literature Distribution Center for ON Semiconductor  
P.O. Box 61312, Phoenix, Arizona 85082-1312 USA  
Phone: 480-829-7710 or 800-344-3860 Toll Free USA/Canada  
Fax: 480-829-7709 or 800-344-3867 Toll Free USA/Canada  
Email: orderlit@onsemi.com

N. American Technical Support: 800-282-9855 Toll Free  
USA/Canada

Japan: ON Semiconductor, Japan Customer Focus Center  
2-9-1 Kamimeguro, Meguro-ku, Tokyo, Japan 153-0051  
Phone: 81-3-5773-3850

ON Semiconductor Website: <http://onsemi.com>

Order Literature: <http://www.onsemi.com/litorder>

For additional information, please contact your local Sales Representative.