

DATA SHEET

For a complete data sheet, please also download:

- The IC06 74HC/HCT/HCU/HCMOS Logic Family Specifications
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Information
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Outlines

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74HC/HCT273

Octal D-type flip-flop with reset;
positive-edge trigger

Product specification
File under Integrated Circuits, IC06

September 1993

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FEATURES

- Ideal buffer for MOS microprocessor or memory
- Common clock and master reset
- Eight positive edge-triggered D-type flip-flops
- See "377" for clock enable version
- See "373" for transparent latch version
- See "374" for 3-state version
- Output capability; standard
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT273 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT273 have eight edge-triggered, D-type flip-flops with individual D inputs and Q outputs. The common clock (CP) and master reset ($\overline{\text{MR}}$) inputs load and reset (clear) all flip-flops simultaneously. The state of each D input, one set-up time before the LOW-to-HIGH clock transition, is transferred to the corresponding output (Q_n) of the flip-flop.

All outputs will be forced LOW independently of clock or data inputs by a LOW voltage level on the $\overline{\text{MR}}$ input.

The device is useful for applications where the true output only is required and the clock and master reset are common to all storage elements.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; t_r = t_f = 6 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t _{PHL} / t _{PLH}	propagation delay CP to Q _n $\overline{\text{MR}}$ to Q _n	C _L = 15 pF; V _{CC} = 5 V	15	15	ns
			15	20	ns
f _{max}	maximum clock frequency		66	36	MHz
C _I	input capacitance		3.5	3.5	pF
C _{PD}	power dissipation capacitance per flip-flop	notes 1 and 2	20	23	pF

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f_i = input frequency in MHz

f_o = output frequency in MHz

∑ (C_L × V_{CC}² × f_o) = sum of outputs

C_L = output load capacitance in pF

V_{CC} = supply voltage in V

2. For HC the condition is V_I = GND to V_{CC}
For HCT the condition is V_I = GND to V_{CC} – 1.5 V

ORDERING INFORMATION

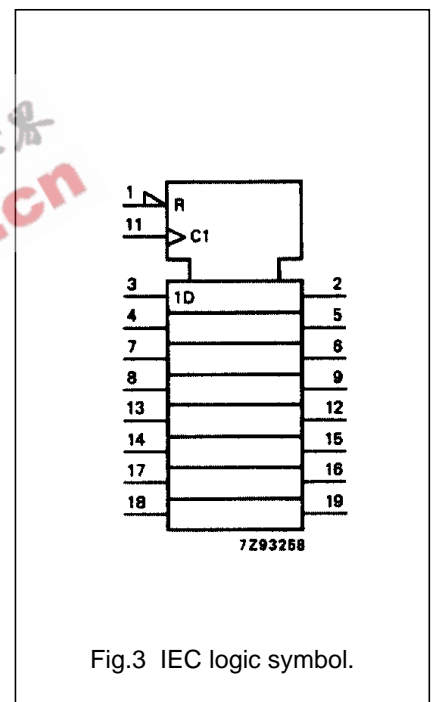
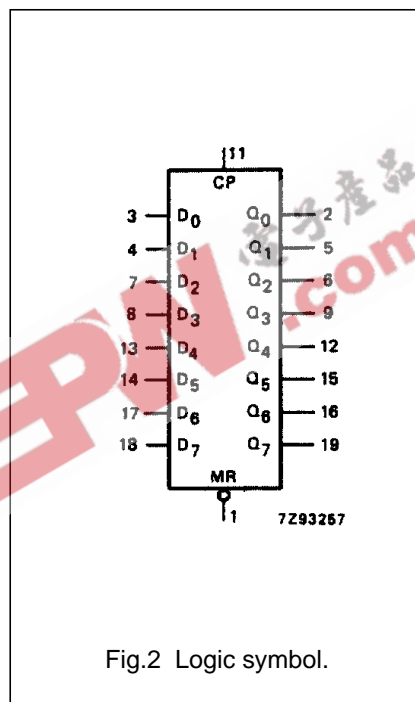
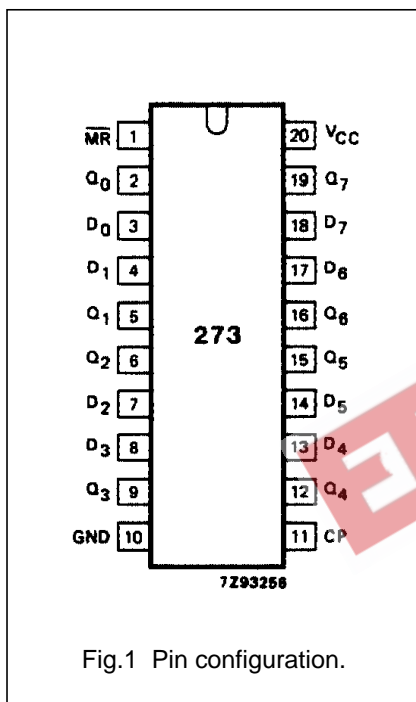
See "74HC/HCT/HCU/HCMOS Logic Package Information".

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PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	\overline{MR}	master reset input (active LOW)
2, 5, 6, 9, 12, 15, 16, 19	Q_0 to Q_7	flip-flop outputs
3, 4, 7, 8, 13, 14, 17, 18	D_0 to D_7	data inputs
10	GND	ground (0 V)
11	CP	clock input (LOW-to-HIGH, edge-triggered)
20	V_{CC}	positive supply voltage



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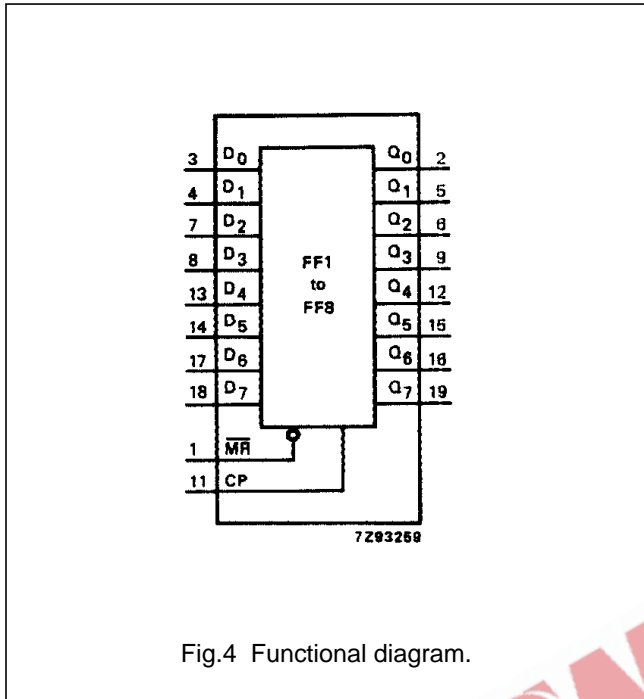


Fig.4 Functional diagram.

FUNCTION TABLE

OPERATING MODES	INPUTS			OUTPUTS
	\overline{MR}	CP	D_n	Q_n
reset (clear)	L	X	X	L
load "1"	H	↑	h	H
load "0"	H	↑	l	L

Note

- 1. H = HIGH voltage level
- h = HIGH voltage level one set-up time prior to the LOW-to-HIGH CP transition
- L = LOW voltage level
- l = LOW voltage level one set-up time prior to the LOW-to-HIGH CP transition
- ↑ = LOW-to-HIGH transition
- X = don't care

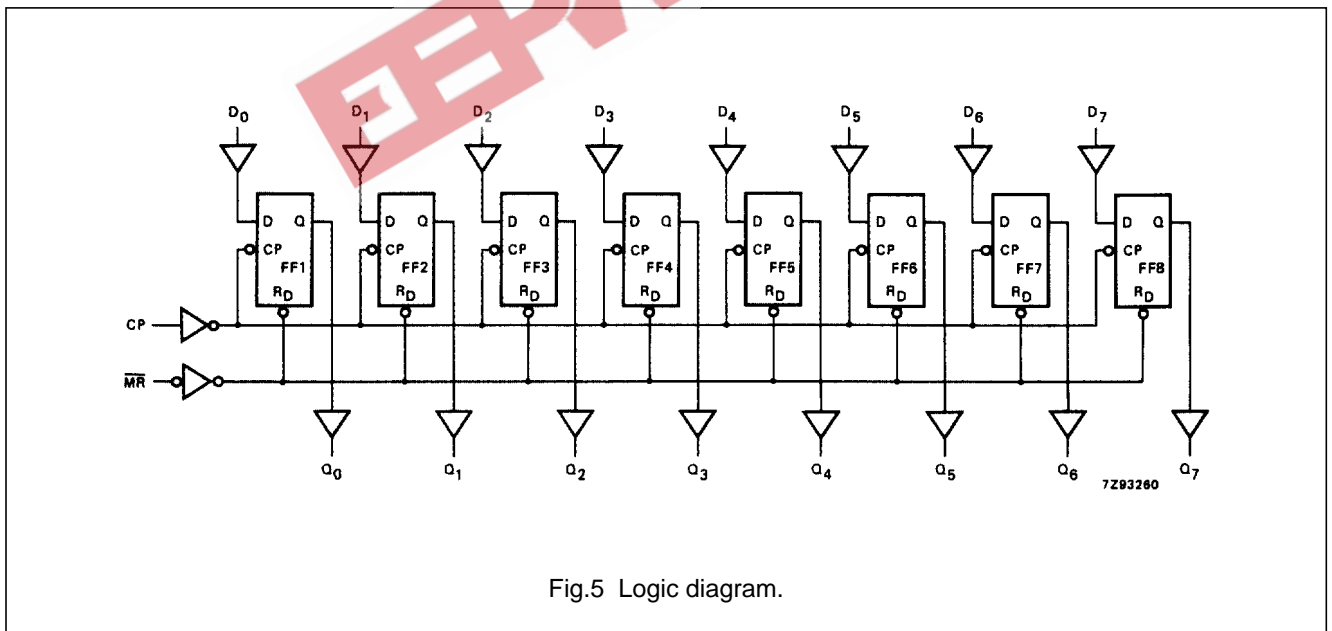


Fig.5 Logic diagram.

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DC CHARACTERISTICS FOR 74HC

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: standard

I_{CC} category: MSI

AC CHARACTERISTICS FOR 74HC

GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T _{amb} (°C)						UNIT	TEST CONDITIONS		
		74HC							V _{CC} (V)	WAVEFORMS	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
t _{PHL} / t _{PLH}	propagation delay CP to Q _n		41 15 13	150 30 26		185 37 31	225 45 38	ns	2.0 4.5 6.0	Fig.6	
t _{PHL}	propagation delay MR to Q _n		44 16 14	150 30 26		185 37 31	225 45 38	ns	2.0 4.5 6.0	Fig.7	
t _{THL} / t _{TLH}	output transition time		19 7 6	75 15 13		95 19 15	110 22 19	ns	2.0 4.5 6.0	Fig.6	
t _w	clock pulse width HIGH or LOW	80 16 14	14 5 4		100 20 17		120 24 20	ns	2.0 4.5 6.0	Fig.6	
t _w	master reset pulse width LOW	60 12 10	17 6 5		75 15 13		90 18 15	ns	2.0 4.5 6.0	Fig.7	
t _{rem}	removal time MR to CP	50 10 9	-6 -2 -2		65 13 11		75 15 13	ns	2.0 4.5 6.0	Fig.7	
t _{su}	set-up time D _n to CP	60 12 10	11 4 3		75 15 13		90 18 15	ns	2.0 4.5 6.0	Fig.8	
t _h	hold time D _n to CP	3 3 3	-6 -2 -2		3 3 3		3 3 3	ns	2.0 4.5 6.0	Fig.8	
f _{max}	maximum clock pulse frequency	6.0 30 35	20.6 103 122		4.8 24 28		4.0 20 24	MHz	2.0 4.5 6.0	Fig.6	

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DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: standard

I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
\overline{MR}	1.00
CP	1.75
D _n	0.15

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T _{amb} (°C)							UNIT	TEST CONDITIONS		
		74HCT								V _{CC} (V)	WAVEFORMS	
		+25			-40 to +85		-40 to +125					min.
min.	typ.	max.	min.	max.	min.	max.						
t _{PHL} / t _{PLH}	propagation delay CP to Q _n		16	30		38		45	ns	4.5	Fig.6	
t _{PHL}	propagation delay \overline{MR} to Q _n		23	34		43		51	ns	4.5	Fig.7	
t _{THL} / t _{TLH}	output transition time		7	15		19		22	ns	4.5	Fig.6	
t _W	clock pulse width HIGH or LOW	16	9		20		24		ns	4.5	Fig.6	
t _W	master reset pulse width LOW	16	8		20		24		ns	4.5	Fig.7	
t _{rem}	removal time \overline{MR} to CP	10	-2		13		15		ns	4.5	Fig.7	
t _{su}	set-up time D _n to CP	12	5		15		18		ns	4.5	Fig.8	
t _h	hold time D _n to CP	3	-4		3		3		ns	4.5	Fig.8	
f _{max}	maximum clock pulse frequency	30	56		24		20		MHz	4.5	Fig.6	

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AC WAVEFORMS

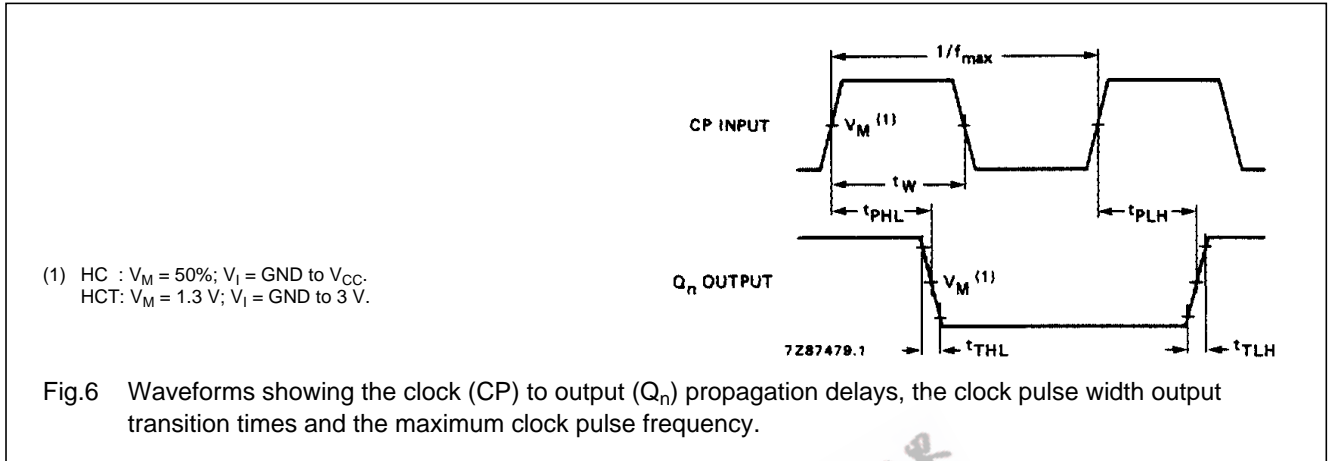


Fig.6 Waveforms showing the clock (CP) to output (Q_n) propagation delays, the clock pulse width output transition times and the maximum clock pulse frequency.

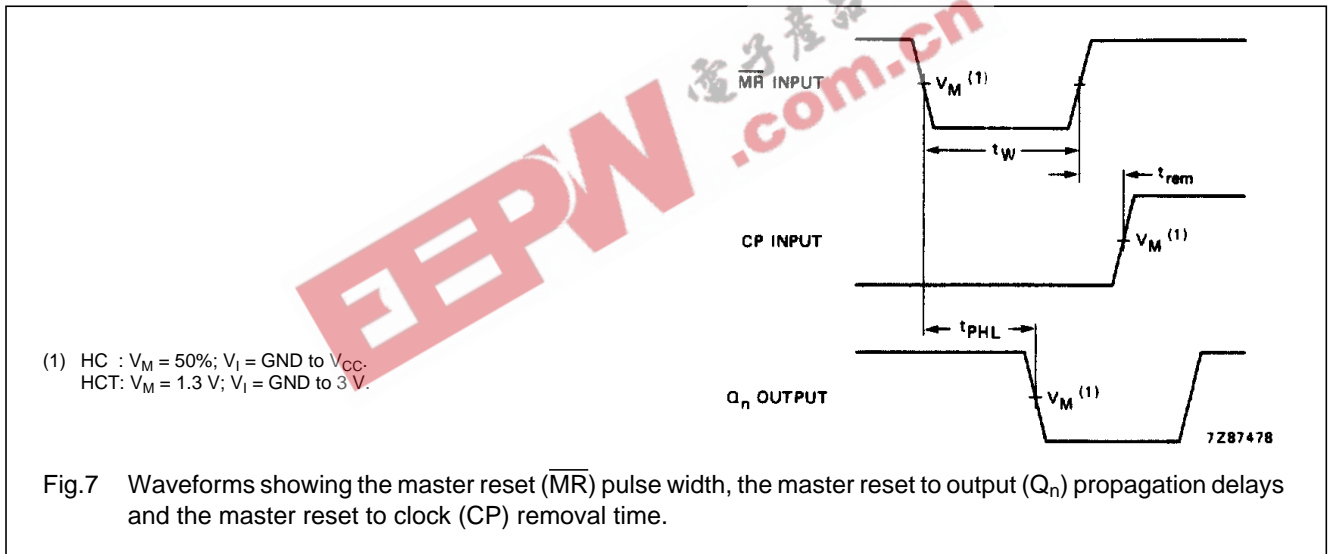


Fig.7 Waveforms showing the master reset ($\overline{\text{MR}}$) pulse width, the master reset to output (Q_n) propagation delays and the master reset to clock (CP) removal time.

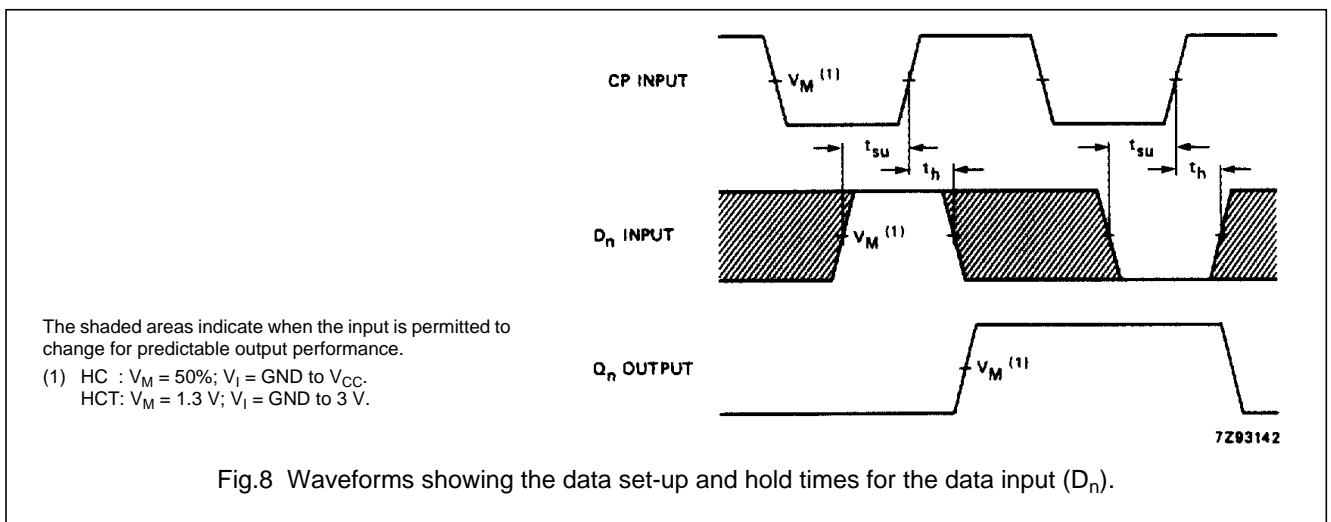


Fig.8 Waveforms showing the data set-up and hold times for the data input (D_n).

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PACKAGE OUTLINES

See *"74HC/HCT/HCU/HCMOS Logic Package Outlines"*.

