INTEGRATED CIRCUITS

DATA SHEET



74LV4316Quad bilateral switches

Product specification Supersedes data of 1994 Dec 01 IC24 Data Handbook





Quad bilateral switches

74LV4316

FEATURES

- Optimized for Low Voltage applications: 1.0V to 6.0V
- Accepts TTL input levels between V_{CC} = 2.7V and V_{CC} = 3.6V
- Low typ "ON" resistance: 80Ω at V_{CC} – VEE = 4.5V 120Ω at V_{CC} – VEE = 3.0V 295Ω at V_{CC} – VEE = 2.0V
- Logic level translation: to enable 3V logic to communicate with ±3V analog signals
- Typical "break before make" built in
- Output capability: non-standard
- I_{CC} category: MSI

DESCRIPTION

The 74LV4316 is a low-voltage CMOS device that is pin and function compatible with 74HC/HCT4316.

The 74LV4316 has four independent analog switches. Each switch has two input/output terminals (nY, nZ) and an active HIGH select input (nS). When the enable input (E) is HIGH, all four analog switches are turned off.

Current through a switch will not cause additional V_{CC} current provided the voltage at the terminals of the switch is maintained within the supply voltage range; $V_{CC} > (V_Y, V_Z) > V_{EE}$. Inputs nY and nZ are electrically equivalent terminals. V_{CC} and GND are the supply voltage pins for the digital control inputs (E and nS). The V_{CC} to GND ranges

The analog inputs/outputs (nY and nZ) can swing between V_{CC} as a positive limit and V_{EE} as a negative limit.

V_{CC} - V_{EE} may not exceed 6.0 V.

QUICK REFERENCE DATA

GND = 0 V; $T_{amb} = 25^{\circ}C$; $t_r = t_f \le 2.5 \text{ ns}$

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t _{PZH} /t _{PZL}	Turn "ON" time: E to V _{OS} nS to V _{OS}	C_L = 15pF R_L = 1K Ω V_{CC} = 3.3V	19	ns
t _{PHZ} /t _{PLZ}	Turn "OFF" time: E to V _{OS} nS to V _{OS}	Com.	20	ns
C _I	Input capacitance		3.5	pF
C _{PD}	Power dissipation capacitance per switch	Notes 1, 2	13	pF
Cs	Maximum switch capacitance		5	pF

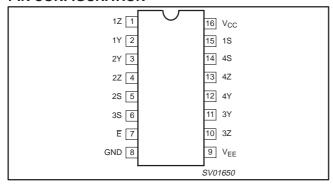
NOTES:

- 1. C_{PD} is used to determine the dynamic power dissipation (P_D in μ W) $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$ where: f_i = input frequency in MHz; C_L = output load capacity in pF; f_0 = output frequency in MHz; V_{CC} = supply voltage in V;
- V_{CC} = supply voltage in V: $\sum (C_L \times V_{CC}^2 \times f_0)$ = sum of the outputs.
- 2. The condition is $V_I = GND$ to V_{CC}

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	PKG. DWG. #
16-Pin Plastic DIL	-40°C to +125°C	74LV4316 N	74LV4316 N	SOT38-4
16-Pin Plastic SO	-40°C to +125°C	74LV4316 D	74LV4316 D	SOT109-1
16-Pin Plastic SSOP Type II	-40°C to +125°C	74LV4316 DB	74LV4316 DB	SOT338-1
16-Pin Plastic TSSOP Type I	-40°C to +125°C	74LV4316 PW	74LV4316PW DH	SOT403-1

PIN CONFIGURATION



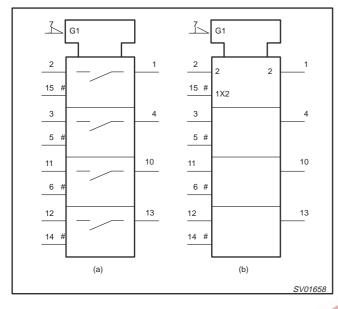
PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
1, 4, 10, 13	1Z – 4Z	Independent inputs/outputs
2, 3, 11, 12	1Y – 4Y	Independent inputs/outputs
7	Ē	Enable input (active LOW)
8	GND	Ground (0V)
9	V _{EE}	Negative supply voltage
15, 5, 6, 14	1S – 4S	Select inputs (active HIGH)
16	V _{CC}	Positive supply voltage

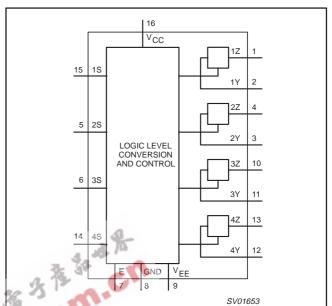
Quad bilateral switches

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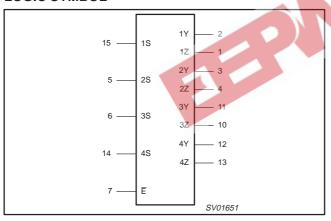
IEC LOGIC SYMBOL



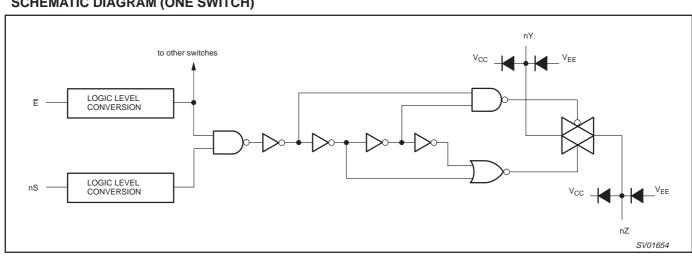
FUNCTIONAL DIAGRAM



LOGIC SYMBOL



SCHEMATIC DIAGRAM (ONE SWITCH)



Quad bilateral switches

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RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
V _{CC}	DC supply voltage	See Note 1	1.0	3.3	6.0	V
VI	Input voltage		0	_	V _{CC}	V
Vo	Output voltage		0	-	V _{CC}	V
T _{amb}	Operating ambient temperature range in free air	See DC and AC characteristics	-40 -40		+85 +125	°C
t _r , t _f	Input rise and fall times	$V_{CC} = 1.0V \text{ to } 2.0V$ $V_{CC} = 2.0V \text{ to } 2.7V$ $V_{CC} = 2.7V \text{ to } 3.6V$ $V_{CC} = 3.6V \text{ to } 5.5V$	- - -	- - - -	500 200 100 50	ns/V

NOTE:

ABSOLUTE MAXIMUM RATINGS^{1, 2}

In accordance with the Absolute Maximum Rating System (IEC 134).

Voltages are referenced to GND (ground = 0 V).

Voltages are	referenced to GND (ground = 0 V).	4		
SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V _{CC}	DC supply voltage	Z 32 - 1	-0.5 to +7.0	V
± I _{IK}	DC input diode current	$V_I < -0.5 \text{ or } V_I > V_{CC} + 0.5V$	20	mA
± I _{OK}	DC output diode current	$V_{\rm O} < -0.5 \text{ or } V_{\rm O} > V_{\rm CC} + 0.5 \text{V}$	20	mA
±I _O	DC switch current	$-0.5V < V_O < V_{CC} + 0.5V$	25	mA
T _{stg}	Storage temperature range		-65 to +150	°C
P _{TOT}	Power dissipation per package – plastic DIL – plastic mini-pack (SO) – plastic shrink mini-pack (SSOP and TSSOP)	for temperature range: -40 to +125°C above +70°C derate linearly with 12 mW/K above +70°C derate linearly with 8 mW/K above +60°C derate linearly with 5.5 mW/K	750 500 400	mW

^{1.} The LV is guaranteed to function down to $V_{CC} = 1.0V$ (input levels GND or V_{CC}); DC characteristics are guaranteed from $V_{CC} = 1.2V$ to $V_{CC} = 5.5V$.

^{1.} Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

^{2.} The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

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DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

					LIMITS			╛
SYMBOL	PARAMETER	TEST CONDITIONS	-40	°C to +8	5°C	-40°C to	+125°C	TINU
			MIN	TYP ¹	MAX	MIN	MAX	1
		V _{CC} = 1.2 V	0.90			0.90		
		V _{CC} = 2.0 V	1.40			1.4		1
V_{IH}	HIGH level Input voltage	V _{CC} = 2.7 to 3.6 V	2.00			2.0		V
	Voltago	V _{CC} = 4.5 V	3.15			3.15		1
		V _{CC} = 6.0 V	4.20			4.20		1
		V _{CC} = 1.2 V			0.30		0.30	
	l. .	V _{CC} = 2.0 V			0.60		0.60	1
V_{IL}	LOW level Input voltage	V _{CC} = 2.7 to 3.6 V			0.80		0.80	V
	Voltage	V _{CC} = 4.5 V			1.35		1.35	1
		V _{CC} = 6.0 V			1.80		1.80	1
±l _l	Input leakage current	$V_{CC} = 3.6 \text{ V}; V_I = V_{CC} \text{ or GND}$ $V_{CC} = 6.0 \text{ V}; V_I = V_{CC} \text{ or GND}$		1.18	1.0 2.0		1.0 2.0	μА
±I _S	Analog switch OFF-state current per channel	V _{CC} = 3.6 V; V _I = V _{IH} or V _{IL} V _{CC} = 6.0 V; V _I = V _{IH} or V _{IL}	为海	0.5	1.0 2.0		1.0 2.0	μА
±I _S	Analog switch ON-state current per channel	V_{CC} = 3.6 V; V_I = V_{IH} or V_{IL} V_{CC} = 6.0 V; V_I = V_{IH} or V_{IL}	CO		1.0 2.0		1.0 2.0	μА
I _{CC}	Quiescent supply current	$V_{CC} = 3.6V; V_I = V_{CC} \text{ or GND}; I_O = 0$ $V_{CC} = 6.0V; V_I = V_{CC} \text{ or GND}; I_O = 0$			20 40		40 80	μА
Δl _{CC}	Additional quiescent supply current per input	$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V; } V_1 = V_{CC} - 0.6 \text{ V}$			500		850	μА
R _{ON}	ON-resistance (peak)	$\begin{array}{c} V_{CC} = 1.2 \; V; \; V_{I} = V_{IH} \; \text{or} \; V_{IL} \\ V_{CC} = 2.0 \; V; \; V_{I} = V_{IH} \; \text{or} \; V_{IL} \\ V_{CC} = 2.7 \; V; \; V_{I} = V_{IH} \; \text{or} \; V_{IL} \\ V_{CC} = 3.0 \; \text{to} \; 3.6 \; V; \; V_{I} = V_{IH} \; \text{or} \; V_{IL} \\ V_{CC} = 4.5 \; V; \; V_{I} = V_{IH} \; \text{or} \; V_{IL} \\ V_{CC} = 6.0 \; V; \; V_{I} = V_{IH} \; \text{or} \; V_{IL} \end{array}$		295 120 110 80 70	- 860 300 270 200 180		- 990 360 325 240 215	Ω
R _{ON}	ON-resistance (rail)	$\begin{array}{c} V_{CC} = 1.2 \; V; \; V_I = V_{IH} \; \text{or} \; V_{IL} \\ V_{CC} = 2.0 \; V; \; V_I = V_{IH} \; \text{or} \; V_{IL} \\ V_{CC} = 2.7 \; V; \; V_I = V_{IH} \; \text{or} \; V_{IL} \\ V_{CC} = 3.0 \; \text{to} \; 3.6 \; V; \; V_I = V_{IH} \; \text{or} \; V_{IL} \\ V_{CC} = 4.5 \; V; \; V_I = V_{IH} \; \text{or} \; V_{IL} \\ V_{CC} = 6.0 \; V; \; V_I = V_{IH} \; \text{or} \; V_{IL} \end{array}$		225 110 85 55 40 35	- 240 150 135 100 90		290 180 180 180 120 110	Ω
R _{ON}	ON-resistance (rail)	$\begin{split} &V_{CC} = 1.2 \; V; \; V_I = V_{IH} \; \text{or} \; V_{IL} \\ &V_{CC} = 2.0 \; V; \; V_I = V_{IH} \; \text{or} \; V_{IL} \\ &V_{CC} = 2.7 \; V; \; V_I = V_{IH} \; \text{or} \; V_{IL} \\ &V_{CC} = 3.0 \; \text{to} \; 3.6 \; V; \; V_I = V_{IH} \; \text{or} \; V_{IL} \\ &V_{CC} = 4.5 \; V; \; V_I = V_{IH} \; \text{or} \; V_{IL} \\ &V_{CC} = 6.0 \; V; \; V_I = V_{IH} \; \text{or} \; V_{IL} \end{split}$		250 120 75 60 45 40	– 270 170 155 115 105		- 325 205 180 135 120	Ω
ΔR _{ON}	Maximum variation of ON-resistance between any two channels	$\begin{array}{c} V_{CC} = 1.2 \; V; \; V_I = V_{IH} \; \text{or} \; V_{IL} \\ V_{CC} = 2.0 \; V; \; V_I = V_{IH} \; \text{or} \; V_{IL} \\ V_{CC} = 2.7 \; V; \; V_I = V_{IH} \; \text{or} \; V_{IL} \\ V_{CC} = 3.0 \; \text{to} \; 3.6 \; V; \; V_I = V_{IH} \; \text{or} \; V_{IL} \\ V_{CC} = 4.5 \; V; \; V_I = V_{IH} \; \text{or} \; V_{IL} \\ V_{CC} = 6.0 \; V; \; V_I = V_{IH} \; \text{or} \; V_{IL} \end{array}$		- 5 4 4 3 2				Ω

NOTE:

1. All typical values are measured at T_{amb} = 25°C.

2. At supply voltage approaching 1.2V, the analog switch ON-resistance becomes extremely non-linear. Therefore it is recommended that these devices be used to transmit digital signals only, when using these supply voltages.

Quad bilateral switches

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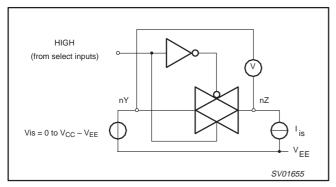


Figure 1. Test circuit for measuring ON-resistance ($R_{on)}$.

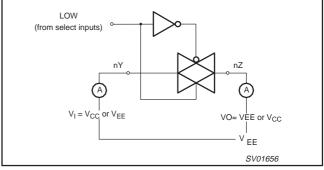


Figure 2. Test circuit for measuring OFF-state current.

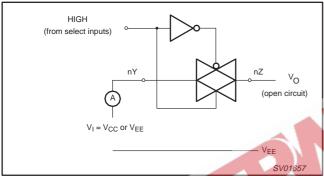


Figure 3. Test circuit for measuring ON-state current.

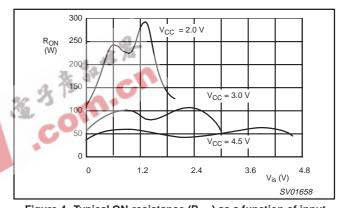


Figure 4. Typical ON-resistance (R_{ON}) as a function of input voltage (V_{is}) for $V_{is} = 0$ to $V_{CC} - V_{EE}$.

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AC CHARACTERISTICS

 $GND = 0 \text{ V; } t_{f} = t_{f} \leq 2.5 \text{ns; } C_{L} = 50 \text{pF}$

				LIMITS					CONDITION
SYMBOL	PARAMETER		40 to +85 °	C	–40 to	+125 °C	UNIT	'	CONDITION
		MIN	TYP ¹	MAX	MIN	MAX		V _{CC} (V)	OTHER
			30					1.2	
			10	19		24		2.0	1_
t _{PHL} /t _{PLH}	Propagation delay		8	14		18	ns	2.7	$R_L = \infty$; $C_L = 50 \text{ pF}$
PHL/PLH	V_{is} to V_{os}		6 [*]	11		14	113	3.0 to 3.6	Figure 12
			5	9		12		4.5	1
			4	7		9		6.0	1
			110					1.2	
			37	70		85		2.0]
t _{PZH} /t _{PZL}	Turn-on time		28	51		63	ns	2.7	$R_L = 1 \text{ k}\Omega;$ $C_L = 50 \text{ pF}$
'PZH' 'PZL	Ē to V _{os}		21 ²	41		50	110	3.0 to 3.6	Figures 13 and 14
			19	35		43	4	4.5]
			15	27		33	. J. J. J.	6.0	
			95			- 85c	34	1.2	1
			32	61	4	75		2.0	$R_L = 1 \text{ k}\Omega;$
t _{PZH} /t _{PZL}	Turn-on time nS to V _{os}		24	45	. 76	55	ns	2.7	$C_{L} = 50 \text{ pF}$
	113 to v _{os}		18 ²	36	4 400	44		3.0 to 3.6	Figures 13 and 14
			16	31		37 29		4.5	1
			12	23		29		6.0 1.2	
			37	68		80		2.0	-
	Turn-off time		28	51		59		2.7	$R_L = 1 \text{ k}\Omega;$
t _{PHZ} /t _{PLZ}	E to V _{os}		22 ²	41		48	ns	3.0 to 3.6	C _L = 50 pF Figures 13 and 14
	55		20	35		41		4.5	Figures 13 and 14
			16	28		32		6.0	1
			90			 		1.2	
			32	59		70		2.0	1
4 /4	Turn-off time		24	44		52		2.7	$R_L = 1 \text{ k}\Omega;$ $C_L = 50 \text{ pF}$
t _{PHZ} /t _{PLZ}	nS to V _{os}		19 ²	36		42	ns	3.0 to 3.6	G _L = 50 pr Figures 13 and 14
			17	31		36		4.5	3:
			14	24		28		6.0	1

NOTES:

All typical values are measured at T_{amb} = 25°C.
 All typical values are measured at V_{CC} = 3.3V

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ADDITIONAL AC CHARACTERISTICS

GND = 0 V; $t_r = t_f \le 2.5 \text{ns}$; $C_L = 50 \text{pF}$

SYMBOL	PARAMETER	TYP	UNIT	V _{CC} (V)	V _{IS(P-P)} (V)	CONDITIONS
	Sine-wave distortion f = 1 kHz	0.80	%	3.0	2.75	$R_L = 10 \text{ k}\Omega; C_L = 50 \text{ pF}$
	Sine-wave distortion 1 = 1 KHZ	0.40	76	6.0	5.50	Figure 10
	Sine-wave distortion f = 10 kHz	2.40	%	3.0	2.75	$R_L = 10 \text{ k}\Omega; C_L = 50 \text{ pF}$
	Sine-wave distortion i = 10 ki iz	1.20	/0	6.0	5.50	Figure 10
	Switch "OFF" signal feed through	-50	dB	3.0	Note 1	$R_L = 600 \text{ k}\Omega; C_L = 50 \text{ pF}; f=1 \text{ MHz}$
	Switch Of F signal reed through	-50	uБ	6.0		Figures 5 and 11
	Crosstalk between any two switches	-60	dB	3.0	Note 1	$R_L = 600 \text{ k}\Omega; C_L = 50 \text{ pF}; f=1 \text{ MHz}$
	Closstaik between any two switches	-60	uБ	6.0		Figure 7
V _(p-p)	Crosstalk voltage between enable or address	110	mV	3.0		R_L = 600 kΩ; C_L = 50 pF; f=1 MHz (nS or \overline{E} , square wave between V_{CC}
(p-p)	input to any switch (peak-to-peak value)	220	111.0	6.0		and GND, $T_r = t_f = 6$ ns) Figure 8
f	Minimum frequency response (–3 dB)	180	mHz	3.0	Note 2	$R_L = 50 \text{ k}\Omega; C_L = 50 \text{ pF}$
† _{max}	willimiditi frequency response (=3 db)	200	111112	6.0	2_	Figures 6 and 9
Cs	Maximum switch capacitance	5	pF		JE /D	

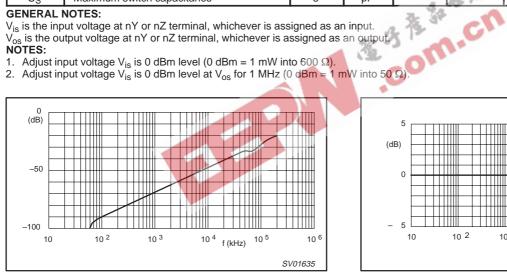


Figure 5. Typical switch "OFF" signal feed-through as a function of frequency.

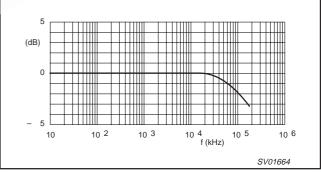


Figure 6. Typical frequency response.

NOTES TO FIGURES 5 AND 6:

Test conditions: V_{CC} = 3.0 V; GND = 0 V; R_L = 50 Ω ; R_{SOURCE} = 1k Ω .

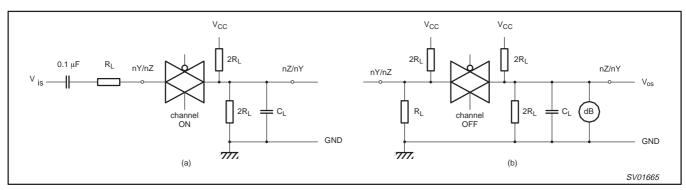


Figure 7. Test circuit for measuring crosstalk between any two switches. (a) channel ON condition; (b) channel OFF condition.

Quad bilateral switches

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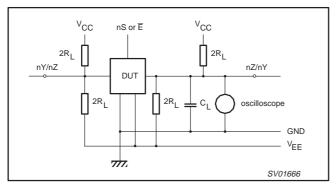
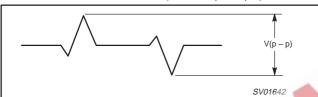


Figure 8. Test circuit for measuring crosstalk between control and any switch.

NOTE TO FIGURE 8:

The crosstalk is defined as follows (oscilloscope output):



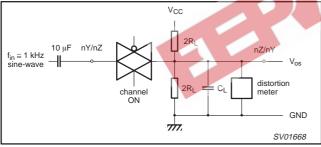


Figure 10. Test circuit for measuring sine-wave distortion.

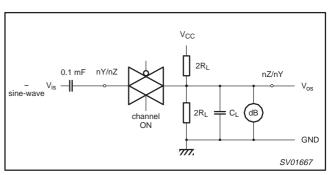


Figure 9. Test circuit for measuring minimum frequency response.

NOTE TO FIGURE 9:

Adjust input voltage to obtain 0 dBm at V_{OS} when F_{in} = 1 MHz. After set-up frequency of f_{in} is increased to obtain a reading of -3 dB at V_{OS} .

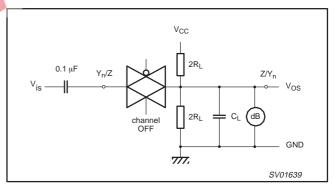


Figure 11. Test circuit for measuring switch "OFF" signal feed-through.

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SY00044

WAVEFORMS

 V_M = 1.5 V at 2.7 V \leq V_{CC} \leq 3.6 V V_M = 0.5 \times V_{CC} at 2.7 V > V_{CC} > 3.6 V V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load

 $\begin{array}{l} \text{V}_{\text{X}} = \text{V}_{\text{OL}} + 0.3 \text{ V at } 2.7 \text{ V} \leq \text{V}_{\text{CC}} \leq 3.6 \text{ V} \\ \text{V}_{\text{X}} = \text{V}_{\text{OL}} + 0.1 \times \text{V}_{\text{CC}} \text{ at } 2.7 \text{ V} > \text{V}_{\text{CC}} > 3.6 \text{ V} \\ \text{V}_{\text{Y}} = \text{V}_{\text{OH}} - 0.3 \text{ V at } 2.7 \text{ V} \leq \text{V}_{\text{CC}} \leq 3.6 \text{ V} \\ \text{V}_{\text{Y}} = \text{V}_{\text{OH}} - 0.1 \times \text{V}_{\text{CC}} \text{ at } 2.7 \text{ V} > \text{V}_{\text{CC}} > 3.6 \text{ V} \end{array}$

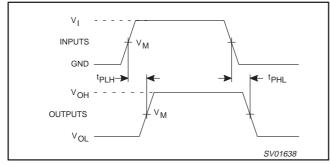


Figure 12. Input (Vis) to output (Vos) propagation delays.

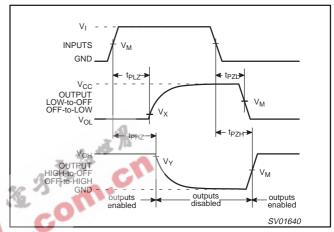


Figure 13. Turn-on and turn-off times for the inputs (nS, \overline{E}) to the output (V_{os}).

TEST CIRCUIT

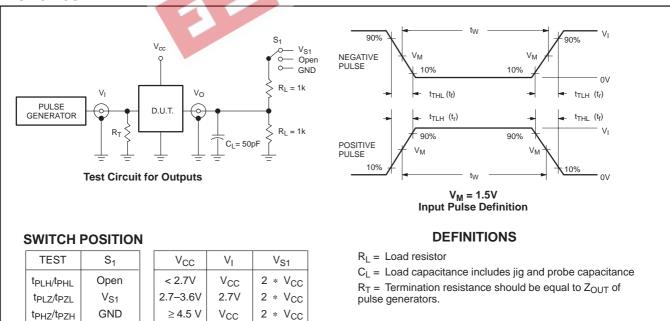


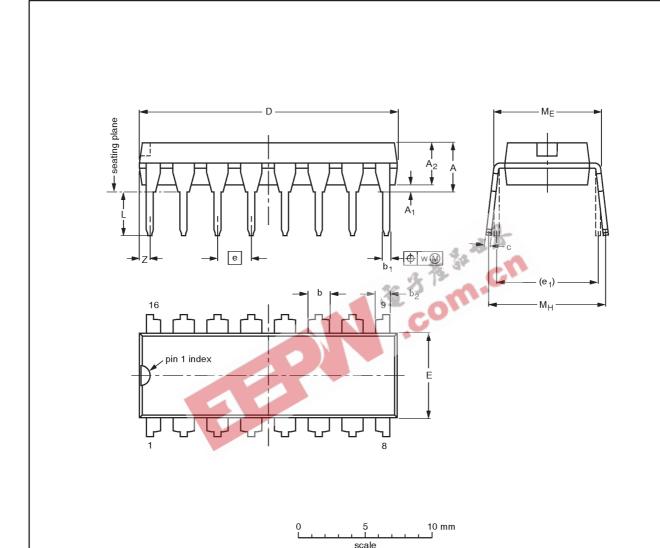
Figure 14. Load circuitry for switching times.

Quad bilateral latches

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DIP16: plastic dual in-line package; 16 leads (300 mil)

SOT38-4



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A ₁ min.	A ₂ max.	b	b ₁	b ₂	С	D ⁽¹⁾	E ⁽¹⁾	е	e ₁	L	ME	M _H	w	Z ⁽¹⁾ max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	1.25 0.85	0.36 0.23	19.50 18.55	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	0.76
inches	0.17	0.020	0.13	0.068 0.051	0.021 0.015	0.049 0.033	0.014 0.009	0.77 0.73	0.26 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.030

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

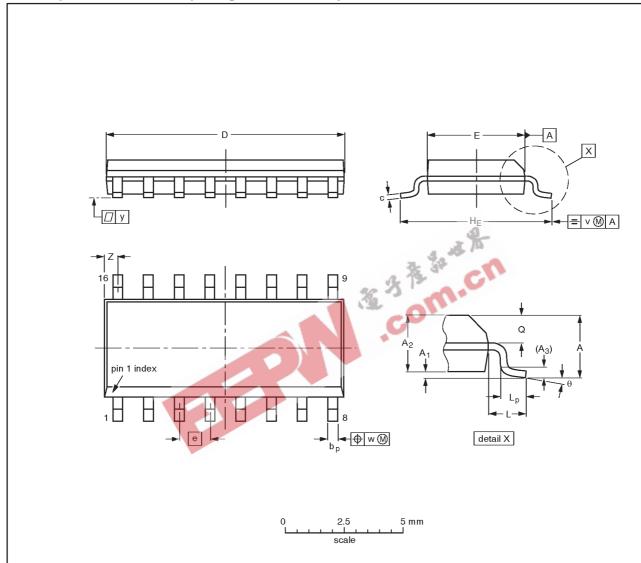
OUTLINE		EUROPEAN	ISSUE DATE		
VERSION	IEC	JEDEC	EIAJ	PROJECTION	ISSUE DATE
SOT38-4					92-11-17 95-01-14

Quad bilateral latches

74LV4316

SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

								_											
UN	IT I	A nax.	A ₁	A ₂	A ₃	bp	С	D ⁽¹⁾	E ⁽¹⁾	е	HE	L	Lp	O	v	w	у	Z ⁽¹⁾	θ
m	n 1	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8°
incl	ies 0.	ากผลา	0.0098 0.0039		0.01		0.0098 0.0075	0.39 0.38	0.16 0.15	0.050	0.24 0.23	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	0°

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

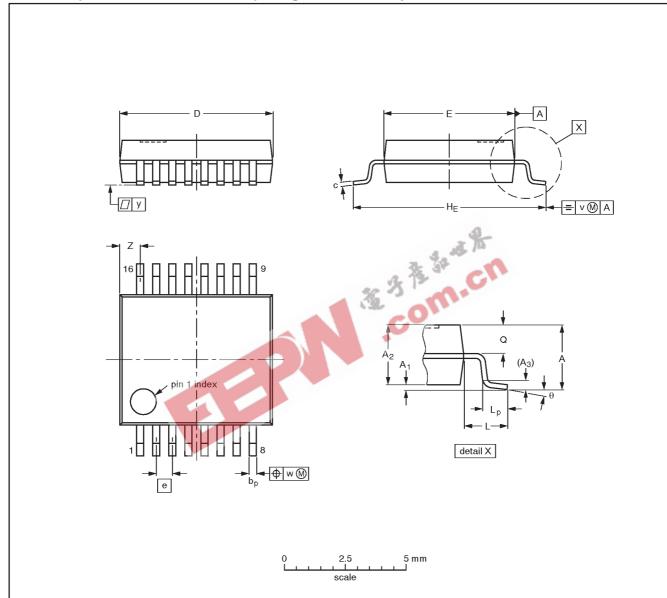
OUTLINE		REFEF	RENCES	EUROPEAN	ISSUE DATE
VERSION	IEC	JEDEC	EIAJ	PROJECTION	ISSUE DATE
SOT109-1	076E07S	MS-012AC			91-08-13 95-01-23

Quad bilateral latches

74LV4316

SSOP16: plastic shrink small outline package; 16 leads; body width 5.3 mm

SOT338-1



DIMENSIONS (mm are the original dimensions)

Billiant of the difference (in the difference)																		
UNIT	A max.	Α1	A ₂	A ₃	bp	С	D ⁽¹⁾	E ⁽¹⁾	е	HE	L	Lp	Q	v	w	у	Z ⁽¹⁾	θ
mm	2.0	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	6.4 6.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	1.00 0.55	8° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

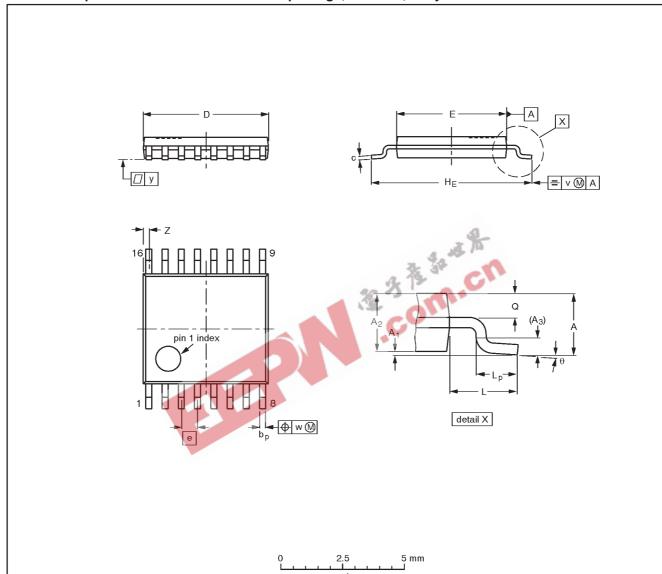
OUTLINE VERSION		REFER	EUROPEAN	ISSUE DATE		
	IEC	JEDEC	EIAJ		PROJECTION	ISSUE DATE
SOT338-1		MO-150AC				94-01-14 95-02-04

Quad bilateral latches

74LV4316

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm

SOT403-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	Α1	A ₂	А3	bр	С	D ⁽¹⁾	E ⁽²⁾	е	HE	L	Lp	Ø	v	w	у	Z ⁽¹⁾	θ
mm	1.10	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1.0	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.40 0.06	8° 0°

Notes

- 1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
- 2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE		REFER	EUROPEAN	ISSUE DATE		
VERSION	IEC	JEDEC	EIAJ		PROJECTION	1930E DATE
SOT403-1		MO-153				-94-07-12- 95-04-04

Quad bilateral latches

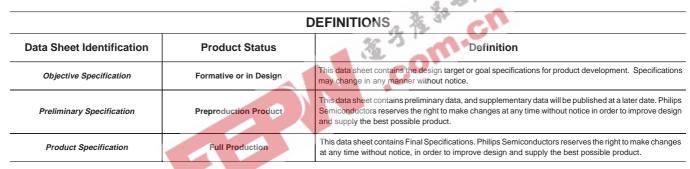
74LV4316

NOTES



Quad bilateral switches

74LV4316



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print code Date of release: 05-96

Document order number: 9397-750-04663

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