FAIRCHILD

SEMICONDUCTOR

### 74F269 8-Bit Bidirectional Binary Counter

#### **General Description**

The 74F269 is a fully synchronous 8-stage up/down counter featuring a preset capability for programmable operation, carry lookahead for easy cascading and a U/D input to control the direction of counting. All state changes, whether in counting or parallel loading, are initiated by the rising edge of the clock.

#### Built-in lookahead carry capability

Features

Count frequency 100 MHz

Synchronous counting and loading

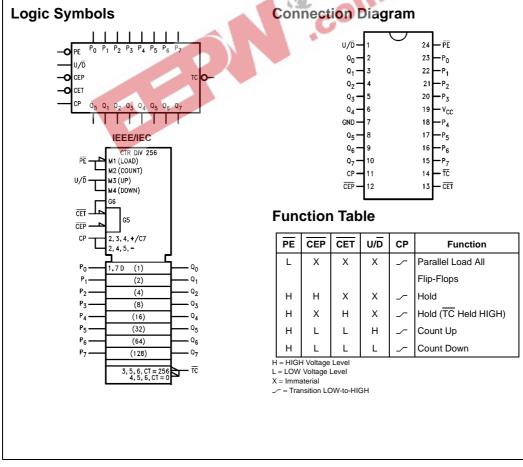
1

- Supply current 113 mA typ
- 300 mil slimline package

#### **Ordering Code:**

Order Number	Package Number	Package Description
74F269SC	M24B	24-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide
74F269SPC	N24C	24-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide





© 2000 Fairchild Semiconductor Corporation DS009510 April 1988 Revised September 2000

Dia Mara	Description	U.L.	Input I <sub>IH</sub> /I <sub>IL</sub>
Pin Nam	es Description	HIGH/LOW	Output I <sub>OH</sub> /I <sub>OL</sub>
P <sub>0</sub> –P <sub>7</sub>	Parallel Data Inputs	1.0/1.0	20 µA/–0.6 mA
PE	Parallel Enable Input (Active LOW)	1.0/1.0	20 µA/–0.6 mA
U/D	Up-Down Count Control Input	1.0/1.0	20 µA/–0.6 mA
CEP	Count Enable Parallel Input (Active LOW)	1.0/1.0	20 µA/–0.6 mA
CET	Count Enable Trickle Input (Active LOW)	1.0/1.0	20 µA/–0.6 mA
CP	Clock Input	1.0/1.0	20 µA/–0.6 mA
TC	Terminal Count Output (Active LOW)	5.0/33.3	–1 mA/20 mA
Q <sub>0</sub> –Q <sub>7</sub>	Flip-Flop Outputs	50/33.3	–1 mA/20 mA
ogic Diagra	m		
	CET CEP PE CP	U/D	
	$\dot{\nabla}$	< 🖓 👝	2
	1 of 8		
		A La	∙D- <u>i</u> ll-∾
		¬++-℃	٦ <u>اا</u>
		ĸ	אן <u>ו</u> ו
Ρ	╷┼──┊╪┚╍┶╸┼═╴╕╱┼╚	D-1	
	۰		≗–
		「 <u></u>	
P	сік	U D	A1 Q1
	ск	U D	A2 Q2
-		UD	AQ_3
P	₃ <b>╶┼╢╢┍──╁────</b> ┟─────┼─────┼─────┼────┼───		
		UD	Q4
P			
			<b></b>
Ρ	╕᠆ᡰᢔᠯᠯᠯᡖ᠋᠊ᡜᠯᢪᢆ᠂᠇ᡶ		<u>∧</u> 5Q5
		UD	
P		   1	A <sub>6</sub> Q <sub>6</sub>
		UD	A7 07
p.	, <u> </u>		
	Ų		
	TC		
	TC		

#### Absolute Maximum Ratings(Note 1)

	-
Storage Temperature	-65°C to +150°C
Ambient Temperature under Bias	$-55^{\circ}C$ to $+125^{\circ}C$
Junction Temperature under Bias	$-55^{\circ}C$ to $+150^{\circ}C$
V <sub>CC</sub> Pin Potential to Ground Pin	-0.5V to +7.0V
Input Voltage (Note 2)	-0.5V to +7.0V
Input Current (Note 2)	-30 mA to +5.0 mA
Voltage Applied to Output	
in HIGH State (with $V_{CC} = 0V$ )	
Standard Output	-0.5V to V <sub>CC</sub>
3-STATE Output	-0.5V to +5.5V
Current Applied to Output	
in LOW State (Max)	twice the rated I <sub>OL</sub> (mA)

# Recommended Operating Conditions

Free Air Ambient Temperature	
Supply Voltage	

74F269

0°C to +70°C +4.5V to +5.5V

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

### **DC Electrical Characteristics**

Symbol	Parameter		Min	Тур	Max	Units	Vcc	Conditions
V <sub>IH</sub>	Input HIGH Voltage		2.0			V	A	Recognized as a HIGH Signal
V <sub>IL</sub>	Input LOW Voltage				0.8	V		Recognized as a LOW Signal
V <sub>CD</sub>	Input Clamp Diode Voltage				-1.2	V	Min	$I_{IN} = -18 \text{ mA}$
V <sub>OH</sub>	Output HIGH Voltage	10% V <sub>CC</sub> 5% V <sub>CC</sub>	2.5 2.7		36 3	v	Min	I <sub>OH</sub> = −1 mA I <sub>OH</sub> = −1 mA
V <sub>OL</sub>	Output LOW Voltage	10% V <sub>CC</sub>			0.5	V	Min	I <sub>OL</sub> = 20 mA
I <sub>IH</sub>	Input HIGH Current				5.0	μA	Max	V <sub>IN</sub> = 2.7V
I <sub>BVI</sub>	Input HIGH Current Breakdown Test				7.0	μA	Max	$V_{IN} = 7.0V$
ICEX	Output HIGH Leakage Current				50	μA	Max	$V_{OUT} = V_{CC}$
V <sub>ID</sub>	Input Leakage Test		4.75			V	0.0	I <sub>ID</sub> = 1.9 μA, All Other Pins Grounded
I <sub>OD</sub>	Output Leakage Circuit Current				3.75	μA	0.0	V <sub>IOD</sub> = 150 mV All Other Pins Grounded
I <sub>IL</sub>	Input LOW Current				-0.6	mA	Max	$V_{IN} = 0.5V$
los	Output Short-Circuit Current		-60		-150	mA	Max	$V_{OUT} = 0V$
I <sub>CCH</sub>	Power Supply Current		1	104	125	mA	Max	V <sub>O</sub> = HIGH
I <sub>CCL</sub>	Power Supply Current			113	135	mA	Max	V <sub>O</sub> = LOW

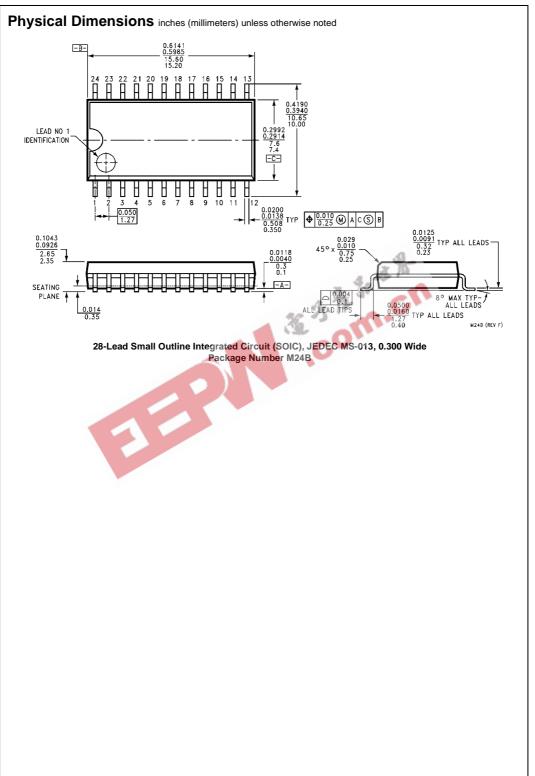
80	
Ñ	
ЦĻ	
2	

## AC Electrical Characteristics

Symbol	Parameter	T <sub>A</sub> = +25°C V <sub>CC</sub> = +5.0V C <sub>L</sub> = 50 pF			$T_{A} = 0^{\circ}C \text{ to } +70^{\circ}C$ $V_{CC} = 5.0V$ $C_{L} = 50 \text{ pF}$		Units
		Min	Тур	Max	Min	Max	
f <sub>MAX</sub>	Maximum Clock Frequency	100			85		MHz
t <sub>PLH</sub>	Propagation Delay	3.5		8.0	3.5	7.0	ns
t <sub>PHL</sub>	CP to Q <sub>n</sub> (Count-Up)	4.5		10.5	4.5	11.0	
t <sub>PLH</sub>	Propagation Delay	3.5		7.5	3.5	10.0	ns
t <sub>PHL</sub>	U/D to TC	4.5		7.5	4.5	11.0	
t <sub>PLH</sub>	Propagation Delay	3.5		7.0	3.5	10.5	ns
t <sub>PHL</sub>	CET to TC	3.0		10.5	3.0	11.5	
t <sub>PLH</sub>	Propagation Delay	4.5		10.0	4.5	10.5	ns
t <sub>PHL</sub>	CP to TC	5.0		10.0	4.5	10.5	
t <sub>PLH</sub>	Propagation Delay	3.5		10.5	3.5	11.0	ns
t <sub>PHL</sub>	CP to <sub>Qn</sub> (Count-Down)	4.5		10.5	4.5	11.0	
t <sub>PLH</sub>	Propagation Delay	3.5		7.0	3.5	10.0	ns
t <sub>PHL</sub>	CP to Q <sub>n</sub> (Load)	4.0		7.0	4.0	7.0	ns

# AC Operating Requirements

		T <sub>A</sub> = +25°C	$T_A = 0^\circ C$ to $+70^\circ C$				
Symbol	Parameter	V <sub>CC</sub> = +5.0V	$V_{CC} = 5.0V$	Units			
		Min Max	Min Max				
t <sub>S</sub> (H)	Setup Time, HIGH or LOW	3.5	4.0				
t <sub>S</sub> (L)	Data to CP	3.0	3.0				
t <sub>H</sub> (H)	Hold Time, HIGH or LOW	1.0	2.0	ns			
t <sub>H</sub> (L)	Data to CP	1.0	1.0				
t <sub>S</sub> (H)	Setup Time, HIGH or LOW	5.5	6.5				
t <sub>S</sub> (L)	PE to CP	5.5	6.5				
t <sub>H</sub> (H)	Hold Time, HIGH or LOW	0	0	ns			
t <sub>H</sub> (L)	PE to CP	0	0				
t <sub>S</sub> (H)	Setup Time, HIGH or LOW	6.0	6.5				
t <sub>S</sub> (L)	CET or CEP to CP	8.0	9.0	ns			
t <sub>H</sub> (H)	Hold Time, HIGH or LOW	0	0	ns			
t <sub>H</sub> (L)	CET or CEP to CP	0	0				
t <sub>W</sub> (H)	Clock Pulse Width, HIGH or LOW	3.5	3.5	ns			
t <sub>W</sub> (L)		3.5	4.0	115			
t <sub>S</sub> (H)	Setup Time, HIGH or LOW	8.0	9.5	ns			
t <sub>S</sub> (L)	U/D to CP	6.0	7.0	ns			
t <sub>H</sub> (H)	Hold Time, HIGH or LOW	0.0	0.0	ns			
t <sub>H</sub> (L)	U/D to CP	0.0	0.0	115			



74F269

