

74LCX16374

Low Voltage 16-Bit D-Type Flip-Flop with 5V Tolerant Inputs and Outputs

General Description

The LCX16374 contains sixteen non-inverting D-type flip-flops with 3-STATE outputs and is intended for bus oriented applications. The device is byte controlled. A buffered clock (CP) and Output Enable (\overline{OE}) are common to each byte and can be shorted together for full 16-bit operation.

The LCX16374 is designed for low voltage (2.5V or 3.3V) V_{CC} applications with capability of interfacing to a 5V signal environment.

The LCX16374 is fabricated with an advanced CMOS technology to achieve high speed operation while maintaining CMOS low power dissipation.

Features

- 5V tolerant inputs and outputs
- 2.3V–3.6V V_{CC} specifications provided
- 6.2 ns t_{PD} max ($V_{CC} = 3.3V$), 20 μA I_{CC} max
- Power down high impedance inputs and outputs
- Supports live insertion/withdrawal (Note 1)
- ± 24 mA output drive ($V_{CC} = 3.0V$)
- Uses patented noise/EMI reduction circuitry
- Latch-up performance exceeds 500 mA
- ESD performance:
 - Human body model > 2000V
 - Machine model > 200V
- Also packaged in plastic Fine-Pitch Ball Grid Array (FBGA)

Note 1: To ensure the high-impedance state during power up or down, \overline{OE} should be tied to V_{CC} through a pull-up resistor; the minimum value or the resistor is determined by the current-sourcing capability of the driver.

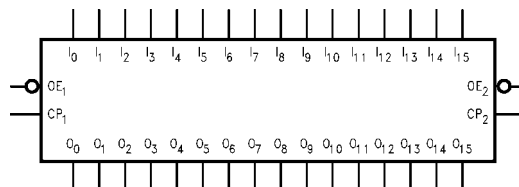
Ordering Code:

Order Number	Package Number	Package Description
74LCX16374G (Note 2)(Note 3)	BGA54A	54-Ball Fine-Pitch Ball Grid Array (FBGA), JEDEC MO-205, 5.5mm Wide
74LCX16374MEA (Note 3)	MS48A	48-Lead Small Shrink Outline Package (SSOP), JEDEC MO-118, 0.300" Wide
74LCX16374MTD (Note 3)	MTD48	48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide

Note 2: Ordering code "G" indicates Trays.

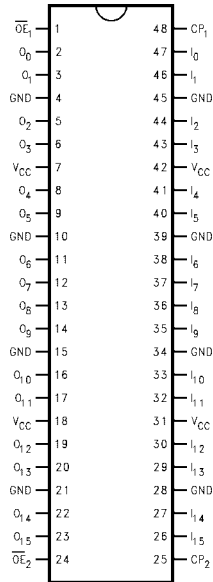
Note 3: Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Logic Symbol

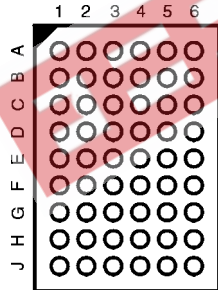


Connection Diagrams

Pin Assignment for SSOP and TSSOP



Pin Assignment for FBGA



(Top Thru View)

Pin Descriptions

Pin Names	Description
\overline{OE}_n	Output Enable Input (Active LOW)
CP _n	Clock Pulse Input
I ₀ -I ₁₅	Inputs
O ₀ -O ₁₅	Outputs
NC	No Connect

FBGA Pin Assignments

	1	2	3	4	5	6
A	O ₀	NC	\overline{OE}_1	CP ₁	NC	I ₀
B	O ₂	O ₁	NC	NC	I ₁	I ₂
C	O ₄	O ₃	V _{CC}	V _{CC}	I ₃	I ₄
D	O ₆	O ₅	GND	GND	I ₅	I ₆
E	O ₈	O ₇	GND	GND	I ₇	I ₈
F	O ₁₀	O ₉	GND	GND	I ₉	I ₁₀
G	O ₁₂	O ₁₁	V _{CC}	V _{CC}	I ₁₁	I ₁₂
H	O ₁₄	O ₁₃	NC	NC	I ₁₃	I ₁₄
J	O ₁₅	NC	\overline{OE}_2	CP ₂	NC	I ₁₅

Truth Tables

	Inputs			Outputs
	CP ₁	\overline{OE}_1	I ₀ -I ₇	O ₀ -O ₇
↗		L	H	H
↘		L	L	L
L		L	X	O ₀
X		H	X	Z

	Inputs			Outputs
	CP ₂	\overline{OE}_2	I ₈ -I ₁₅	O ₈ -O ₁₅
↗		L	H	H
↘		L	L	L
L		L	X	O ₀
X		H	X	Z

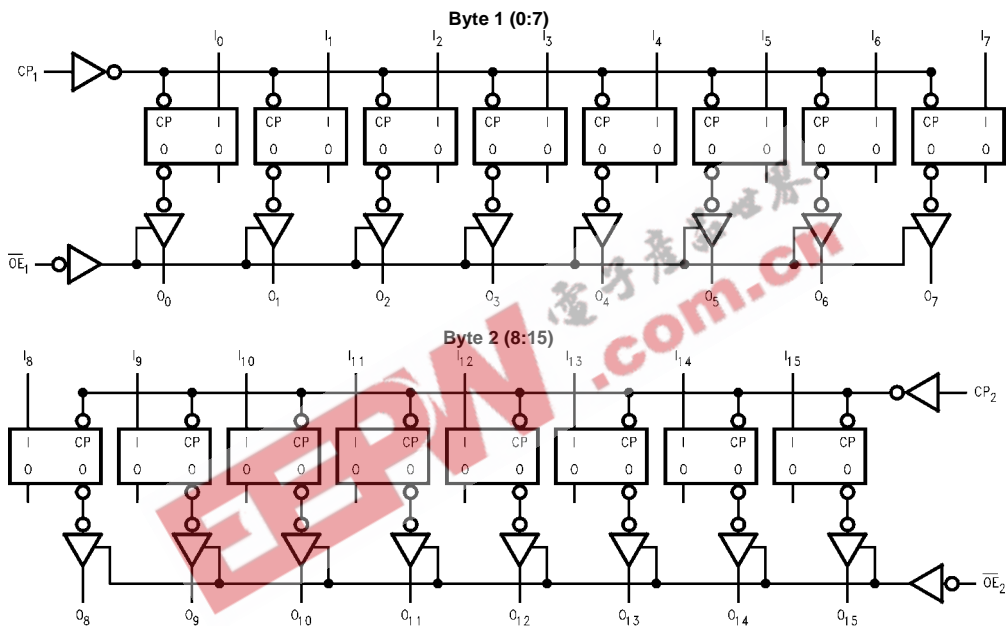
H = HIGH Voltage Level
 L = LOW Voltage Level
 X = Immaterial
 Z = High Impedance
 O₀ = Previous O₀ before HIGH-to-LOW of CP

Functional Description

The LCX16374 consists of sixteen edge-triggered flip-flops with individual D-type inputs and 3-STATE true outputs. The device is byte controlled with each byte functioning identically, but independent of the other. The control pins can be shorted together to obtain full 16-bit operation. Each byte has a buffered clock and buffered Output Enable common to all flip-flops within that byte. The description which follows applies to each byte. Each flip-flop will store the

state of their individual D inputs that meet the setup and hold time requirements on the LOW-to-HIGH Clock (CP_n) transition. With the Output Enable (\overline{OE}_n) LOW, the contents of the flip-flops are available at the outputs. When \overline{OE}_n is HIGH, the outputs go to the high impedance state. Operation of the \overline{OE}_n input does not affect the state of the flip-flops.

Logic Diagrams



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 4)

Symbol	Parameter	Value	Conditions	Units
V _{CC}	Supply Voltage	-0.5 to +7.0		V
V _I	DC Input Voltage	-0.5 to +7.0		V
V _O	DC Output Voltage	-0.5 to +7.0 -0.5 to V _{CC} + 0.5	3-STATE Output in HIGH or LOW State (Note 5)	V
I _{IK}	DC Input Diode Current	-50	V _I < GND	mA
I _{OK}	DC Output Diode Current	-50 +50	V _O < GND V _O > V _{CC}	mA
I _O	DC Output Source/Sink Current	±50		mA
I _{CC}	DC Supply Current per Supply Pin	±100		mA
I _{GND}	DC Ground Current per Ground Pin	±100		mA
T _{STG}	Storage Temperature	-65 to +150		°C

Note 4: The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the Absolute Maximum Ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 5: I_O Absolute Maximum Rating must be observed.

Recommended Operating Conditions (Note 6)

Symbol	Parameter	Min	Max	Units
V _{CC}	Supply Voltage	Operating Data Retention 2.0 1.5	3.6 3.6	V
V _I	Input Voltage	0	5.5	V
V _O	Output Voltage	HIGH or LOW State 3-STATE 0 0	V _{CC} 5.5	V
I _{OH} /I _{OL}	Output Current	V _{CC} = 3.0V - 3.6V V _{CC} = 2.7V - 3.0V V _{CC} = 2.3V - 2.7V	±24 ±12 ±8	mA
T _A	Free-Air Operating Temperature	-40	85	°C
Δt/ΔV	Input Edge Rate, V _{IN} = 0.8V - 2.0V, V _{CC} = 3.0V	0	10	ns/V

Note 6: Unused inputs must be held HIGH or LOW. They may not float.

DC Electrical Characteristics

Symbol	Parameter	Conditions	V _{CC} (V)		T _A = -40°C to +85°C		Units
			Min	Max	Min	Max	
V _{IH}	HIGH Level Input Voltage		2.3 - 2.7	1.7			V
			2.7 - 3.6	2.0			
V _{IL}	LOW Level Input Voltage		2.3 - 2.7		0.7		V
			2.7 - 3.6		0.8		
V _{OH}	HIGH Level Output Voltage	I _{OH} = -100 μA	2.3 - 3.6	V _{CC} - 0.2			V
		I _{OH} = -8 mA	2.3	1.8			
		I _{OH} = -12 mA	2.7	2.2			
		I _{OH} = -18 mA	3.0	2.4			
		I _{OH} = -24 mA	3.0	2.2			
V _{OL}	LOW Level Output Voltage	I _{OL} = 100 μA	2.3 - 3.6		0.2		V
		I _{OL} = 8 mA	2.3		0.6		
		I _{OL} = 12 mA	2.7		0.4		
		I _{OL} = 16 mA	3.0		0.4		
		I _{OL} = 24 mA	3.0		0.55		
I _I	Input Leakage Current	0 ≤ V _I ≤ 5.5V	2.3 - 3.6		±5.0	μA	
I _{OZ}	3-STATE Output Leakage	0 ≤ V _O ≤ 5.5V V _I = V _{IH} or V _{IL}	2.3 - 3.6		±5.0	μA	
I _{OFF}	Power-Off Leakage Current	V _I or V _O = 5.5V	0		10	μA	

DC Electrical Characteristics (Continued)								
Symbol	Parameter	Conditions	V _{CC} (V)	T _A = -40°C to +85°C		Units		
				Min	Max			
I _{CC}	Quiescent Supply Current	V _I = V _{CC} or GND	2.3 – 3.6		20	μA		
		3.6V ≤ V _I , V _O ≤ 5.5V (Note 7)	2.3 – 3.6		±20			
ΔI _{CC}	Increase in I _{CC} per Input	V _{IH} = V _{CC} - 0.6V	2.3 – 3.6		500	μA		
Note 7: Outputs disabled or 3-STATE only.								
AC Electrical Characteristics								
Symbol	Parameter	T _A = -40° to +85°C, R _L = 500Ω						Units
		V _{CC} = 3.3V ± 0.3V		V _{CC} = 2.7V		V _{CC} = 2.5V ± 0.2V		
		C _L = 50 pF		C _L = 50 pF		C _L = 30 pF		
		Min	Max	Min	Max	Min	Max	
f _{MAX}	Maximum Clock Frequency	170						MHz
t _{PHL}	Propagation Delay	1.5	6.2	1.5	6.5	1.5	7.4	ns
t _{PLH}	CP to O _n	1.5	6.2	1.5	6.5	1.5	7.4	
t _{PZL}	Output Enable time	1.5	6.1	1.5	6.3	1.5	7.9	ns
t _{PZH}		1.5	6.1	1.5	6.3	1.5	7.9	
t _{PLZ}	Output Disable Time	1.5	6.0	1.5	6.2	1.5	7.2	ns
t _{PHZ}		1.5	6.0	1.5	6.2	1.5	7.2	
t _S	Setup Time	2.5		2.5		3.0		ns
t _H	Hold Time	1.5		1.5		2.0		ns
t _W	Pulse Width	3.0		3.0		3.5		ns
t _{OSSL}	Output to Output Skew (Note 8)		1.0					ns
t _{OSLH}			1.0					
Note 8: Skew is defined as the absolute value of the differences between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t _{OSSL}) or LOW-to-HIGH (t _{OSLH}). Parameter guaranteed by design.								
Dynamic Switching Characteristics								
Symbol	Parameter	Conditions	V _{CC} (V)	T _A = 25°C		Units		
				Typical				
V _{OLP}	Quiet Output Dynamic Peak V _{OL}	C _L = 50 pF, V _{IH} = 3.3V, V _{IL} = 0V	3.3	0.8	V			
		C _L = 30 pF, V _{IH} = 2.5V, V _{IL} = 0V	2.5	0.6				
V _{OLV}	Quiet Output Dynamic Valley V _{OL}	C _L = 50 pF, V _{IH} = 3.3V, V _{IL} = 0V	3.3	-0.8	V			
		C _L = 30 pF, V _{IH} = 2.5V, V _{IL} = 0V	2.5	0.6				
Capacitance								
Symbol	Parameter	Conditions	Typical	Units				
C _{IN}	Input Capacitance	V _{CC} = Open, V _I = 0V or V _{CC}	7	pF				
C _{OUT}	Output Capacitance	V _{CC} = 3.3V, V _I = 0V or V _{CC}	8	pF				
C _{PD}	Power Dissipation Capacitance	V _{CC} = 3.3V, V _I = 0V or V _{CC} , f = 10 MHz	20	pF				

AC LOADING and WAVEFORMS Generic for LCX Family

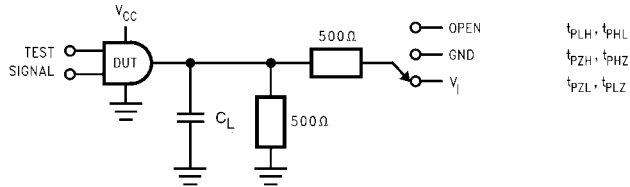


FIGURE 1. AC Test Circuit (C_L includes probe and jig capacitance)

Test	Switch
t_{PLH}, t_{PHL}	Open
t_{PZL}, t_{PLZ}	6V at $V_{CC} = 3.3 \pm 0.3V$, and 2.7V $V_{CC} \times 2$ at $V_{CC} = 2.5 \pm 0.2V$
t_{PZH}, t_{PHZ}	GND

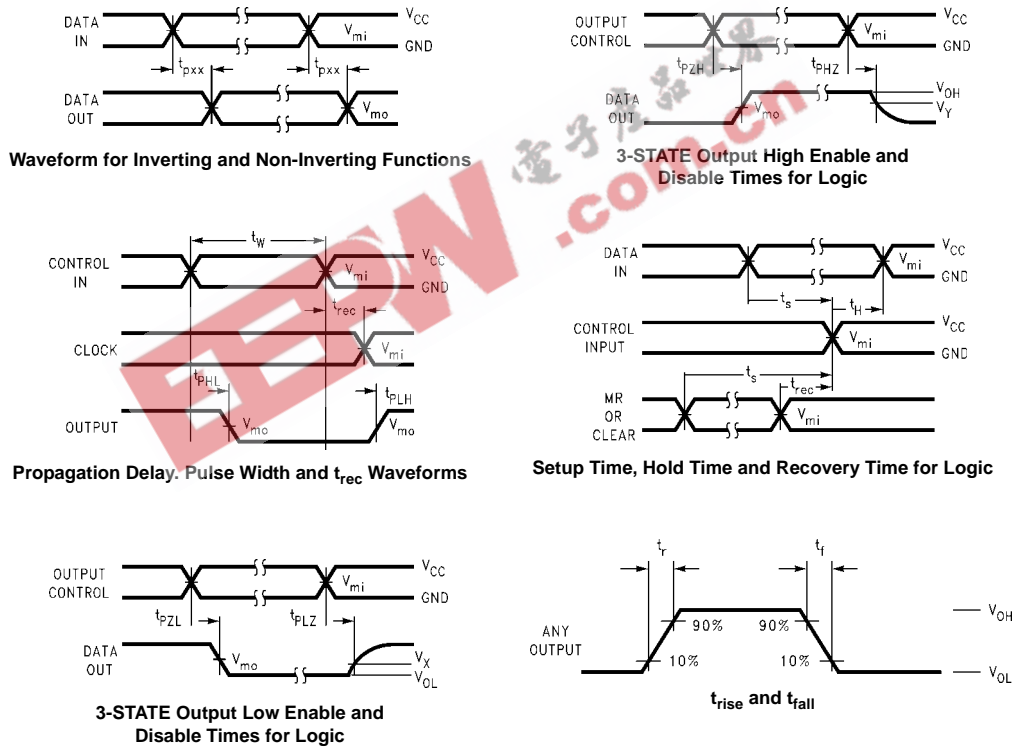
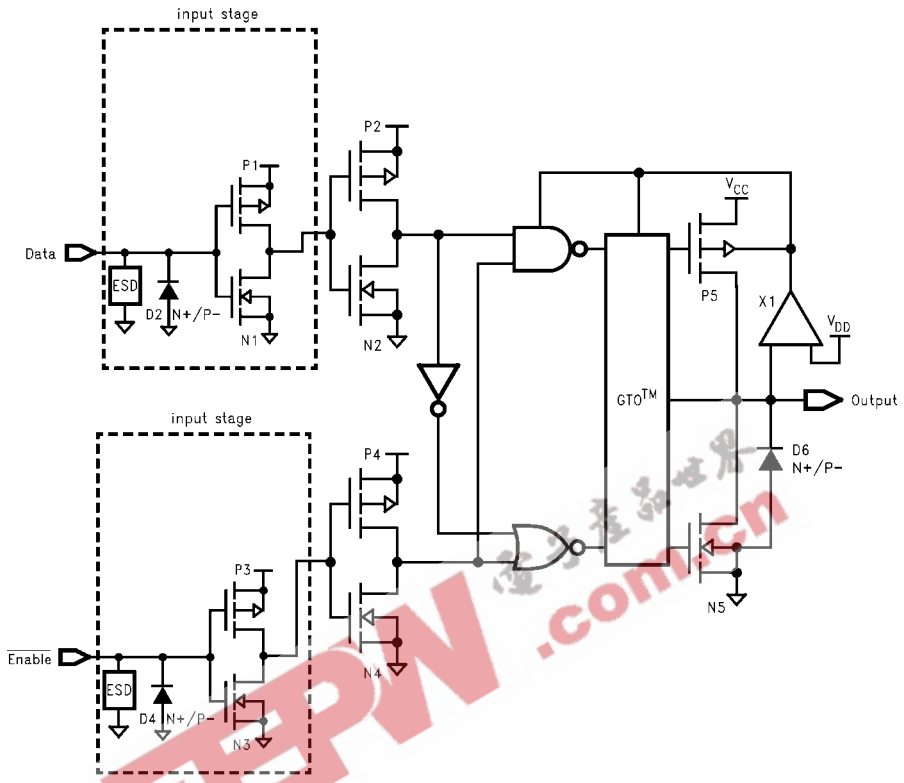


FIGURE 2. Waveforms
(Input Characteristics; $f = 1MHz, t_r = t_f = 3ns$)

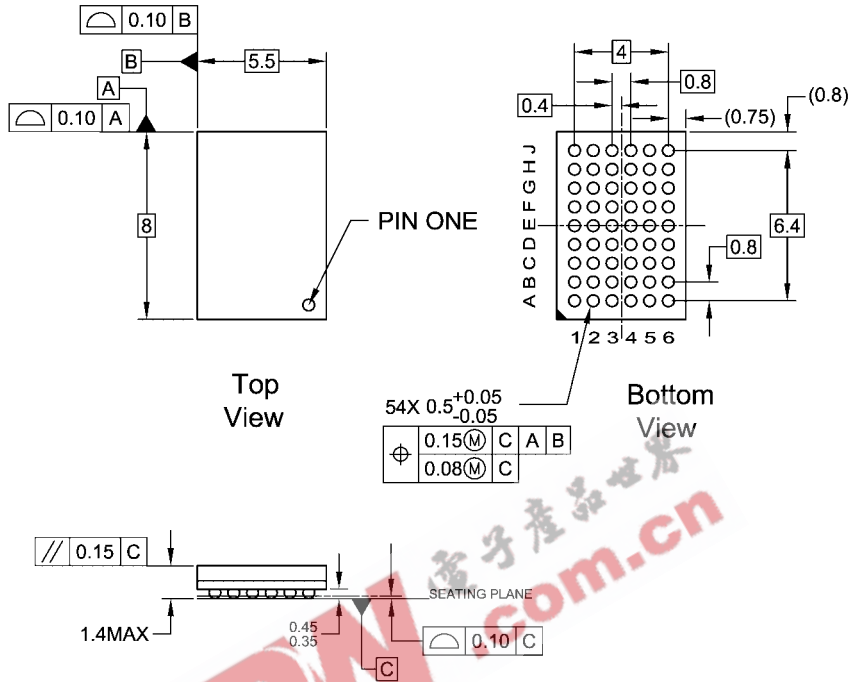
Symbol	V_{CC}		
	$3.3V \pm 0.3V$	2.7V	$2.5V \pm 0.2V$
V_{mi}	1.5V	1.5V	$V_{CC}/2$
V_{mo}	1.5V	1.5V	$V_{CC}/2$
V_x	$V_{OL} + 0.3V$	$V_{OL} + 0.3V$	$V_{OL} + 0.15V$
V_y	$V_{OH} - 0.3V$	$V_{OH} - 0.3V$	$V_{OH} - 0.15V$

Schematic Diagram Generic for LCX Family



74LCX16374

Physical Dimensions inches (millimeters) unless otherwise noted



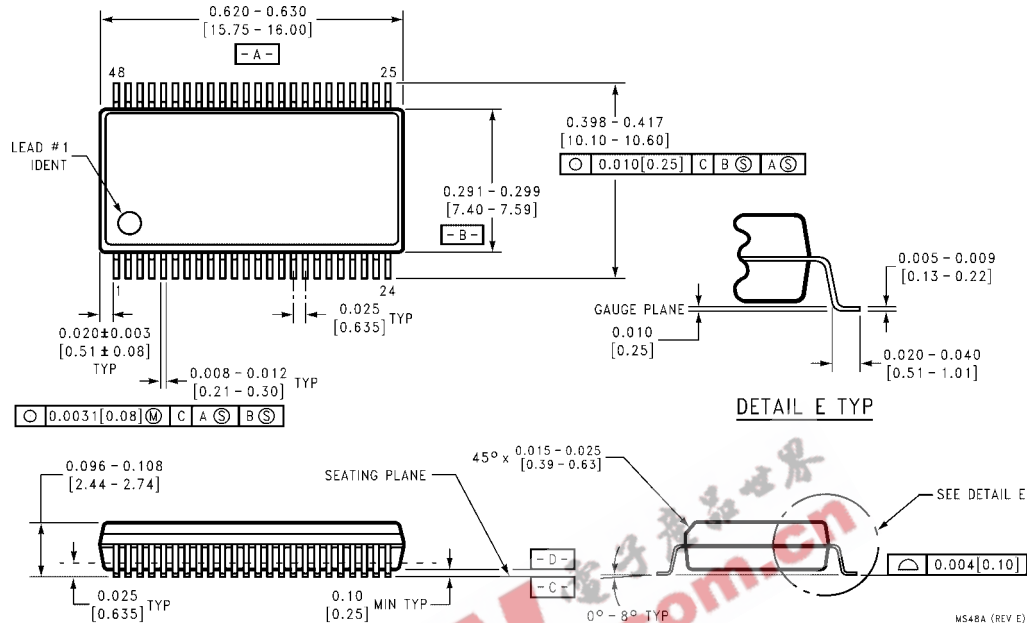
NOTES:

- A. THIS PACKAGE CONFORMS TO JEDEC M0-205
- B. ALL DIMENSIONS IN MILLIMETERS
- C. LAND PATTERN RECOMMENDATION: NSMD (Non Solder Mask Defined)
.35MM DIA PADS WITH A SOLDERMASK OPENING OF .45MM CONCENTRIC TO PADS
- D. DRAWING CONFORMS TO ASME Y14.5M-1994

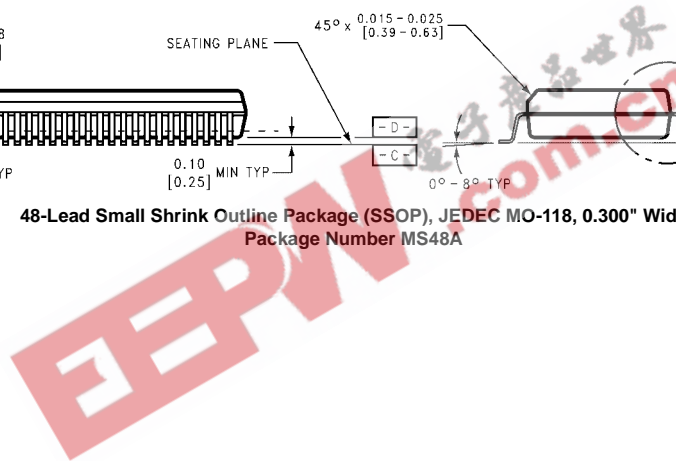
BGA54ArevD

**54-Ball Fine-Pitch Ball Grid Array (FBGA), JEDEC M0-205, 5.5mm Wide
Package Number BGA54A**

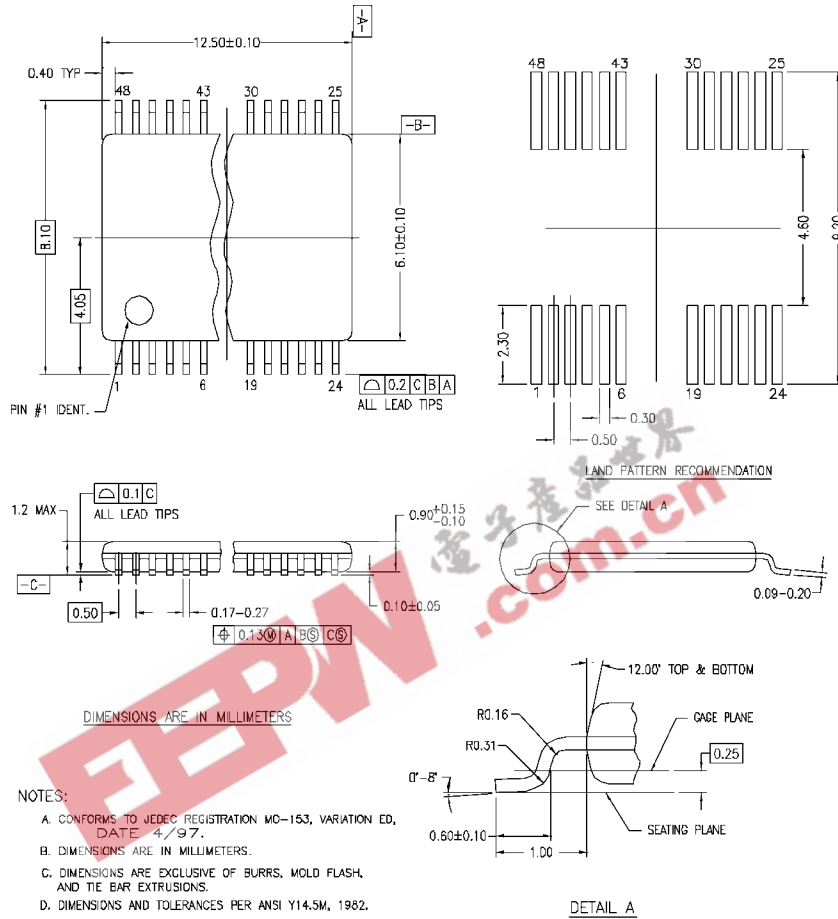
Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



48-Lead Small Shrink Outline Package (SSOP), JEDEC MO-118, 0.300" Wide
Package Number MS48A



Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



MTD48REVC

48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide Package Number MTD48

Fairchild does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied and Fairchild reserves the right at any time without notice to change said circuitry and specifications.

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

www.fairchildsemi.com