

# DATA SHEET

For a complete data sheet, please also download:

- The IC06 74HC/HCT/HCU/HCMOS Logic Family Specifications
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Information
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Outlines

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## **74HC/HCT4351** 8-channel analog multiplexer/demultiplexer with latch

Product specification  
File under Integrated Circuits, IC06

December 1990

# 8-channel analog multiplexer/demultiplexer with latch

## 74HC/HCT4351

### FEATURES

- Wide analog input voltage range:  $\pm 5\text{ V}$
- Low "ON" resistance:
  - 80  $\Omega$  (typ.) at  $V_{CC} - V_{EE} = 4.5\text{ V}$
  - 70  $\Omega$  (typ.) at  $V_{CC} - V_{EE} = 6.0\text{ V}$
  - 60  $\Omega$  (typ.) at  $V_{CC} - V_{EE} = 9.0\text{ V}$
- Logic level translation: to enable 5 V logic to communicate with  $\pm 5\text{ V}$  analog signals
- Typical "break before make" built in
- Address latches provided
- Output capability: non-standard
- I<sub>CC</sub> category: MSI

### GENERAL DESCRIPTION

The 74HC/HCT4351 are high-speed Si-gate CMOS devices. They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT4351 are 8-channel analog multiplexers/demultiplexers with three select inputs ( $S_0$  to  $S_2$ ), two enable inputs ( $\overline{E}_1$  and  $E_2$ ), a latch enable input ( $\overline{LE}$ ), eight independent inputs/outputs ( $Y_0$  to  $Y_7$ ) and a common input/output ( $Z$ ).

With  $\overline{E}_1$  LOW and  $E_2$  is HIGH, one of the eight switches is selected (low impedance ON-state) by  $S_0$  to  $S_2$ . The data at the select inputs may be latched by using the active LOW latch enable input ( $\overline{LE}$ ). When  $\overline{LE}$  is HIGH the latch is transparent. When either of the two enable inputs,  $\overline{E}_1$  (active LOW) and  $E_2$  (active HIGH), is inactive, all 8 analog switches are turned off.

$V_{CC}$  and GND are the supply voltage pins for the digital control inputs ( $S_0$  to  $S_2$ ,  $\overline{LE}$ ,  $\overline{E}_1$  and  $E_2$ ). The  $V_{CC}$  to GND ranges are 2.0 to 10.0 V for HC and 4.5 to 5.5 V for HCT. The analog inputs/outputs ( $Y_0$  to  $Y_7$ , and  $Z$ ) can swing between  $V_{CC}$  as a positive limit and  $V_{EE}$  as a negative limit.

$V_{CC} - V_{EE}$  may not exceed 10.0 V.

For operation as a digital multiplexer/demultiplexer,  $V_{EE}$  is connected to GND (typically ground).

### QUICK REFERENCE DATA

$V_{EE} = \text{GND} = 0\text{ V}$ ;  $T_{\text{amb}} = 25\text{ }^\circ\text{C}$ ;  $t_r = t_f = 6\text{ ns}$

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
$t_{PZH} / t_{PZL}$	turn "ON" time $\overline{E}_1, E_2$ or $S_n$ to $V_{os}$	$C_L = 15\text{ pF}$ ; $R_L = 1\text{ k}\Omega$ ; $V_{CC} = 5\text{ V}$	27	35	ns
$t_{PHZ} / t_{PLZ}$	turn "OFF" time $\overline{E}_1, E_2$ or $S_n$ to $V_{os}$		21	23	ns
$C_i$	input capacitance		3.5	3.5	pF
$C_{PD}$	power dissipation capacitance per switch	notes 1 and 2	25	25	pF
$C_s$	max. switch capacitance independent (Y) common (Z)		5	5	pF
			25	25	pF

### Notes

1.  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu\text{W}$ ):
 
$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum \{(C_L + C_S) \times V_{CC}^2 \times f_o\}$$
 where:
  - $f_i$  = input frequency in MHz
  - $f_o$  = output frequency in MHz
  - $C_L$  = output load capacitance in pF
  - $C_S$  = max. switch capacitance in pF
  - $\sum \{(C_L + C_S) \times V_{CC}^2 \times f_o\}$  = sum of outputs
  - $V_{CC}$  = supply voltage in V

2. For HC the condition is  $V_i = \text{GND to } V_{CC}$   
For HCT the condition is  $V_i = \text{GND to } V_{CC} - 1.5\text{ V}$

### ORDERING INFORMATION

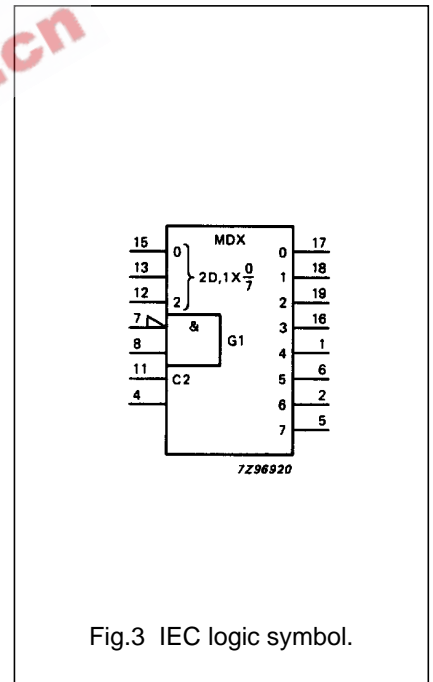
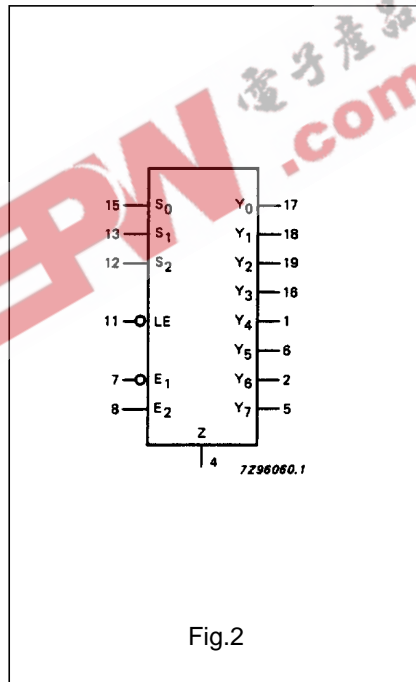
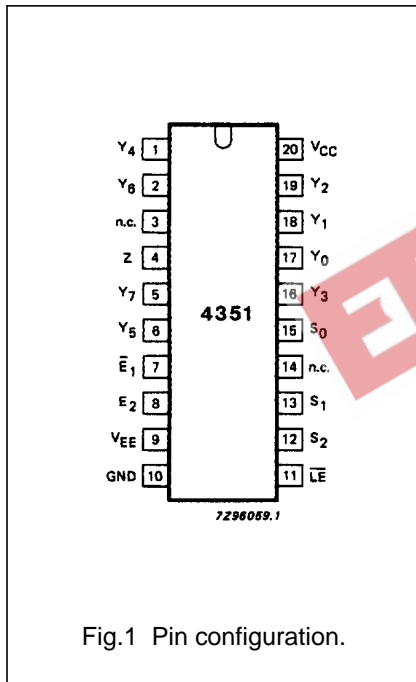
See "74HC/HCT/HCU/HCMOS Logic Package Information".

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PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
4	Z	common
3, 14	n.c.	not connected
7	$\bar{E}_1$	enable input (active LOW)
8	$E_2$	enable input (active HIGH)
9	$V_{EE}$	negative supply voltage
10	GND	ground (0 V)
11	$\bar{LE}$	latch enable input (active LOW)
15, 13, 12	$S_0$ to $S_2$	select inputs
17, 18, 19, 16, 1, 6, 2, 5	$Y_0$ to $Y_7$	independent inputs/outputs
20	$V_{CC}$	positive supply voltage



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**FUNCTION TABLE**

INPUTS						CHANNEL ON
$\bar{E}_1$	$E_2$	$\bar{LE}$	$S_2$	$S_1$	$S_0$	
H	X	X	X	X	X	none
X	L	X	X	X	X	none
L	H	H	L	L	L	$Y_0$
L	H	H	L	L	H	$Y_1$
L	H	H	L	H	L	$Y_2$
L	H	H	L	H	H	$Y_3$
L	H	H	H	L	L	$Y_4$
L	H	H	H	L	H	$Y_5$
L	H	H	H	H	L	$Y_6$
L	H	H	H	H	H	$Y_7$
L	H	L	X	X	X	(1)
X	X	↓	X	X	X	(2)

**Notes**

1. Last selected channel "ON".
2. Selected channels latched.
3. H = HIGH voltage level  
L = LOW voltage level  
X = don't care  
↓ = HIGH-to-LOW  $\bar{LE}$  transition

**APPLICATIONS**

- Analog multiplexing and demultiplexing
- Digital multiplexing and demultiplexing
- Signal gating

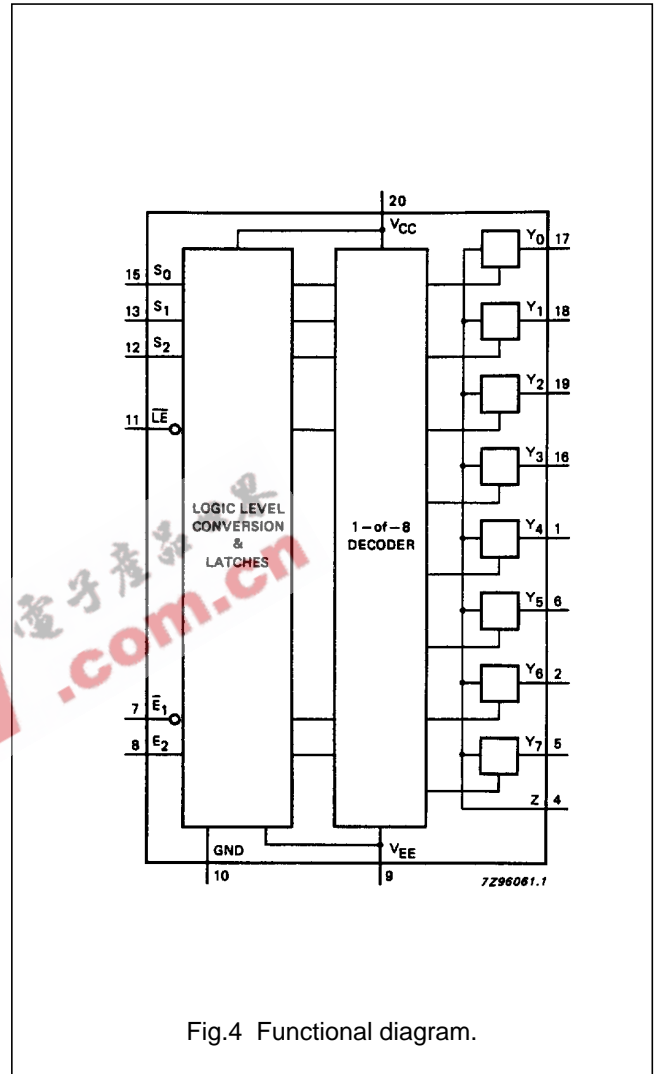


Fig.4 Functional diagram.

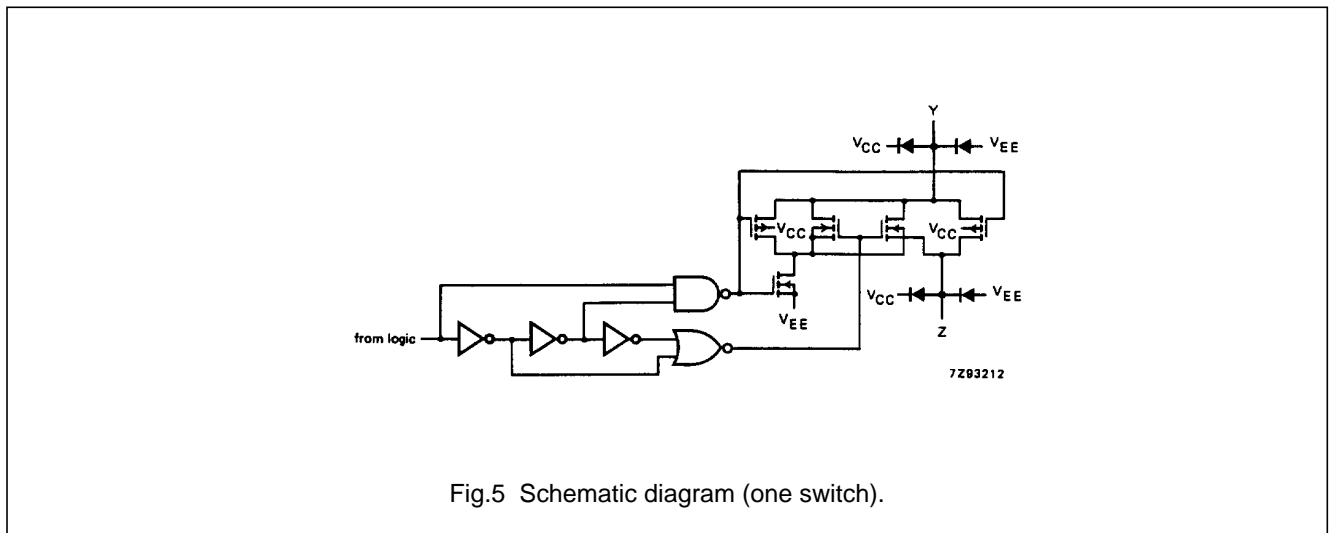


Fig.5 Schematic diagram (one switch).

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### RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltages are referenced to  $V_{EE} = \text{GND}$  (ground = 0 V)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONDITIONS
$V_{CC}$	DC supply voltage	-0.5	+11.0	V	
$\pm I_{IK}$	DC digital input diode current		20	mA	for $V_I < -0.5 \text{ V}$ or $V_I > V_{CC} + 0.5 \text{ V}$
$\pm I_{SK}$	DC switch diode current		20	mA	for $V_S < -0.5 \text{ V}$ or $V_S > V_{CC} + 0.5 \text{ V}$
$\pm I_S$	DC switch current		25	mA	for $-0.5 \text{ V} < V_S < V_{CC} + 0.5 \text{ V}$
$\pm I_{EE}$	DC $V_{EE}$ current		20	mA	
$\pm I_{CC}; \pm I_{GND}$	DC $V_{CC}$ or GND current		50	mA	
$T_{stg}$	storage temperature range	-65	+150	°C	
$P_{tot}$	power dissipation per package				for temperature range: -40 to +125 °C 74HC/HCT
	plastic DIL		750	mW	above +70 °C: derate linearly with 12 mW/K
	plastic mini-pack (SO)		500	mW	above +70 °C: derate linearly with 8 mW/K
$P_S$	power dissipation per switch		100	mW	

### Note to ratings

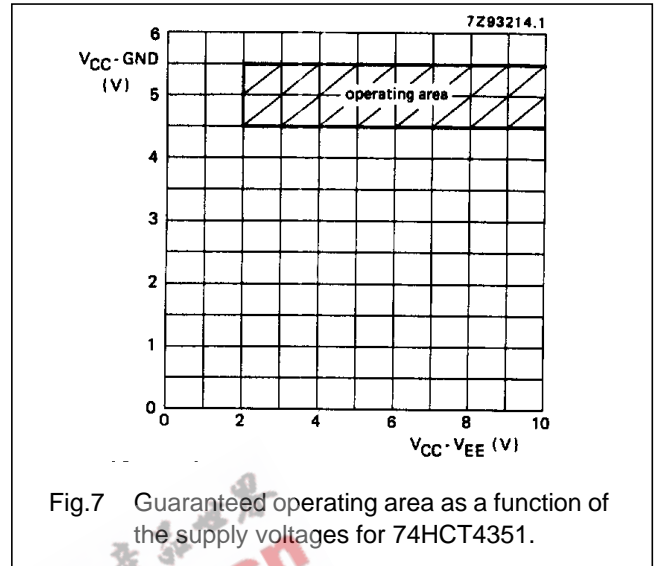
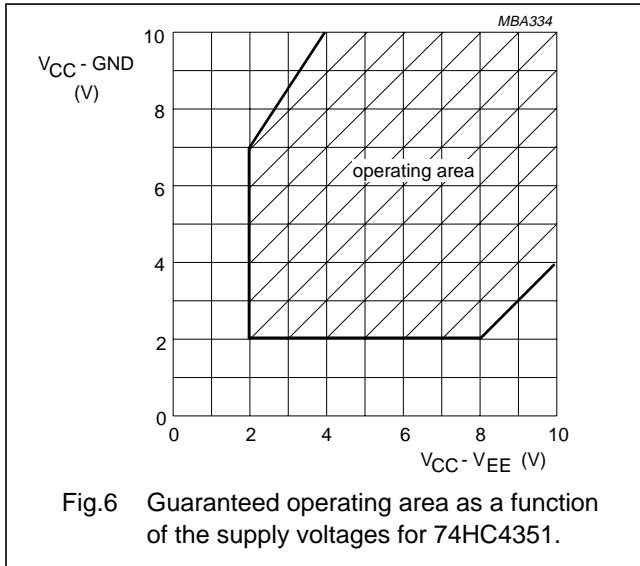
- To avoid drawing  $V_{CC}$  current out of terminal Z, when switch current flows in terminals  $Y_n$ , the voltage drop across the bidirectional switch must not exceed 0.4 V. If the switch current flows into terminal Z, no  $V_{CC}$  current will flow out of terminals  $Y_n$ . In this case there is no limit for the voltage drop across the switch, but the voltages at  $Y_n$  and Z may not exceed  $V_{CC}$  or  $V_{EE}$ .

### RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	74HC			74HCT			UNIT	CONDITIONS
		min.	typ.	max.	min.	typ.	max.		
$V_{CC}$	DC supply voltage $V_{CC}-\text{GND}$	2.0	5.0	10.0	4.5	5.0	5.5	V	see Figs 6 and 7
$V_{CC}$	DC supply voltage $V_{CC}-V_{EE}$	2.0	5.0	10.0	2.0	5.0	10.0	V	see Figs 6 and 7
$V_I$	DC input voltage range	GND		$V_{CC}$	GND		$V_{CC}$	V	
$V_S$	DC switch voltage range	$V_{EE}$		$V_{CC}$	$V_{EE}$		$V_{CC}$	V	
$T_{amb}$	operating ambient temperature range	-40		+85	-40		+85	°C	see DC and AC CHARACTERISTICS
$T_{amb}$	operating ambient temperature range	-40		+125	-40		+125	°C	
$t_r, t_f$	input rise and fall times		6.0	1000 500 400 250		6.0	500	ns	$V_{CC} = 2.0 \text{ V}$ $V_{CC} = 4.5 \text{ V}$ $V_{CC} = 6.0 \text{ V}$ $V_{CC} = 10.0 \text{ V}$

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DC CHARACTERISTICS FOR 74HC/HCT

For 74HC:  $V_{CC} - GND$  or  $V_{CC} - V_{EE} = 2.0, 4.5, 6.0$  and  $9.0$  V

For 74HCT:  $V_{CC} - GND = 4.5$  and  $5.5$  V;  $V_{CC} - V_{EE} = 2.0, 4.5, 6.0$  and  $9.0$  V

SYMBOL	PARAMETER	$T_{amb} (°C)$						UNIT	TEST CONDITIONS					
		74HC/HCT							$V_{CC}$ (V)	$V_{EE}$ (V)	$I_S$ ( $\mu A$ )	$V_{is}$	$V_I$	
		+25			-40 to +85		-40 to +125							
		min.	typ.	max.	min.	max.	min.							max.
$R_{ON}$	ON resistance (rail)	-	-	-	-	-	-	$\Omega$	2.0	0	100	$V_{CC}$ to $V_{EE}$	$V_{IN}$ or $V_{IL}$	
		100	180	225	270	$\Omega$	4.5	0	1000					
		90	160	200	240	$\Omega$	6.0	0	1000					
		70	130	165	195	$\Omega$	4.5	-4.5	1000					
$R_{ON}$	ON resistance (rail)	150	-	-	-	-	$\Omega$	2.0	0	100	$V_{EE}$	$V_{IH}$ or $V_{IL}$		
		80	140	175	210	$\Omega$	4.5	0	1000					
		70	120	150	180	$\Omega$	6.0	0	1000					
		60	105	130	160	$\Omega$	4.5	-4.5	1000					
$R_{ON}$	ON resistance (rail)	150	-	-	-	-	$\Omega$	2.0	0	100	$V_{CC}$	$V_{IH}$ or $V_{IL}$		
		90	160	200	240	$\Omega$	4.5	0	1000					
		80	140	175	210	$\Omega$	6.0	0	1000					
		65	120	150	180	$\Omega$	4.5	-4.5	1000					
$\Delta R_{ON}$	maximum $\Delta$ ON resistance between any two channels	-	-	-	-	-	$\Omega$	2.0	0	-	$V_{CC}$ to $V_{EE}$	$V_{IH}$ or $V_{IL}$		
		9	-	-	-	$\Omega$	4.5	0	-					
		8	-	-	-	$\Omega$	6.0	0	-					
		6	-	-	-	$\Omega$	4.5	-4.5	-					

Notes to DC characteristics

- At supply voltages ( $V_{CC} - V_{EE}$ ) approaching 2.0 V, the analog switch ON-resistance becomes extremely non-linear. There it is recommended that these devices be used to transmit digital signals only, when using these supply voltages.
- For test circuit measuring  $R_{ON}$  see Fig.8.

## 8-channel analog multiplexer/demultiplexer with latch

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### DC CHARACTERISTICS FOR 74HC

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)							UNIT	TEST CONDITIONS			
		74HC								V <sub>CC</sub> (V)	V <sub>EE</sub> (V)	V <sub>I</sub>	OTHER
		+25			-40 to +85		-40 to +125						
		min.	typ.	max.	min.	max.	min.	max.					
V <sub>IH</sub>	HIGH level input voltage	1.5	1.2		1.5		1.5		V	2.0			
		3.15	2.4		3.15		3.15			4.5			
		4.2	3.2		4.2		4.2			6.0			
		6.3	4.7		6.3		6.3			9.0			
V <sub>IL</sub>	LOW level input voltage		0.8	0.5		0.5		0.5	V	2.0			
			2.1	1.35		1.35		1.35		4.5			
			2.8	1.8		1.8		1.8		6.0			
			4.3	2.7		2.7		2.7		9.0			
±I <sub>I</sub>	input leakage current			0.1		1.0		1.0	μA	6.0	0	V <sub>CC</sub> or GND	
				0.2		2.0		2.0		10.0	0		
±I <sub>S</sub>	analog switch OFF-state current per channel			0.1		1.0		1.0	μA	10.0	0	V <sub>IH</sub> or V <sub>IL</sub>	M <sub>S</sub> I = V <sub>CC</sub> - V <sub>EE</sub> (see Fig.10)
±I <sub>S</sub>	analog switch OFF-state current all channels			0.4		4.0		4.0	μA	10.0	0	V <sub>IH</sub> or V <sub>IL</sub>	M <sub>S</sub> I = V <sub>CC</sub> - V <sub>EE</sub> (see Fig.10)
±I <sub>S</sub>	analog switch ON-state current			0.4		4.0		4.0	μA	10.0	0	V <sub>IH</sub> or V <sub>IL</sub>	M <sub>S</sub> I = V <sub>CC</sub> - V <sub>EE</sub> (see Fig.11)
I <sub>CC</sub>	quiescent supply current			8.0		80.0		160.0	μA	6.0	0	V <sub>CC</sub> or GND	V <sub>IS</sub> = V <sub>EE</sub> or V <sub>CC</sub> ; V <sub>OS</sub> = V <sub>CC</sub> or V <sub>EE</sub>
				16.0		160.0		320.0		10.0	0		

## 8-channel analog multiplexer/demultiplexer with latch

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### AC CHARACTERISTICS FOR 74HC

GND = 0 V;  $t_r = t_f = 6$  ns;  $C_L = 50$  pF

SYMBOL	PARAMETER	$T_{amb}$ (°C)							UNIT	TEST CONDITIONS		
		74HC								$V_{CC}$ (V)	$V_{EE}$ (V)	OTHER
		+25			-40 to +85		-40 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
$t_{PHL}/t_{PLH}$	propagation delay $V_{is}$ to $V_{os}$		14	60		75		90	ns	2.0	0	$R_L = \infty$ ; $C_L = 50$ pF (see Fig.17)
			5	12		15		18		4.5	0	
			4	10		13		15		6.0	0	
			4	8		10		12		4.5	-4.5	
$t_{PZH}/t_{PZL}$	turn "ON" time $\bar{E}_1$ to $V_{os}$		85	300		375		450	ns	2.0	0	$R_L = 1$ k $\Omega$ ; $C_L = 50$ pF (see Fig.18)
			31	60		75		90		4.5	0	
			25	51		64		77		6.0	0	
			28	55		69		83		4.5	-4.5	
$t_{PZH}/t_{PZL}$	turn "ON" time $E_2$ to $V_{os}$		85	300		375		450	ns	2.0	0	$R_L = 1$ k $\Omega$ ; $C_L = 50$ pF (see Fig.18)
			31	60		75		90		4.5	0	
			25	51		64		77		6.0	0	
			25	55		69		83		4.5	-4.5	
$t_{PZH}/t_{PZL}$	turn "ON" time $\bar{LE}$ to $V_{os}$		91	300		375		450	ns	2.0	0	$R_L = 1$ k $\Omega$ ; $C_L = 50$ pF (see Fig.18)
			33	60		75		90		4.5	0	
			26	51		64		77		6.0	0	
			27	55		69		83		4.5	-4.5	
$t_{PZH}/t_{PZL}$	turn "ON" time $S_n$ to $V_{os}$		88	300		375		450	ns	2.0	0	$R_L = 1$ k $\Omega$ ; $C_L = 50$ pF (see Fig.18)
			32	60		75		90		4.5	0	
			26	51		64		77		6.0	0	
			25	50		63		75		4.5	-4.5	
$t_{PHZ}/t_{PLZ}$	turn "OFF" time $\bar{E}_1$ to $V_{os}$		69	250		315		375	ns	2.0	0	$R_L = 1$ k $\Omega$ ; $C_L = 50$ pF (see Fig.18)
			25	50		63		75		4.5	0	
			20	43		54		64		6.0	0	
			20	40		50		60		4.5	-4.5	
$t_{PHZ}/t_{PLZ}$	turn "OFF" time $E_2$ to $V_{os}$		72	250		315		375	ns	2.0	0	$R_L = 1$ k $\Omega$ ; $C_L = 50$ pF (see Fig.18)
			26	50		63		75		4.5	0	
			21	43		54		64		6.0	0	
			19	40		50		60		4.5	-4.5	
$t_{PHZ}/t_{PLZ}$	turn "OFF" time $\bar{LE}$ to $V_{os}$		83	275		345		415	ns	2.0	0	$R_L = 1$ k $\Omega$ ; $C_L = 50$ pF (see Fig.18)
			30	55		69		83		4.5	0	
			24	47		59		71		6.0	0	
			26	45		56		68		4.5	-4.5	
$t_{PHZ}/t_{PLZ}$	turn "OFF" time $S_n$ to $V_{os}$		80	275		345		415	ns	2.0	0	$R_L = 1$ k $\Omega$ ; $C_L = 50$ pF (see Fig.18)
			29	55		69		83		4.5	0	
			23	47		59		71		6.0	0	
			24	48		60		72		4.5	-4.5	



8-channel analog multiplexer/demultiplexer  
with latch

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SYMBOL	PARAMETER	T <sub>amb</sub> (°C)							UNIT	TEST CONDITIONS		
		74HC								V <sub>CC</sub> (V)	V <sub>EE</sub> (V)	OTHER
		+25			-40 to +85		-40 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
t <sub>su</sub>	set-up time S <sub>n</sub> to $\overline{\text{LE}}$	60	17			75		90	ns	2.0	0	R <sub>L</sub> = 1 kΩ; C <sub>L</sub> = 50 pF (see Fig.19)
		12	6			15		18		4.5	0	
		10	5			13		15		6.0	0	
		18	9			23		27		4.5	-4.5	
t <sub>h</sub>	hold time S <sub>n</sub> to $\overline{\text{LE}}$	5	-8			5		5	ns	2.0	0	R <sub>L</sub> = 1 kΩ; C <sub>L</sub> = 50 pF (see Fig.19)
		5	-3			5		5		4.5	0	
		5	-2			5		5		6.0	0	
		5	-4			5		5		4.5	-4.5	
t <sub>w</sub>	$\overline{\text{LE}}$ minimum pulse width HIGH	100	11			125		150	ns	2.0	0	R <sub>L</sub> = 1 kΩ; C <sub>L</sub> = 50 pF (see Fig.19)
		20	1			25		30		4.5	0	
		17	3			21		26		6.0	0	
		25	7			31		38		4.5	-4.5	

# 8-channel analog multiplexer/demultiplexer with latch

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## DC CHARACTERISTICS FOR 74HCT

Voltages are referenced to GND (ground = 0)

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS				
		74HCT							V <sub>CC</sub> (V)	V <sub>EE</sub> (V)	V <sub>I</sub>	OTHER	
		+25			-40 to +85		-40 to +125						
		min.	typ.	max.	min.	max.	min.						max.
V <sub>IH</sub>	HIGH level input voltage	2.0	1.6		2.0		2.0		V	4.5 to 5.5			
V <sub>IL</sub>	LOW level input voltage		1.2	0.8		0.8		0.8	V	4.5 to 5.5			
±I <sub>I</sub>	input leakage current			0.1		1.0		1.0	μA	5.5	0	V <sub>CC</sub> or GND	
±I <sub>S</sub>	analog switch OFF-state current per channel			0.1		1.0		1.0	μA	10.0	0	V <sub>IH</sub> or V <sub>IL</sub>	V <sub>S</sub>  = V <sub>CC</sub> - V <sub>EE</sub> (see Fig.10)
±I <sub>S</sub>	analog switch OFF-state current all channels			0.4		4.0		4.0	μA	10.0	0	V <sub>IH</sub> or V <sub>IL</sub>	V <sub>S</sub>  = V <sub>CC</sub> - V <sub>EE</sub> (see Fig.10)
±I <sub>S</sub>	analog switch ON-state current			0.4		4.0		4.0	μA	10.0	0	V <sub>IH</sub> or V <sub>IL</sub>	V <sub>S</sub>  = V <sub>CC</sub> - V <sub>EE</sub> (see Fig.11)
I <sub>CC</sub>	quiescent supply current			8.0 16.0		80.0 160.0		160.0 320.0	μA	5.5 5.0	0 -5.0	V <sub>CC</sub> or GND	V <sub>is</sub> = V <sub>EE</sub> or V <sub>CC</sub> ; V <sub>os</sub> = V <sub>CC</sub> or V <sub>EE</sub>
ΔI <sub>CC</sub>	additional quiescent supply current per input pin for unit load coefficient is 1 (note 1)		100	360		450		490	μA	4.5 to 5.5	0	V <sub>CC</sub> -2.1 V	other inputs at V <sub>CC</sub> or GND

### Note to HCT types

- The value of additional quiescent supply current (ΔI<sub>CC</sub>) for a unit load of 1 is given here. To determine ΔI<sub>CC</sub> per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
$\overline{E}_1, E_2$	0.50
$\overline{S}_n$	0.50
$\overline{LE}$	1.5

## 8-channel analog multiplexer/demultiplexer with latch

74HC/HCT4351

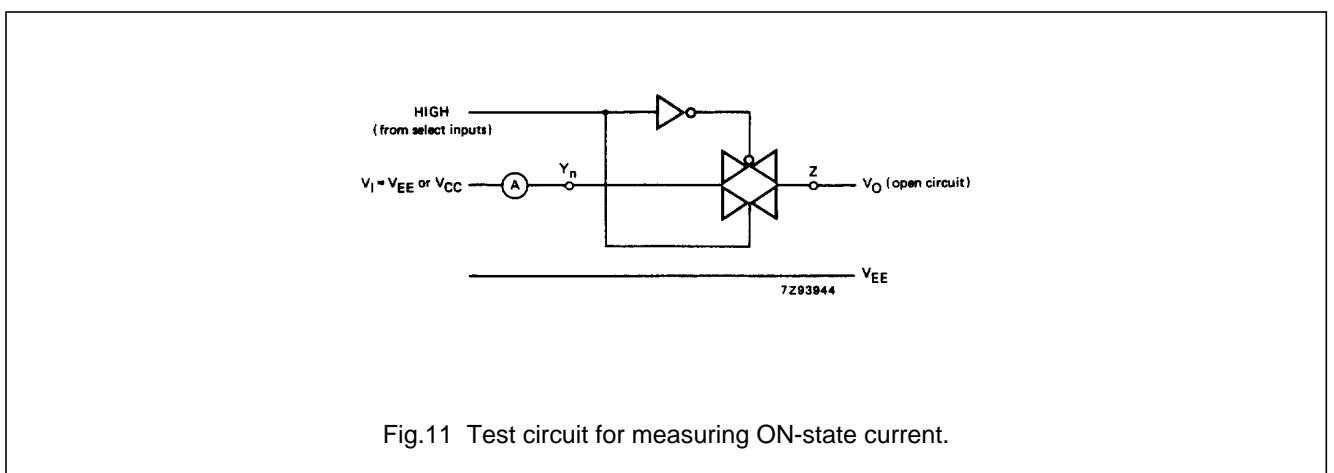
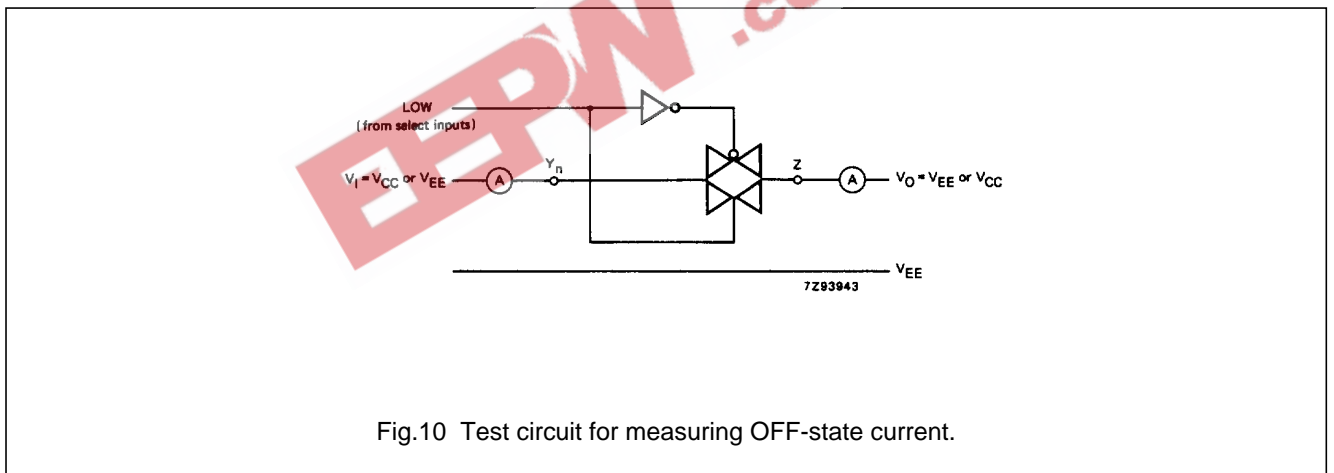
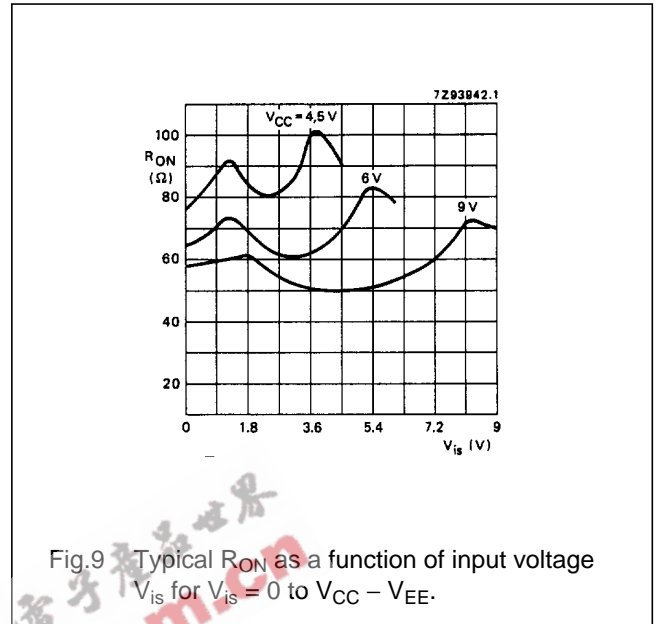
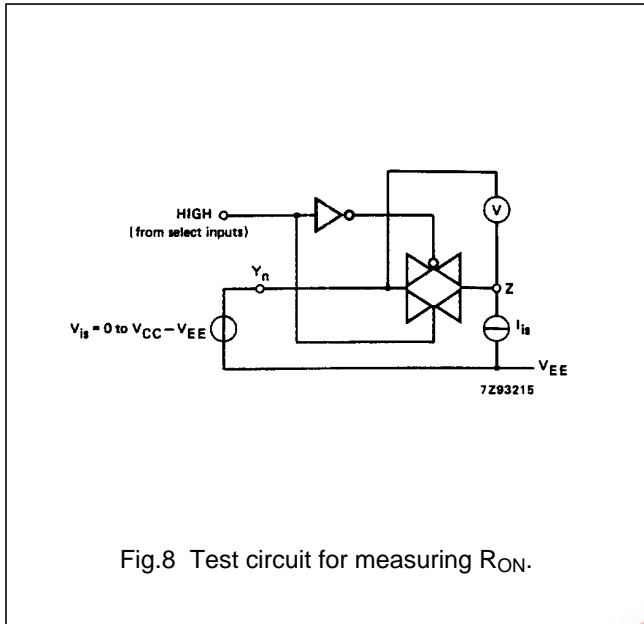
### AC CHARACTERISTICS FOR 74HCT

GND = 0 V;  $t_r = t_f = 6$  ns;  $C_L = 50$  pF

SYMBOL	PARAMETER	$T_{amb}$ (°C)							UNIT	TEST CONDITIONS		
		74HCT								$V_{CC}$ (V)	$V_{EE}$ (V)	OTHER
		+25			-40 to +85		-40 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
$t_{PHL}/t_{PLH}$	propagation delay $V_{is}$ to $V_{os}$		6 4	12 8		15 10		18 12	ns	4.5 4.5	0 -4.5	$R_L = \infty$ ; $C_L = 50$ pF (see Fig.17)
$t_{PZH}/t_{PZL}$	turn "ON" time $\overline{E}_1$ to $V_{os}$		40 31	75 60		94 75		113 90	ns	4.5 4.5	0 -4.5	$R_L = 1$ k $\Omega$ ; $C_L = 50$ pF (see Fig.18)
$t_{PZH}/t_{PZL}$	turn "ON" time $E_2$ to $V_{os}$		35 26	70 50		88 63		105 75	ns	4.5 4.5	0 -4.5	$R_L = 1$ k $\Omega$ ; $C_L = 50$ pF (see Fig.18)
$t_{PZH}/t_{PZL}$	turn "ON" time $\overline{LE}$ to $V_{os}$		42 37	75 60		94 75		113 90	ns	4.5 4.5	0 -4.5	$R_L = 1$ k $\Omega$ ; $C_L = 50$ pF (see Fig.18)
$t_{PZH}/t_{PZL}$	turn "ON" time $S_n$ to $V_{os}$		39 30	75 60		94 75		113 90	ns	4.5 4.5	0 -4.5	$R_L = 1$ k $\Omega$ ; $C_L = 50$ pF (see Fig.18)
$t_{PHZ}/t_{PLZ}$	turn "OFF" time $\overline{E}_1$ to $V_{os}$		27 20	55 40		69 50		83 60	ns	4.5 4.5	0 -4.5	$R_L = 1$ k $\Omega$ ; $C_L = 50$ pF (see Fig.18)
$t_{PHZ}/t_{PLZ}$	turn "OFF" time $E_2$ to $V_{os}$		32 26	60 50		75 63		90 75	ns	4.5 4.5	0 -4.5	$R_L = 1$ k $\Omega$ ; $C_L = 50$ pF (see Fig.18)
$t_{PHZ}/t_{PLZ}$	turn "OFF" time $\overline{LE}$ to $V_{os}$		33 30	60 55		75 69		90 83	ns	4.5 4.5	0 -4.5	$R_L = 1$ k $\Omega$ ; $C_L = 50$ pF (see Fig.18)
$t_{PHZ}/t_{PLZ}$	turn "OFF" time $S_n$ to $V_{os}$		33 29	65 55		81 69		98 83	ns	4.5 4.5	0 -4.5	$R_L = 1$ k $\Omega$ ; $C_L = 50$ pF (see Fig.18)
$t_{su}$	set-up time $S_n$ to $\overline{LE}$	12 14	6 7			15 18		18 21	ns	4.5 4.5	0 -4.5	$R_L = 1$ k $\Omega$ ; $C_L = 50$ pF (see Fig.19)
$t_h$	hold time $S_n$ to $\overline{LE}$	5 5	-1 -2			5 5		5 5	ns	4.5 4.5	0 -4.5	$R_L = 1$ k $\Omega$ ; $C_L = 50$ pF (see Fig.19)
$t_w$	$\overline{LE}$ minimum pulse width HIGH	25 25	13 13			31 31		38 38	ns	4.5 4.5	0 -4.5	$R_L = 1$ k $\Omega$ ; $C_L = 50$ pF (see Fig.19)

8-channel analog multiplexer/demultiplexer with latch

74HC/HCT4351



# 8-channel analog multiplexer/demultiplexer with latch

74HC/HCT4351

## ADDITIONAL AC CHARACTERISTICS FOR 74HC/HCT

### Recommended conditions and typical values

GND = 0 V; T<sub>amb</sub> = 25 °C

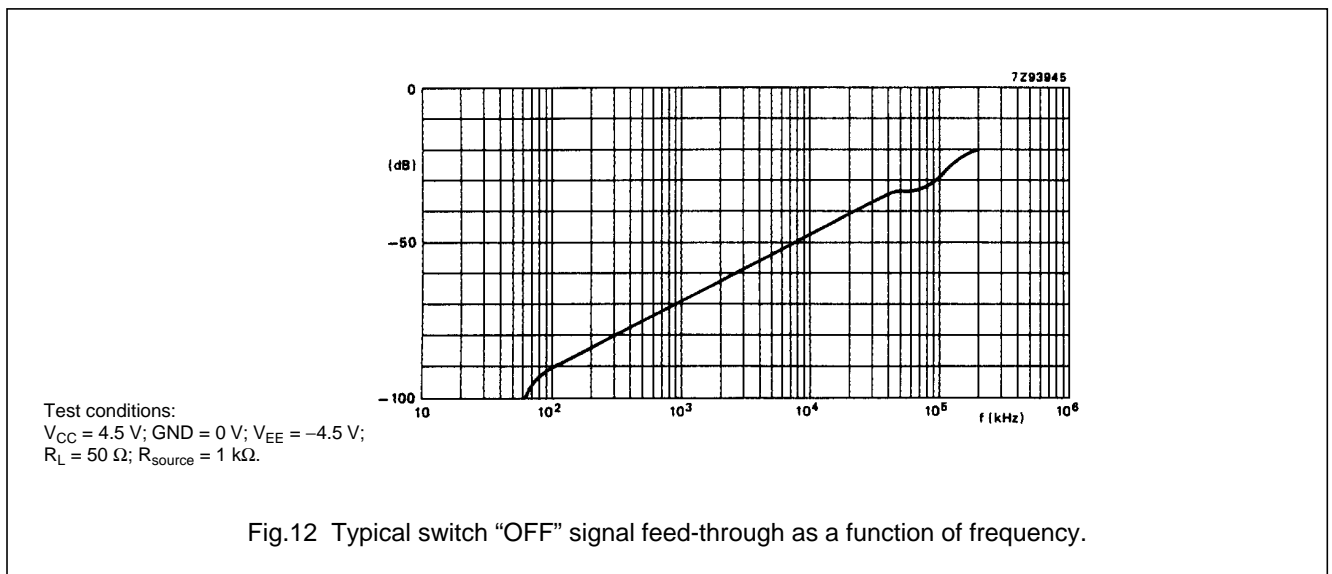
SYMBOL	PARAMETER	typ.	UNIT	V <sub>CC</sub> (V)	V <sub>EE</sub> (V)	V <sub>is(p-p)</sub> (V)	CONDITIONS
	sine-wave distortion f = 1 kHz	0.04 0.02	% %	2.25 4.5	-2.25 -4.5	4.0 8.0	R <sub>L</sub> = 10 kΩ; C <sub>L</sub> = 50 pF (see Fig.14)
	sine-wave distortion f = 10 kHz	0.12 0.06	% %	2.25 4.5	-2.25 -4.5	4.0 8.0	R <sub>L</sub> = 10 kΩ; C <sub>L</sub> = 50 pF (see Fig.14)
	switch "OFF" signal feed-through	-50 -50	dB dB	2.25 4.5	-2.25 -4.5	note 1	R <sub>L</sub> = 600 Ω; C <sub>L</sub> = 50 pF (see Figs 12 and 15)
V <sub>(p-p)</sub>	crosstalk voltage between control and any switch (peak-to-peak value)	120 220	mV mV	4.5 4.5	0 -4.5		R <sub>L</sub> = 600 Ω; C <sub>L</sub> = 50 pF; f = 1 MHz (E <sub>1</sub> , E <sub>2</sub> or S <sub>n</sub> , square-wave between V <sub>CC</sub> and GND, t <sub>r</sub> = t <sub>f</sub> = 6 ns) (see Fig.16)
f <sub>max</sub>	minimum frequency response (-3dB)	160 170	MHz MHz	2.25 4.5	-2.25 -4.5	note 2	R <sub>L</sub> = 50 Ω; C <sub>L</sub> = 10 pF (see Figs 13 and 14)
C <sub>S</sub>	maximum switch capacitance independent (Y) common (Z)	5 25	pF pF				

### Notes to AC characteristics

1. Adjust input voltage V<sub>is</sub> to 0 dBm level (0 dBm = 1 mW into 600 Ω).
2. Adjust input voltage V<sub>is</sub> to 0 dBm level at V<sub>os</sub> for 1 MHz (0 dBm = 1 mW into 50 Ω).

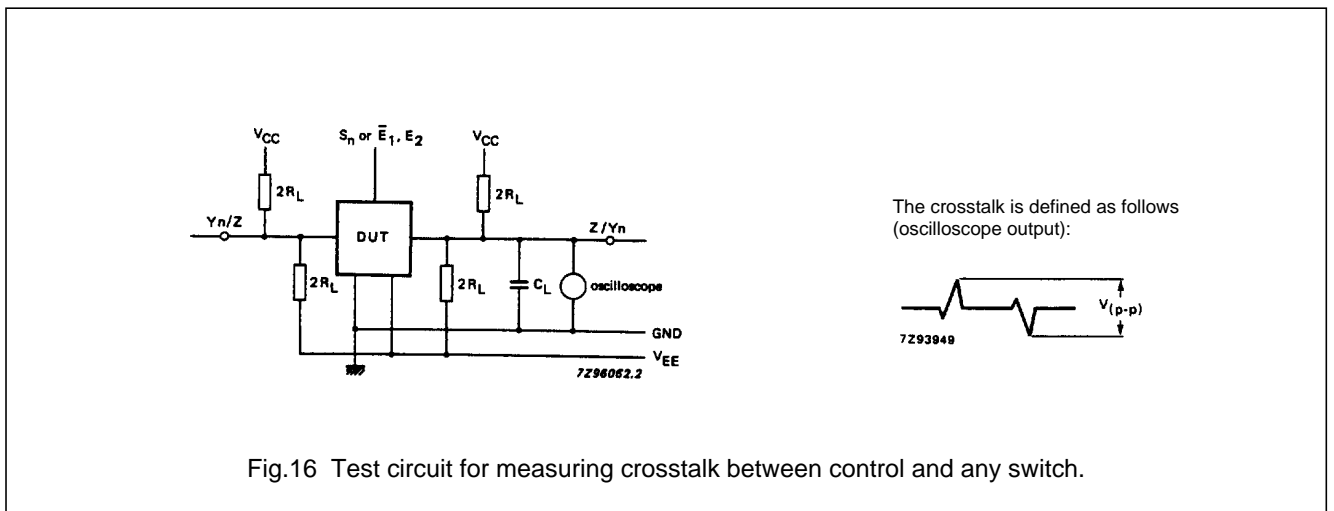
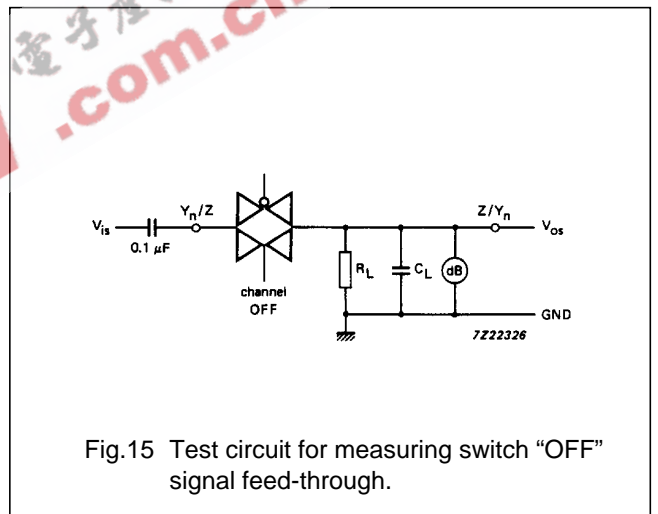
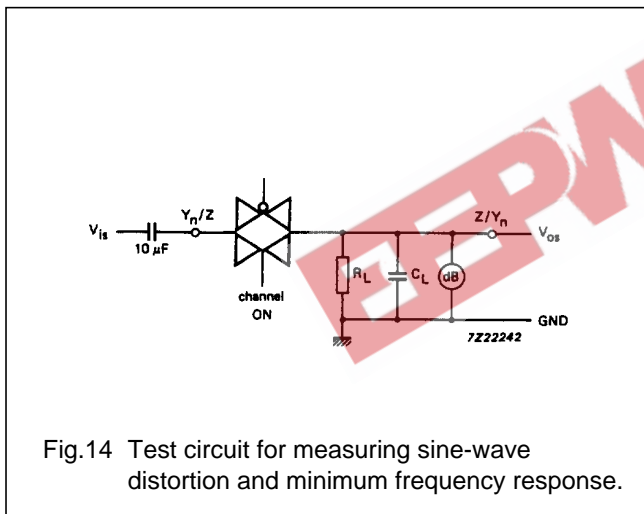
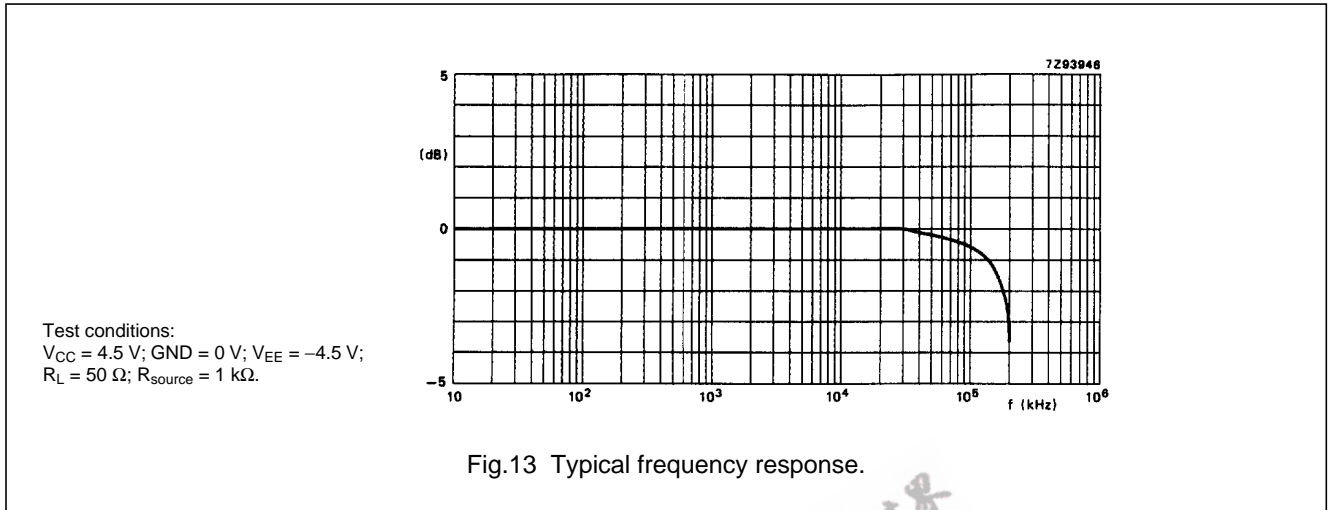
V<sub>is</sub> is the input voltage at a Y<sub>n</sub> or Z terminal, whichever is assigned as an input.

V<sub>os</sub> is the output voltage at a Y<sub>n</sub> or Z terminal, whichever is assigned as an output.



# 8-channel analog multiplexer/demultiplexer with latch

74HC/HCT4351



8-channel analog multiplexer/demultiplexer with latch

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AC WAVEFORMS

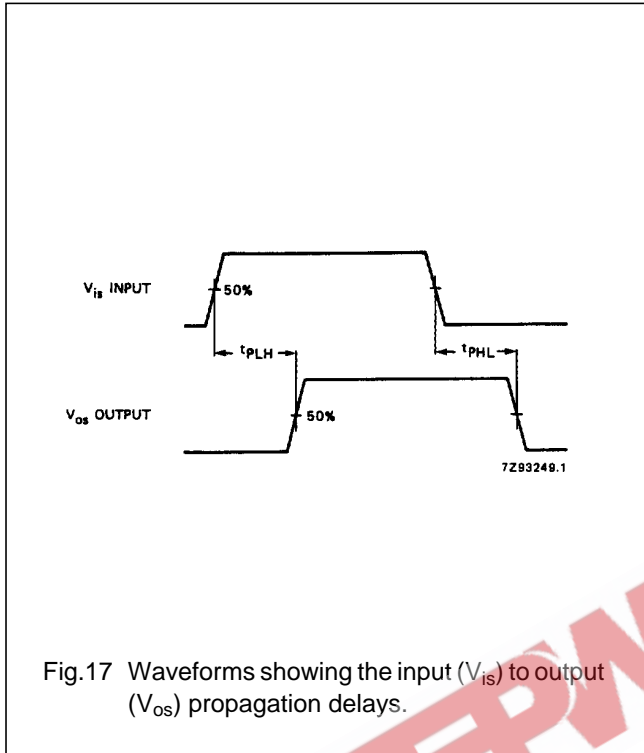
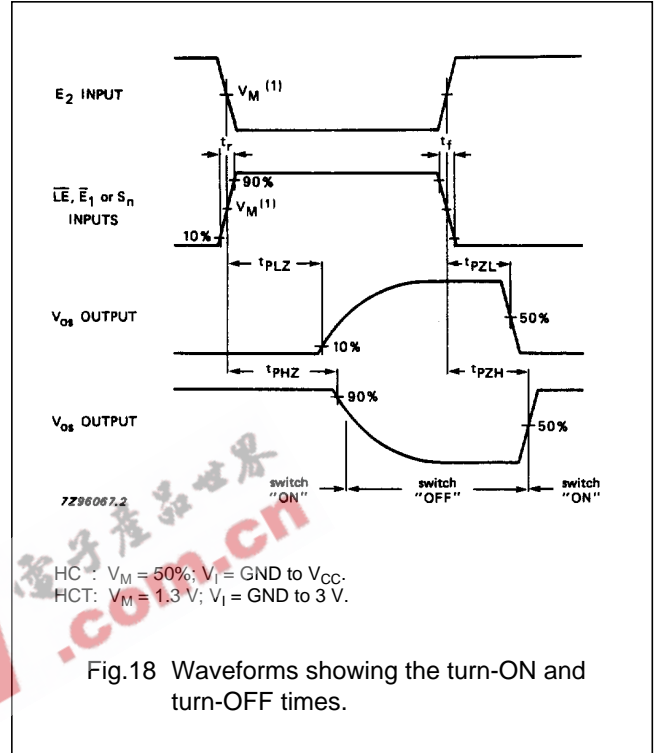
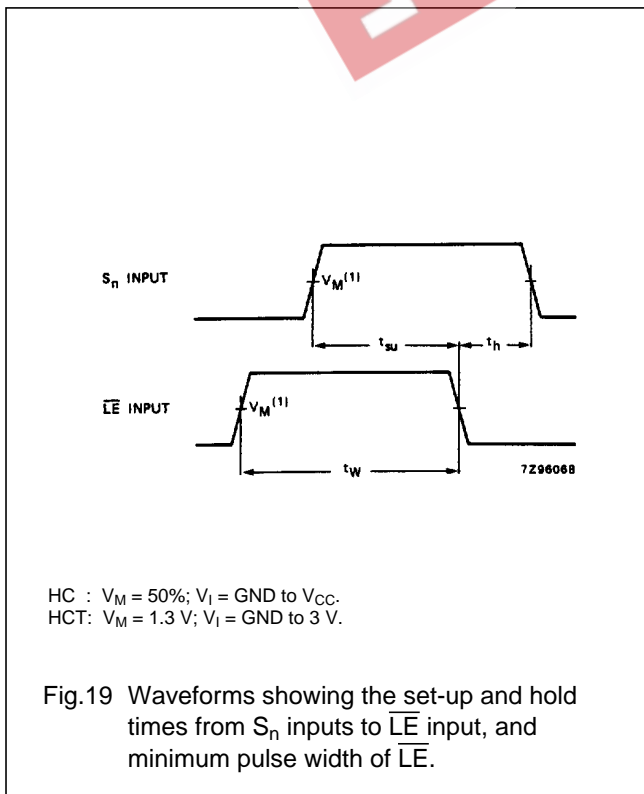


Fig.17 Waveforms showing the input ( $V_{is}$ ) to output ( $V_{os}$ ) propagation delays.



HC :  $V_M = 50\%$ ;  $V_I = \text{GND to } V_{CC}$ .  
 HCT:  $V_M = 1.3 \text{ V}$ ;  $V_I = \text{GND to } 3 \text{ V}$ .

Fig.18 Waveforms showing the turn-ON and turn-OFF times.



HC :  $V_M = 50\%$ ;  $V_I = \text{GND to } V_{CC}$ .  
 HCT:  $V_M = 1.3 \text{ V}$ ;  $V_I = \text{GND to } 3 \text{ V}$ .

Fig.19 Waveforms showing the set-up and hold times from  $S_n$  inputs to  $\overline{LE}$  input, and minimum pulse width of  $\overline{LE}$ .

# 8-channel analog multiplexer/demultiplexer with latch

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## TEST CIRCUIT AND WAVEFORMS

7293951

**Conditions**

TEST	SWITCH	V <sub>is</sub>
t <sub>PZH</sub>	V <sub>EE</sub>	V <sub>CC</sub>
t <sub>PZL</sub>	V <sub>CC</sub>	V <sub>EE</sub>
t <sub>PHZ</sub>	V <sub>EE</sub>	V <sub>CC</sub>
t <sub>PLZ</sub>	V <sub>CC</sub>	V <sub>EE</sub>
others	open	pulse

FAMILY	AMPLITUDE	V <sub>M</sub>	t <sub>r</sub> ; t <sub>f</sub>	
			f <sub>max</sub> ; PULSE WIDTH	OTHER
74HC	V <sub>CC</sub>	50%	< 2 ns	6 ns
74HCT	3.0 V	1.3 V	< 2 ns	6 ns

C<sub>L</sub> = load capacitance including jig and probe capacitance (see AC CHARACTERISTICS for values).  
 R<sub>T</sub> = termination resistance should be equal to the output impedance Z<sub>O</sub> of the pulse generator.  
 t<sub>r</sub> = t<sub>f</sub> = 6 ns; when measuring f<sub>max</sub>, there is no constraint on t<sub>r</sub>, t<sub>f</sub> with 50% duty factor.

Fig.20 Test circuit for measuring AC performance.

7287478.3

**Conditions**

TEST	SWITCH	V <sub>is</sub>
t <sub>PZH</sub>	V <sub>EE</sub>	V <sub>CC</sub>
t <sub>PZL</sub>	V <sub>CC</sub>	V <sub>EE</sub>
t <sub>PHZ</sub>	V <sub>EE</sub>	V <sub>CC</sub>
t <sub>PLZ</sub>	V <sub>CC</sub>	V <sub>EE</sub>
others	open	pulse

FAMILY	AMPLITUDE	V <sub>M</sub>	t <sub>r</sub> ; t <sub>f</sub>	
			f <sub>max</sub> ; PULSE WIDTH	OTHER
74HC	V <sub>CC</sub>	50%	< 2 ns	6 ns
74HCT	3.0 V	1.3 V	< 2 ns	6 ns

C<sub>L</sub> = load capacitance including jig and probe capacitance (see AC CHARACTERISTICS for values).  
 R<sub>T</sub> = termination resistance should be equal to the output impedance Z<sub>O</sub> of the pulse generator.  
 t<sub>r</sub> = t<sub>f</sub> = 6 ns; when measuring f<sub>max</sub>, there is no constraint on t<sub>r</sub>, t<sub>f</sub> with 50% duty factor.

Fig.21 Input pulse definitions.



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8-channel analog multiplexer/demultiplexer  
with latch

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74HC/HCT4351

**PACKAGE OUTLINES**

See *"74HC/HCT/HCU/HCMOS Logic Package Outlines"*.

