FAIRCHILD SEMICONDUCTOR™

June 1988
Revised October 1998

74ACT323
8-Bit Universal Shift/Storage Register with Synchronous Reset and Common I/O Pins

General Description

The ACT323 is an 8-bit universal shift/storage register with 3-STATE outputs. Parallel load inputs and flip-flop outputs are multiplexed to minimize pin count. Separate serial inputs and outputs are provided for Q_0 and Q_7 to allow easy cascading. Four operation modes are possible: hold (store), shift left, shift right and parallel load.

Features

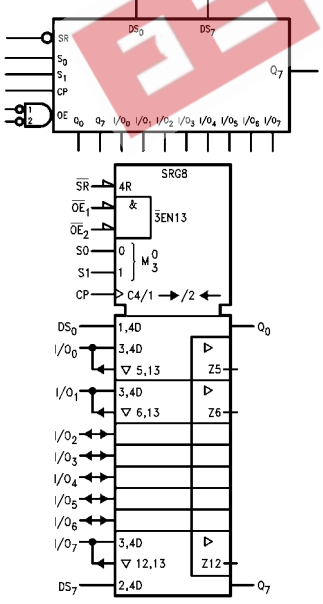
- I_{CC} and I_{OZ} reduced by 50%
- Common parallel I/O for reduced pin count
- Additional serial inputs and outputs for expansion
- Four operating modes: shift left, shift right, load and store
- 3-STATE outputs for bus-oriented applications
- Outputs source/sink 24 mA
- TTL-compatible inputs

Ordering Code:

Order Number	Package Number	Package Description
74ACT323PC	N20A	20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

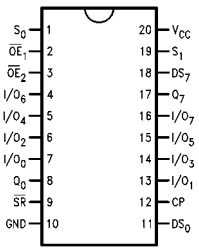
Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code.

Logic Symbols



Connection Diagram

Pin Assignment for DIP



Pin Descriptions

Pin Name	Description
CP	Clock Pulse Input
DS_0	Serial Data Input for Right Shift
DS_7	Serial Data Input for Left Shift
S_0, S_1	Mode Select Inputs
$\overline{SR}$	Synchronous Reset Input
$\overline{OE}_1$, $\overline{OE}_2$	3-STATE Output Enable Inputs
I/O_0–I/O_7	Multiplexed Parallel Data Inputs or 3-STATE Parallel Data Outputs
Q_0, Q_7	Serial Outputs

FACT™ is a trademark of Fairchild Semiconductor Corporation.

Functional Description

The ACT323 contains eight edge-triggered D-type flip-flops and the interstage logic necessary to perform synchronous reset, shift left, shift right, parallel load and hold operations. The type of operation is determined by S_0 and S_1 as shown in the Mode Select Table. All flip-flop outputs are brought out through 3-STATE buffers to separate I/O pins that also serve as data inputs in the parallel load mode. Q_0 and Q_7 are also brought out on other pins for expansion in serial shifting of longer words.

A LOW signal on $\overline{SR}$ overrides the Select inputs and allows the flip-flops to be reset by the next rising edge of CP. All other state changes are also initiated by the LOW-to-HIGH CP transition. Inputs can change when the clock is in either state provided only that the recommended setup and hold times, relative to the rising edge of CP, are observed.

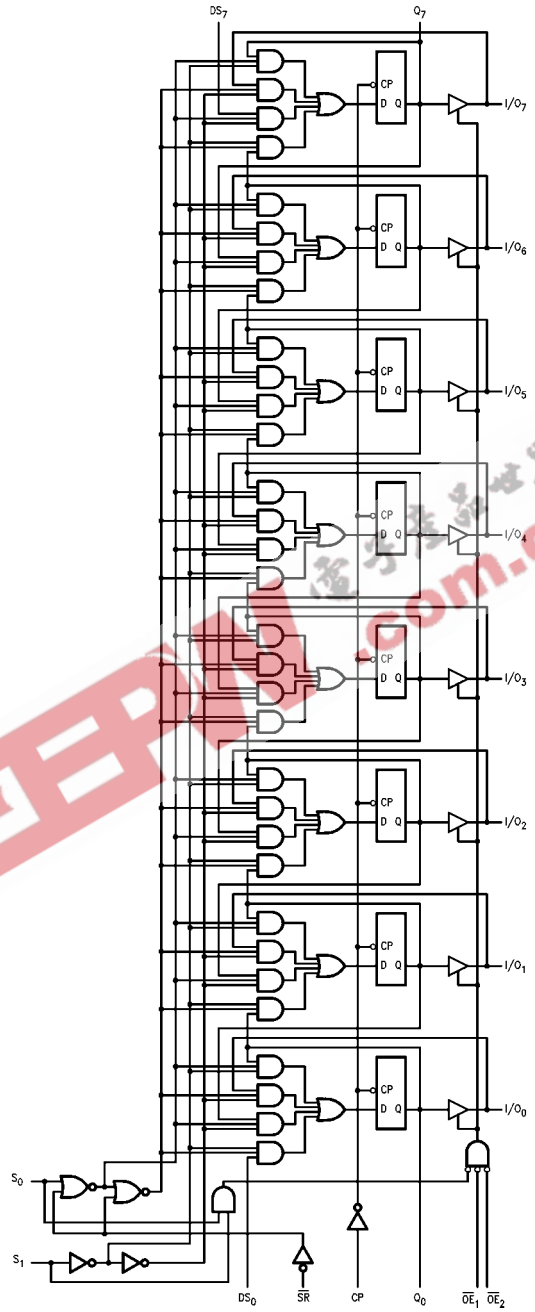
A HIGH signal on either $\overline{OE}_1$ or $\overline{OE}_2$ disables the 3-STATE buffers and puts the I/O pins in the high impedance state. In this condition the shift, load, hold and reset operations can still occur. The 3-STATE buffers are also disabled by HIGH signals on both S_0 and S_1 in preparation for a parallel load operation.

Mode Select Table

Inputs				Response
$\overline{SR}$	S_1	S_0	CP	
L	X	X	⌐	Synchronous Reset; Q_0–Q_7 = LOW
H	H	H	⌐	Parallel Load; $I/O_n \rightarrow Q_n$
H	L	H	⌐	Shift Right; $DS_0 \rightarrow Q_0$, $Q_0 \rightarrow Q_1$, etc.
H	H	L	⌐	Shift Left; $DS_7 \rightarrow Q_7$, $Q_7 \rightarrow Q_6$, etc.
H	L	L	X	Hold

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
⌐ = LOW-to-HIGH Clock Transition

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings(Note 1)

Supply Voltage (V_{CC})	−0.5V to +7.0V
DC Input Diode Current (I_{IK})	
V_I = −0.5V	−20 mA
V_I = V_{CC} + 0.5V	+20 mA
DC Input Voltage (V_I)	−0.5V to V_{CC} + 0.5V
DC Output Diode Current (I_{OK})	
V_O = −0.5V	−20 mA
V_O = V_{CC} + 0.5V	+20 mA
DC Output Voltage (V_O)	−0.5V to V_{CC} + 0.5V
DC Output Source or	
Sink Current (I_O)	±50 mA
DC V_{CC} or Ground Current	
Per Output Pin (I_{CC} or I_{GND})	±50 mA
Storage Temperature (T_{STG})	−65°C to +150°C
Junction Temperature (T_J)	
PDIP	140°C

Recommended Operating Conditions

Supply Voltage (V_{CC})	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	−40°C to +85°C
Minimum Input Edge Rate (ΔV/Δt)	
V_{IN} from 0.8V to 2.0V	
V_{CC} @ 4.5V, 5.5V	125 mV/ns

Note 1: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. Fairchild does not recommend operation of FACT™ circuits outside databook specifications.

DC Electrical Characteristics

Symbol	Parameter	V_{CC} (V)	T_A = +25°C Typ	T_A = −40°C to +85°C Guaranteed Limits		Units	Conditions
V_{IH}	Minimum High Level Input Voltage	4.5	1.5	2.0	2.0	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		5.5	1.5	2.0	2.0		
V_{IL}	Maximum Low Level Input Voltage	4.5	1.5	0.8	0.8	V	V_{OUT} = 0.1V or V_{CC} − 0.1V
		5.5	1.5	0.8	0.8		
V_{OH}	Minimum High Level Output Voltage	4.5	4.49	4.4	4.4	V	I_{OUT} = −50 μA
		5.5	5.49	5.4	5.4		
							V_{IN} = V_{IL} or V_{IH}
		4.5		3.86	3.76	V	I_{OH} = −24 mA
		5.5		4.86	4.76		I_{OH} = −24 mA (Note 2)
V_{OL}	Maximum Low Level Output Voltage	4.5	0.001	0.1	0.1	V	I_{OUT} = 50 μA
		5.5	0.001	0.1	0.1		
							V_{IN} = V_{IL} or V_{IH}
		4.5		0.36	0.44	V	I_{OL} = −24 mA
		5.5		0.36	0.44		I_{OL} = −24 mA (Note 2)
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	μA	V_I = V_{CC}, GND
I_{OZT}	Maximum I/O Leakage Current	5.5		±0.3	±3.0	μA	$V_{I/O}$ = V_{CC} or GND V_{IN} = V_{IH}, V_{IL}
I_{CCT}	Maximum I_{CC}/Input	5.5	0.6		1.5	mA	V_I = V_{CC} − 2.1V
I_{OLD}	Minimum Dynamic Output Current (Note 3)	5.5			75	mA	V_{OLD} = 1.65V Max
I_{OHD}		5.5			−75	mA	V_{OHD} = 3.85V Min
I_{CC}	Maximum Quiescent Supply Current	5.5		4.0	40.0	μA	V_{IN} = V_{CC} or GND

Note 2: All outputs loaded; thresholds on input associated with output under test.

Note 3: Maximum test duration 2.0 ms, one output loaded at a time.

AC Electrical Characteristics

Symbol	Parameter	V_{CC} (V) (Note 4)	$T_A = 25°C$, $C_L = 50$ pF			$T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units
			Min	Typ	Max	Min	Max	
f_{max}	Maximum Input Frequency	5.0	120	125		110		MHz
t_{PLH}	Propagation Delay CP to Q_0 or Q_7	5.0	5.0	9.0	12.5	4.0	14.0	ns
t_{PHL}	Propagation Delay CP to Q_0 or Q_7	5.0	5.0	9.0	13.5	4.5	15.0	ns
t_{PLH}	Propagation Delay CP to I/O_n	5.0	5.0	8.5	12.5	4.5	14.5	ns
t_{PHL}	Propagation Delay CP to I/O_n	5.0	6.0	10.0	14.5	5.0	16.0	ns
t_{PZH}	Output Enable Time	5.0	3.5	7.5	11.0	3.0	12.5	ns
t_{PZL}	Output Enable Time	5.0	3.5	7.5	11.5	3.0	13.0	ns
t_{PHZ}	Output Disable Time	5.0	4.0	8.5	12.5	3.0	13.5	ns
t_{PLZ}	Output Disable Time	5.0	3.0	8.0	11.5	2.5	12.5	ns

Note 4: Voltage Range 5.0 is 5.0V ±0.5V

AC Operating Requirements

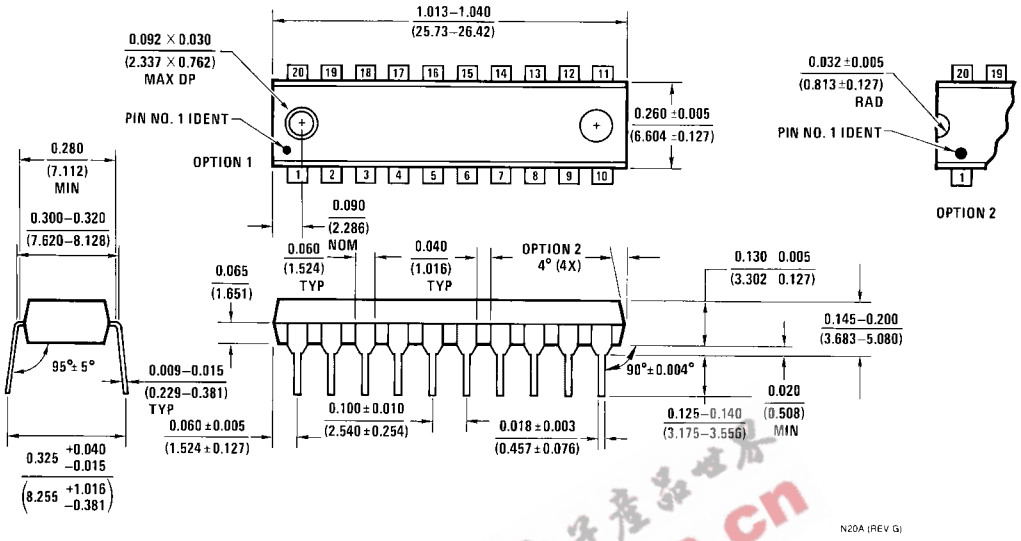
Symbol	Parameter	V_{CC} (V) (Note 5)	$T_A = 25°C$, $C_L = 50$ pF, $V_{CC} = +5.0V$	$T_A = -40°C$ to $+85°C$, $C_L = 50$ pF, $V_{CC} = +5.0V$		Units
			Typ	Guaranteed Minimum		
t_S	Setup Time, HIGH or LOW S_0 or S_1 to CP	5.0	2.0	5.0	5.0	ns
t_H	Hold Time, HIGH or LOW S_0 or S_1 to CP	5.0	0	1.5	1.5	ns
t_S	Setup Time, HIGH or LOW I/O_n, DS_0, DS_7 to CP	5.0	1.0	4.0	4.5	ns
t_H	Hold Time, HIGH or LOW I/O_n, DS_0, DS_7 to CP	5.0	0	1.0	1.0	ns
t_S	Setup Time, HIGH or LOW $\overline{SR}$ to CP	5.0	1.0	2.5	2.5	ns
t_H	Hold Time, HIGH or LOW $\overline{SR}$ to CP	5.0	0	1.0	1.0	ns
t_W	CP Pulse Width HIGH or LOW	5.0	2.0	4.0	4.5	ns

Note 5: Voltage Range 5.0 is 5.0V ±0.5V

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	V_{CC} = OPEN
C_{PD}	Power Dissipation Capacitance	170	pF	V_{CC} = 5.0V

Physical Dimensions inches (millimeters) unless otherwise noted



20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
Package Number N20A

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

www.fairchildsemi.com