

74AC74 • 74ACT74

Dual D-Type Positive Edge-Triggered Flip-Flop

General Description

The AC/ACT74 is a dual D-type flip-flop with Asynchronous Clear and Set inputs and complementary (Q , $\bar{Q}$) outputs. Information at the input is transferred to the outputs on the positive edge of the clock pulse. Clock triggering occurs at a voltage level of the clock pulse and is not directly related to the transition time of the positive-going pulse. After the Clock Pulse input threshold voltage has been passed, the Data input is locked out and information present will not be transferred to the outputs until the next rising edge of the Clock Pulse input.

Asynchronous Inputs:

- LOW input to $\bar{S}_D$ (Set) sets Q to HIGH level
- LOW input to $\bar{C}_D$ (Clear) sets Q to LOW level
- Clear and Set are independent of clock
- Simultaneous LOW on $\bar{C}_D$ and $\bar{S}_D$ makes both Q and $\bar{Q}$ HIGH

Features

- I_{CC} reduced by 50%
- Output source/sink 24 mA
- ACT74 has TTL-compatible inputs

Ordering Code:

Order Number	Package Number	Package Description
74AC74SC	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
74AC74SC_NL (Note 1)	M14A	Pb-Free 14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
74AC74SJ	M14D	Pb-Free 14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74AC74MTC	MTC14	14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
74AC74MTCX_NL (Note 2)	MTC14	Pb-Free 14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
74AC74PC	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
74ACT74SC	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
74ACT74SC_NL (Note 1)	M14A	Pb-Free 14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
74ACT74SJ	M14D	Pb-Free 14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74ACT74SJX_NL (Note 2)	M14D	Pb-Free 14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74ACT74MTC	MTC14	14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
74ACT74PC	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code.

Pb-Free package per JEDEC J-STD-020B.

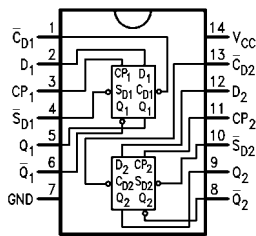
Note 1: " _NL" indicates lead-free product (per JEDEC J-STD-020B).

Note 2: " _NL" indicates lead-free product (per JEDEC J-STD-020B). Device is available in Tape and Reel only.

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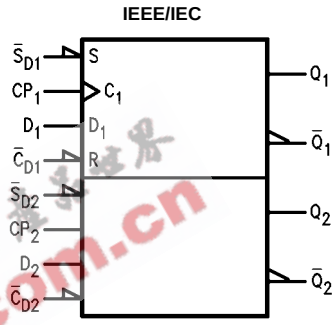
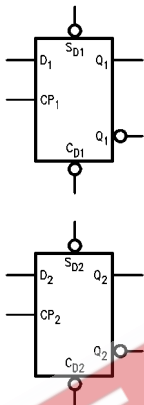
Connection Diagram



Pin Descriptions

Pin Names	Description
D ₁ , D ₂	Data Inputs
CP ₁ , CP ₂	Clock Pulse Inputs
$\overline{C}_{D1}$, $\overline{C}_{D2}$	Direct Clear Inputs
$\overline{S}_{D1}$, $\overline{S}_{D2}$	Direct Set Inputs
Q ₁ , $\overline{Q}_1$, Q ₂ , $\overline{Q}_2$	Outputs

Logic Symbols

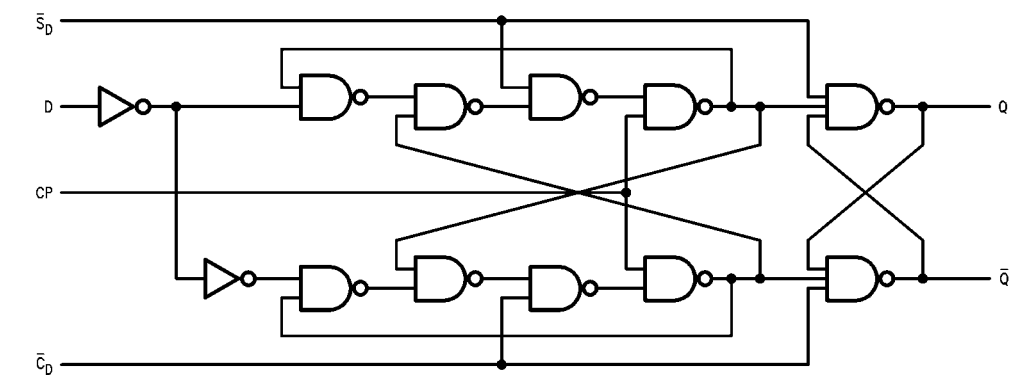


Truth Table
(Each Half)

Inputs				Outputs	
$\overline{S}_D$	$\overline{C}_D$	CP	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H	H
H	H	↗	H	H	L
H	H	↗	L	L	H
H	H	L	X	Q ₀	$\overline{Q}_0$

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
↗ = LOW-to-HIGH Clock Transition
Q₀ ($\overline{Q}_0$) = Previous Q ($\overline{Q}$) before LOW-to-HIGH Transition of Clock

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

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Absolute Maximum Ratings(Note 3)

Supply Voltage (V_{CC})	-0.5V to +7.0V
DC Input Diode Current (I_{IK})	
$V_I = -0.5V$	-20 mA
$V_I = V_{CC} + 0.5V$	+20 mA
DC Input Voltage (V_I)	-0.5V to $V_{CC} + 0.5V$
DC Output Diode Current (I_{OK})	
$V_O = -0.5V$	-20 mA
$V_O = V_{CC} + 0.5V$	+20 mA
DC Output Voltage (V_O)	-0.5V to $V_{CC} + 0.5V$
DC Output Source	
or Sink Current (I_O)	± 50 mA
DC V_{CC} or Ground Current	
per Output Pin (I_{CC} or I_{GND})	± 50 mA
Storage Temperature (T_{STG})	-65°C to +150°C
Junction Temperature (T_J)	
PDIP	140°C

Recommended Operating Conditions

Supply Voltage (V_{CC})	
AC	2.0V to 6.0V
ACT	4.5V to 5.5V
Input Voltage (V_I)	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Operating Temperature (T_A)	-40°C to +85°C
Minimum Input Edge Rate ($\Delta V/\Delta t$)	
AC Devices	
V_{IN} from 30% to 70% of V_{CC}	
V_{CC} @ 3.3V, 4.5V, 5.5V	125 mV/ns
Minimum Input Edge Rate ($\Delta V/\Delta t$)	
ACT Devices	
V_{IN} from 0.8V to 2.0V	
V_{CC} @ 4.5V, 5.5V	125 mV/ns

Note 3: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. Fairchild does not recommend operation of FACT™ circuits outside databook specifications.

DC Electrical Characteristics for AC

Symbol	Parameter	V_{CC} (V)	$T_A = +25^\circ\text{C}$		$T_A = -40^\circ\text{C to } +85^\circ\text{C}$	Units	Conditions
			Typ	Guaranteed Limits			
V_{IH}	Minimum HIGH Level Input Voltage	3.0	1.5	2.1	2.1	V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$
		4.5	2.25	3.15	3.15		
		5.5	2.75	3.85	3.85		
V_{IL}	Maximum LOW Level Input Voltage	3.0	1.5	0.9	0.9	V	$V_{OUT} = 0.1V$ or $V_{CC} - 0.1V$
		4.5	2.25	1.35	1.35		
		5.5	2.75	1.65	1.65		
V_{OH}	Minimum HIGH Level Output Voltage	3.0	2.99	2.9	2.9	V	$I_{OUT} = -50 \mu A$
		4.5	4.49	4.4	4.4		
		5.5	5.49	5.4	5.4		
		3.0		2.56	2.46	V	$V_{IN} = V_{IL}$ or V_{IH} $I_{OH} = -12$ mA $I_{OH} = -24$ m $I_{OH} = -24$ m (Note 4)
		4.5		3.86	3.76		
		5.5		4.86	4.76		
V_{OL}	Maximum LOW Level Output Voltage	3.0	0.002	0.1	0.1	V	$I_{OUT} = 50 \mu A$
		4.5	0.001	0.1	0.1		
		5.5	0.001	0.1	0.1		
		3.0		0.36	0.44	V	$V_{IN} = V_{IL}$ or V_{IH} $I_{OL} = 12$ mA $I_{OL} = 24$ mA $I_{OL} = 24$ mA (Note 4)
		4.5		0.36	0.44		
		5.5		0.36	0.44		
I_{IN} (Note 6)	Maximum Input Leakage Current	5.5		± 0.1	± 1.0	μA	$V_I = V_{CC}, GND$
I_{OLD}	Minimum Dynamic	5.5			75	mA	$V_{OLD} = 1.65V$ Maximum
I_{OHD}	Output Current (Note 5)	5.5			-75	mA	$V_{OHD} = 3.85V$ Minimum
I_{CC} (Note 6)	Maximum Quiescent Supply Current	5.5		2.0	20.0	μA	$V_{IN} = V_{CC}$ or GND

Note 4: All outputs loaded; thresholds on input associated with output under test.

Note 5: Maximum test duration 2.0 ms, one output loaded at a time.

Note 6: I_{IN} and I_{CC} @ 3.0V are guaranteed to be less than or equal to the respective limit @ 5.5V V_{CC} .

DC Electrical Characteristics for ACT

Symbol	Parameter	V _{CC} (V)	T _A = +25°C		T _A = -40°C to +85°C		Units	Conditions
			Typ	Guaranteed Limits				
V _{IH}	Minimum HIGH Level Input Voltage	4.5	1.5	2.0	2.0		V	V _{OUT} = 0.1V or V _{CC} - 0.1V
		5.5	1.5	2.0	2.0			
V _{IL}	Maximum LOW Level Output Voltage	4.5	1.5	0.8	0.8		V	V _{OUT} = 0.1V or V _{CC} - 0.1V
		5.5	1.5	0.8	0.8			
V _{OH}	Minimum HIGH Level Output Voltage	4.5	4.49	4.4	4.4		V	I _{OUT} = -50 μA
		5.5	5.49	5.4	5.4			
		4.5		3.86	3.76		V	V _{IN} = V _{IL} or V _{IH} I _{OH} = -24 mA I _{OH} = -24 mA (Note 7)
		5.5		4.86	4.76			
V _{OL}	Maximum LOW Level Output Voltage	4.5	0.001	0.1	0.1		V	I _{OUT} = 50 μA
		5.5	0.001	0.1	0.1			
		4.5		0.36	0.44		V	V _{IN} = V _{IL} or V _{IH} I _{OL} = 24 mA I _{OL} = 24 mA (Note 7)
		5.5		0.36	0.44			
I _{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0		μA	V _I = V _{CC} , GND
I _{CCT}	Maximum I _{CC} /Input	5.5	0.6		1.5		mA	V _I = V _{CC} - 2.1V
I _{OLD}	Minimum Dynamic	5.5			75		mA	V _{OLD} = 1.65V Maximum
I _{OHD}	Output Current (Note 8)	5.5			-75		mA	V _{OHD} = 3.85V Minimum
I _{CC}	Maximum Quiescent Supply Current	5.5		2.0	20.0		μA	V _{IN} = V _{CC} or GND

Note 7: All outputs loaded; thresholds on input associated with output under test.

Note 8: Maximum test duration 2.0 ms, one output loaded at a time.

AC Electrical Characteristics for AC

Symbol	Parameter	V _{CC} (V) (Note 9)	T _A = +25°C C _L = 50 pF			T _A = -40°C to +85°C C _L = 50 pF		Units
			Min	Typ	Max	Min	Max	
f _{MAX}	Maximum Clock Frequency	3.3	100	125		95		MHz
		5.0	140	160		125		
t _{PLH}	Propagation Delay C _{Dn} or S _{Dn} to Q _n or Q _n	3.3	3.5	8.0	12.0	2.5	13.0	ns
		5.0	2.5	6.0	9.0	2.0	10.0	
t _{PHL}	Propagation Delay C _{Dn} or S _{Dn} to Q _n or Q _n	3.3	4.0	10.5	12.0	3.5	13.5	ns
		5.0	3.0	8.0	9.5	2.5	10.5	
t _{PLH}	Propagation Delay CP _n to Q _n or Q _n	3.3	4.5	8.0	13.5	4.0	16.0	ns
		5.0	3.5	6.0	10.0	3.0	10.5	
t _{PHL}	Propagation Delay CP _n to Q _n or Q _n	3.3	3.5	8.0	14.0	3.5	14.5	ns
		5.0	2.5	6.0	10.0	2.5	10.5	

Note 9: Voltage Range 3.3 is 3.3V ± 0.3V

Voltage Range 5.0 is 5.0V ± 0.5V

AC Operating Requirements for AC

Symbol	Parameter	V _{CC} (V) (Note 10)	T _A = +25°C C _L = 50 pF		T _A = -40°C to +85°C C _L = 50 pF	Units
			Typ	Guaranteed Minimum		
		t _S	Set-up Time, HIGH or LOW D _n to CP _n	3.3 5.0	1.5 1.0	
t _H	Hold Time, HIGH or LOW D _n to CP _n	3.3 5.0	-2.0 -1.5	0.5 0.5	0.5 0.5	ns
t _W	CP _n or $\overline{C_{Dn}}$ or $\overline{S_{Dn}}$ Pulse Width	3.3 5.0	3.0 2.5	5.5 4.5	7.0 5.0	ns
t _{rec}	Recovery Time $\overline{C_{Dn}}$ or $\overline{S_{Dn}}$ to CP	3.3 5.0	-2.5 -2.0	0 0	0 0	ns

Note 10: Voltage Range 3.3 is 3.3V ± 0.3V

Voltage Range 5.0 is 5.0V ± 0.5V

AC Electrical Characteristics for ACT

Symbol	Parameter	V _{CC} (V) (Note 11)	T _A = +25°C C _L = 50 pF			T _A = -40°C to +85°C C _L = 50 pF		Units
			Min	Typ	Max	Min	Max	
f _{MAX}	Maximum Clock Frequency	5.0	145	210		125		MHz
t _{PLH}	Propagation Delay $\overline{C_{Dn}}$ or $\overline{S_{Dn}}$ to Q _n or $\overline{Q_n}$	5.0	3.0	5.5	9.5	2.5	10.5	ns
t _{PHL}	Propagation Delay $\overline{C_{Dn}}$ or $\overline{S_{Dn}}$ to Q _n or $\overline{Q_n}$	5.0	3.0	6.0	10.0	3.0	11.5	ns
t _{PLH}	Propagation Delay CP _n to Q _n or $\overline{Q_n}$	5.0	4.0	7.5	11.0	4.0	13.0	ns
t _{PHL}	Propagation Delay CP _n to Q _n or $\overline{Q_n}$	5.0	3.5	6.0	10.0	3.0	11.5	ns

Note 11: Voltage Range 5.0 is 5.0V ± 0.5V

AC Operating Requirements for ACT

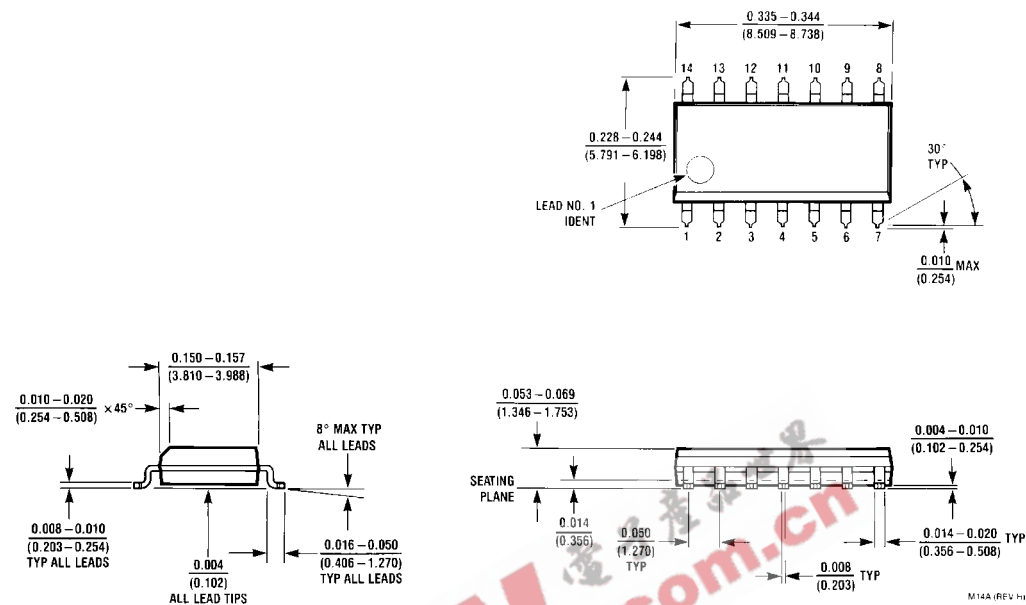
Symbol	Parameter	V _{CC} (V) (Note 12)	T _A = +25°C C _L = 50 pF		T _A = −40°C to +85°C C _L = 50 pF	Units
			Typ	Guaranteed Minimum		
t _S	Set-up Time, HIGH or LOW D _n to CP _n	5.0	1.0	3.0	3.5	ns
t _H	Hold Time, HIGH or LOW D _n to CP _n	5.0	−0.5	1.0	1.0	ns
t _W	CP _n or $\overline{C_{Dn}}$ or $\overline{S_{Dn}}$ Pulse Width	5.0	3.0	5.0	6.0	ns
t _{rec}	Recovery Time $\overline{C_{Dn}}$ or $\overline{S_{Dn}}$ to CP	5.0	−2.5	0	0	ns

Note 12: Voltage Range 5.0 is 5.0V ± 0.5V

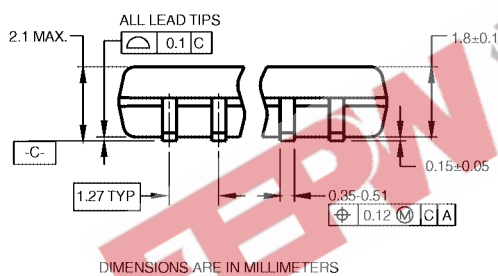
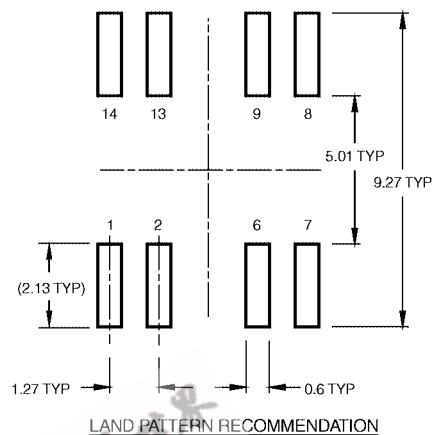
Capacitance

Symbol	Parameter	Typ	Units	Conditions
C _{IN}	Input Capacitance	4.5	pF	V _{CC} = OPEN
C _{PD}	Power Dissipation Capacitance	35.0	pF	V _{CC} = 5.0V

Physical Dimensions inches (millimeters) unless otherwise noted



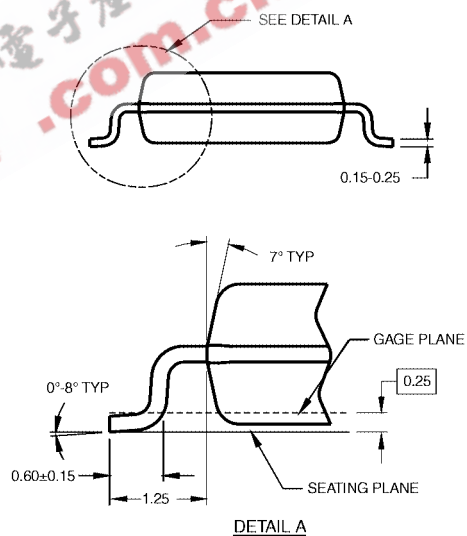
14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
Package Number M14A



NOTES:

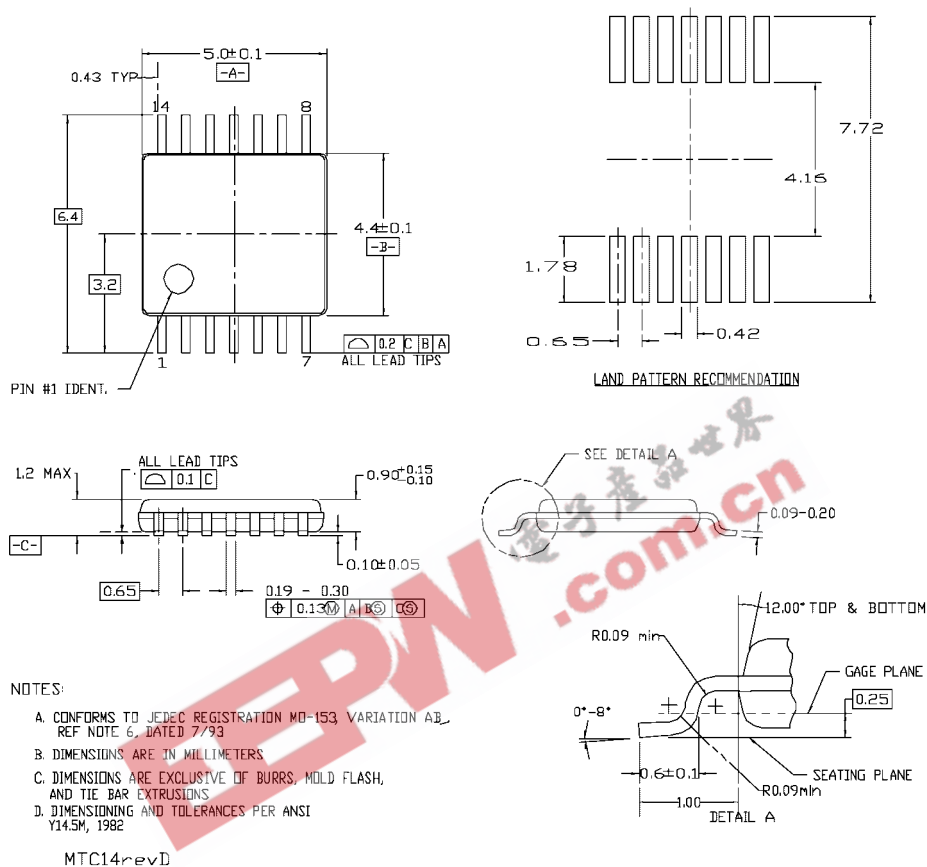
- A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

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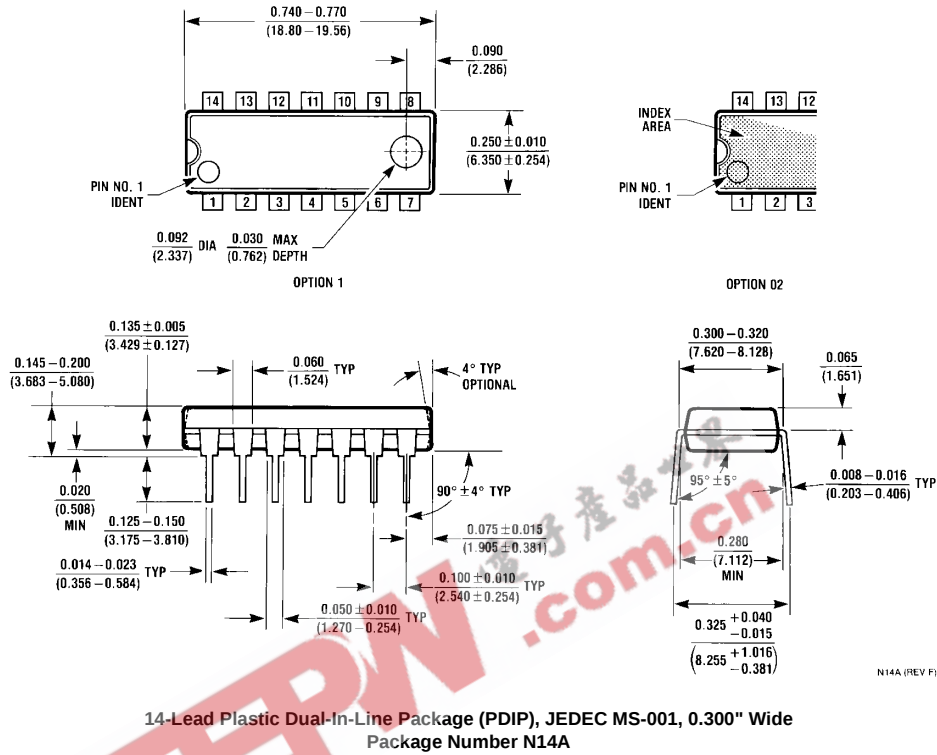
**Pb-Free 14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
Package Number M14D**

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



**14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
Package Number MTC14**

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



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