

54F/74F191 Up/Down Binary Counter with Preset and Ripple Clock

General Description

The 'F191 is a reversible modulo-16 binary counter featuring synchronous counting and asynchronous presetting. The preset feature allows the 'F191 to be used in programmable dividers. The Count Enable input, the Terminal Count output and Ripple Clock output make possible a variety of methods of implementing multistage counters. In the counting modes, state changes are initiated by the rising edge of the clock.

Features

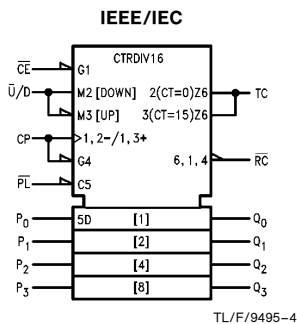
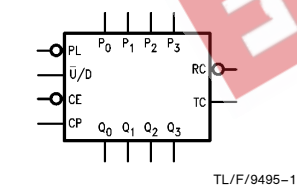
- High-Speed—125 MHz typical count frequency
- Synchronous counting
- Asynchronous parallel load
- Cascadable

| Commercial | Military | Package Number | Package Description |
|-------------------|-------------------|----------------|---|
| 74F191PC | | N16E | 16-Lead (0.300" Wide) Molded Dual-In-Line |
| | 54F191DM (Note 2) | J16A | 16-Lead Ceramic Dual-In-Line |
| 74F191SC (Note 1) | | M16A | 16-Lead (0.150" Wide) Molded Small Outline, JEDEC |
| 74F191SJ (Note 1) | | M16D | 16-Lead (0.300" Wide) Molded Small Outline, EIAJ |
| | 54F191FM (Note 2) | W16A | 16-Lead Cerpack |
| | 54F191LM (Note 2) | E20A | 20-Lead Ceramic Leadless Chip Carrier, Type C |

Note 1: Devices also available in 13" reel. Use suffix = SCX and SJX.

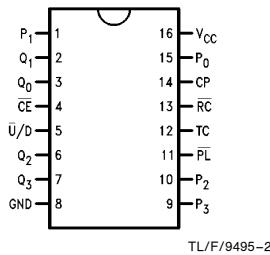
Note 2: Military grade device with environmental and burn-in processing. Use suffix = DMQB, FMQB and LMQB.

Logic Symbols

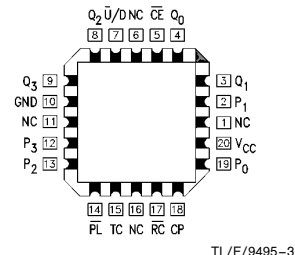


Connection Diagrams

Pin Assignment for DIP, SOIC and Flatpak



Pin Assignment for LCC



TRI-STATE® is a registered trademark of National Semiconductor Corporation.

Unit Loading/Fan Out

| Pin Names | Description | 54F/74F | |
|--------------------------------|---|------------------|---|
| | | U.L. HIGH/LOW | Input I _{IH} /I _{IL} Output I _{OH} /I _{OL} |
| \overline{CE} | Count Enable Input (Active LOW) | 1.0/3.0 | 20 μ A/ -1.8 mA |
| CP | Clock Pulse Input (Active Rising Edge) | 1.0/1.0 | 20 μ A/ -0.6 mA |
| P ₀ -P ₃ | Parallel Data Inputs | 1.0/1.0 | 20 μ A/ -0.6 mA |
| \overline{PL} | Asynchronous Parallel Load Input (Active LOW) | 1.0/1.0 | 20 μ A/ -0.6 mA |
| $\overline{U/D}$ | Up/Down Count Control Input | 1.0/1.0 | 20 μ A/ -0.6 mA |
| Q ₀ -Q ₃ | Flip-Flop Outputs | 50/33.3 | -1 mA/20 mA |
| \overline{RC} | Ripple Clock Output (Active LOW) | 50/33.3 | -1 mA/20 mA |
| TC | Terminal Count Output (Active HIGH) | 50/33.3 | -1 mA/20 mA |

Functional Description

The 'F191 is a synchronous up/down 4-bit binary counter. It contains four edge-triggered flip-flops, with internal gating and steering logic to provide individual preset, count-up and count-down operations.

Each circuit has an asynchronous parallel load capability permitting the counter to be preset to any desired number. When the Parallel Load (\overline{PL}) input is LOW, information present on the Parallel Data inputs (P₀-P₃) is loaded into the counter and appears on the Q outputs. This operation overrides the counting functions, as indicated in the Mode Select Table.

A HIGH signal on the \overline{CE} input inhibits counting. When \overline{CE} is LOW, internal state changes are initiated synchronously by the LOW-to-HIGH transition of the clock input. The direction of counting is determined by the $\overline{U/D}$ input signal, as indicated in the Mode Select Table. \overline{CE} and $\overline{U/D}$ can be changed with the clock in either state, provided only that the recommended setup and hold times are observed.



Two types of outputs are provided as overflow/underflow indicators. The Terminal Count (TC) output is normally LOW and goes HIGH when a circuit reaches zero in the count-down mode or reaches 15 in the count-up mode. The TC output will then remain HIGH until a state change occurs, whether by counting or presetting or until $\overline{U/D}$ is changed. The TC output should not be used as a clock signal because it is subject to decoding spikes.

The TC signal is also used internally to enable the Ripple Clock (\overline{RC}) output. The \overline{RC} output is normally HIGH. When \overline{CE} is LOW and TC is HIGH, the \overline{RC} output will go LOW when the clock next goes LOW and will stay LOW until the clock goes HIGH again. This feature simplifies the design of multistage counters, as indicated in Figures 1 and 2. In Figure 1, each \overline{RC} output is used as the clock input for the next higher stage. This configuration is particularly advantageous when the clock source has a limited drive capability, since it drives only the first stage. To prevent counting in all stages it is only necessary to inhibit the first stage, since a HIGH signal on \overline{CE} inhibits the \overline{RC} output pulse, as indicated in the \overline{RC} Truth Table. A disadvantage of this configuration, in some applications, is the timing skew between state changes in the first and last stages. This represents the cumulative delay of the clock as it ripples through the preceding stages.



A method of causing state changes to occur simultaneously in all stages is shown in Figure 2. All clock inputs are driven in parallel and the \overline{RC} outputs propagate the carry/borrow signals in ripple fashion. In this configuration the LOW state duration of the clock must be long enough to allow the negative-going edge of the carry/borrow signal to ripple through to the last stage before the clock goes HIGH. There is no such restriction on the HIGH state duration of the clock, since the \overline{RC} output of any device goes HIGH shortly after its CP input goes HIGH.



The configuration shown in Figure 3 avoids ripple delays and their associated restrictions. The \overline{CE} input for a given stage is formed by combining the TC signals from all the preceding stages. Note that in order to inhibit counting an enable signal must be included in each carry gate. The simple inhibit scheme of Figures 1 and 2 doesn't apply, because the TC output of a given stage is not affected by its own \overline{CE} .

Mode Select Table

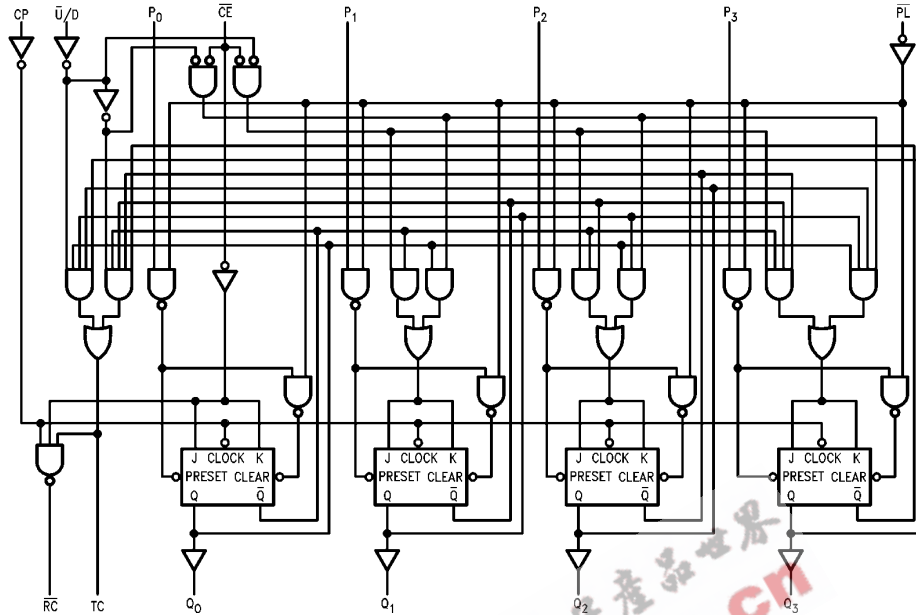
| Inputs | | | | Mode |
|-----------------|-----------------|------------------|---|------------------|
| \overline{PL} | \overline{CE} | $\overline{U/D}$ | CP | |
| H | L | L |  | Count Up |
| H | L | H |  | Count Down |
| L | X | X | X | Preset (Asyn.) |
| H | H | X | X | No Change (Hold) |

\overline{RC} Truth Table

| Inputs | | | Output |
|-----------------|-----|---|---|
| \overline{CE} | TC* | CP | \overline{RC} |
| L | H |  |  |
| H | X | X | H |
| X | L | X | H |

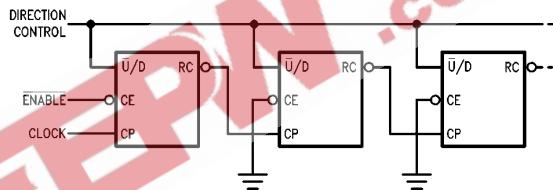
*TC is generated internally
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
 = LOW-to-HIGH Clock Transition
 = LOW Pulse

Logic Diagram



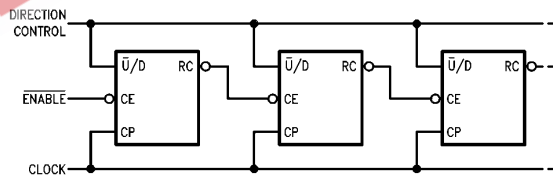
TL/F/9495-5

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.



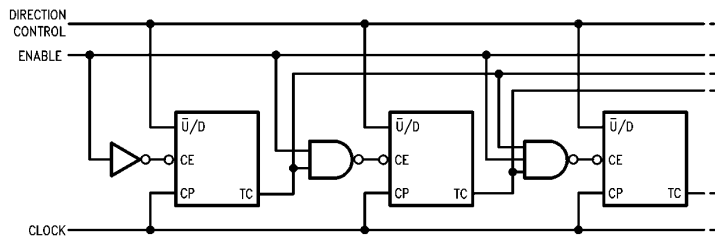
TL/F/9495-6

FIGURE 1. n-Stage Counter Using Ripple Clock



TL/F/9495-7

FIGURE 2. Synchronous n-Stage Counter Using Ripple Carry/Borrow



TL/F/9495-8

FIGURE 3. Synchronous n-Stage Counter with Gated Carry/Borrow

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

| | |
|---|--------------------------|
| Storage Temperature | -65°C to +150°C |
| Ambient Temperature under Bias | -55°C to +125°C |
| Junction Temperature under Bias | -55°C to +175°C |
| Plastic | -55°C to +150°C |
| V _{CC} Pin Potential to Ground Pin | -0.5V to +7.0V |
| Input Voltage (Note 2) | -0.5V to +7.0V |
| Input Current (Note 2) | -30 mA to +5.0 mA |
| Voltage Applied to Output in HIGH State (with V _{CC} = 0V) | |
| Standard Output | -0.5V to V _{CC} |
| TRI-STATE® Output | -0.5V to +5.5V |

Current Applied to Output in LOW State (Max) twice the rated I_{OL} (mA)

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

Recommended Operating Conditions

| | |
|------------------------------|-----------------|
| Free Air Ambient Temperature | |
| Military | -55°C to +125°C |
| Commercial | 0°C to +70°C |
| Supply Voltage | |
| Military | +4.5V to +5.5V |
| Commercial | +4.5V to +5.5V |

DC Electrical Characteristics

| Symbol | Parameter | 54F/74F | | | Units | V _{CC} | Conditions |
|------------------|-----------------------------------|--|-------------------|--------------|-------|-----------------|--|
| | | Min | Typ | Max | | | |
| V _{IH} | Input HIGH Voltage | 2.0 | | | V | | Recognized as a HIGH Signal |
| V _{IL} | Input LOW Voltage | | | 0.8 | V | | Recognized as a LOW Signal |
| V _{CD} | Input Clamp Diode Voltage | | | -1.2 | V | Min | I _{IN} = -18 mA |
| V _{OH} | Output HIGH Voltage | 54F 10% V _{CC} 74F 10% V _{CC} 74F 5% V _{CC} | 2.5 2.5 2.7 | | V | Min | I _{OH} = -1 mA I _{OH} = -1 mA I _{OH} = -1 mA |
| V _{OL} | Output LOW Voltage | 54F 10% V _{CC} 74F 10% V _{CC} | | 0.5 0.5 | V | Min | I _{OL} = 20 mA I _{OL} = 20 mA |
| I _{IH} | Input HIGH Current | 54F 74F | | 20.0 5.0 | μA | Max | V _{IN} = 2.7V |
| I _{BVI} | Input HIGH Current Breakdown Test | 54F 74F | | 100 7.0 | μA | Max | V _{IN} = 7.0V |
| I _{CEX} | Output HIGH Leakage Current | 54F 74F | | 250 50 | μA | Max | V _{OUT} = V _{CC} |
| V _{ID} | Input Leakage Test | 74F | 4.75 | | V | 0.0 | I _{ID} = 1.9 μA, All Other Pins Grounded |
| I _{OD} | Output Leakage Circuit Current | 74F | | 3.75 | μA | 0.0 | V _{IOD} = 150 mV All Other Pins Grounded |
| I _{IL} | Input LOW Current | | | -0.6 -1.8 | mA | Max | V _{IN} = 0.5V (except \overline{CE}) V _{IN} = 0.5V (\overline{CE}) |
| I _{OS} | Output Short-Circuit Current | | -60 | -150 | mA | Max | V _{OUT} = 0V |
| I _{CC} | Power Supply Current | | 38 | 55 | mA | Max | |

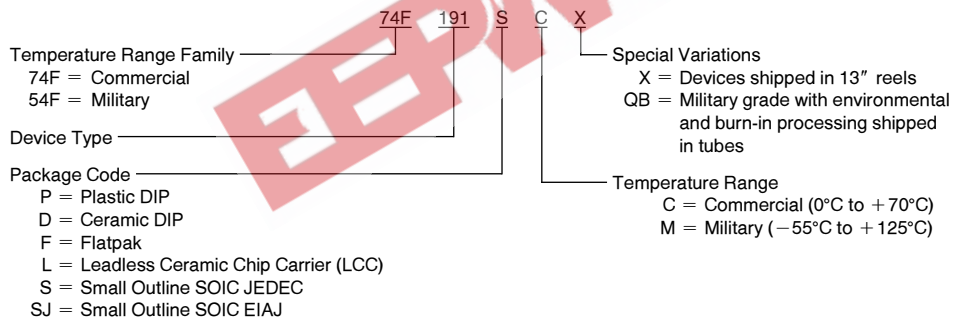
| AC Electrical Characteristics | | | | | | | | | |
|--------------------------------------|--|---|-------------|--------------|--|--------------|--|--------------|-------|
| Symbol | Parameter | 74F | | | 54F | | 74F | | Units |
| | | T _A = +25°C V _{CC} = +5.0V C _L = 50 pF | | | T _A , V _{CC} = Mil C _L = 50 pF | | T _A , V _{CC} = Com C _L = 50 pF | | |
| | | Min | Typ | Max | Min | Max | Min | Max | |
| f _{max} | Maximum Count Frequency | 100 | 125 | | 75 | | 90 | | MHz |
| t _{PLH} t _{PHL} | Propagation Delay CP to Q _n | 3.0 5.0 | 5.5 8.5 | 7.5 11.0 | 3.0 5.0 | 9.5 13.5 | 3.0 5.0 | 8.5 12.0 | ns |
| t _{PLH} t _{PHL} | Propagation Delay CP to TC | 6.0 5.0 | 10.0 8.5 | 13.0 11.0 | 6.0 5.0 | 16.5 13.5 | 6.0 5.0 | 14.0 12.0 | |
| t _{PLH} t _{PHL} | Propagation Delay CP to \overline{RC} | 3.0 3.0 | 5.5 5.0 | 7.5 7.0 | 3.0 3.0 | 9.5 9.0 | 3.0 3.0 | 8.5 8.0 | ns |
| t _{PLH} t _{PHL} | Propagation Delay \overline{CE} to \overline{RC} | 3.0 3.0 | 5.0 5.5 | 7.0 7.0 | 3.0 3.0 | 9.0 9.0 | 3.0 3.0 | 8.0 8.0 | |
| t _{PLH} t _{PHL} | Propagation Delay $\overline{U/D}$ to \overline{RC} | 7.0 5.5 | 11.0 9.0 | 18.0 12.0 | 7.0 5.5 | 22.0 14.0 | 7.0 5.5 | 20.0 13.0 | ns |
| t _{PLH} t _{PHL} | Propagation Delay $\overline{U/D}$ to TC | 4.0 4.0 | 7.0 6.5 | 10.0 10.0 | 4.0 4.0 | 13.5 12.5 | 4.0 4.0 | 11.0 11.0 | |
| t _{PLH} t _{PHL} | Propagation Delay P _n to Q _n | 3.0 6.0 | 4.5 10.0 | 7.0 13.0 | 3.0 6.0 | 9.0 16.0 | 3.0 6.0 | 8.0 14.0 | ns |
| t _{PLH} t _{PHL} | Propagation Delay \overline{PL} to Q _n | 5.0 5.5 | 8.5 9.0 | 11.0 12.0 | 5.0 5.5 | 13.0 14.5 | 5.0 5.5 | 12.0 13.0 | |
| t _{PLH} t _{PHL} | Propagation Delay P _n to TC | 5.0 6.5 | | 14.0 13.0 | | | 5.0 6.0 | 15.0 14.0 | ns |
| t _{PLH} t _{PHL} | Propagation Delay P _n to \overline{RC} | 6.5 6.0 | | 19.0 14.0 | | | 6.5 6.0 | 20.0 15.0 | |
| t _{PLH} t _{PHL} | Propagation Delay \overline{PL} to TC | 8.0 6.0 | | 16.5 13.5 | | | 8.0 6.0 | 17.5 14.5 | ns |
| t _{PLH} t _{PHL} | Propagation Delay \overline{PL} to \overline{RC} | 10.0 9.0 | | 20.0 15.5 | | | 10.0 9.0 | 21.0 16.0 | |

AC Operating Requirements

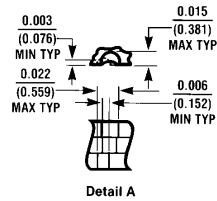
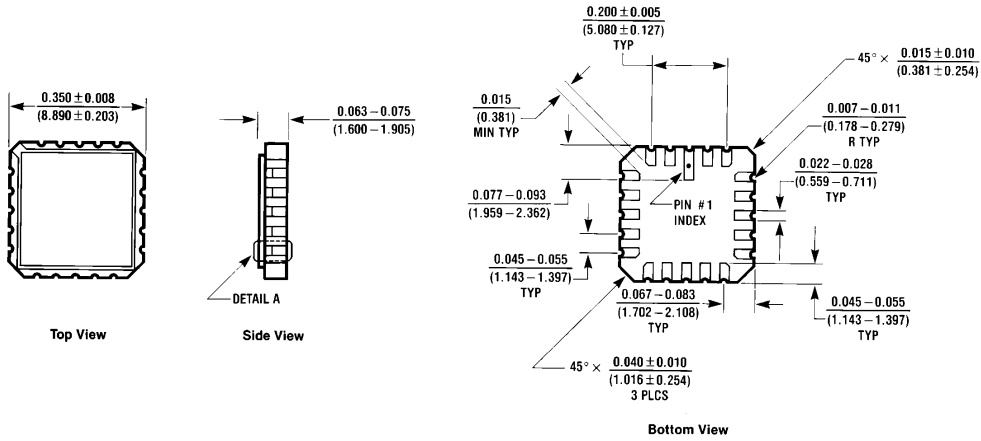
| Symbol | Parameter | 74F | | 54F | | 74F | | Units |
|--|--|---|-----|--|-----|--|-----|-------|
| | | T _A = +25°C V _{CC} = +5.0V | | T _A , V _{CC} = Mil | | T _A , V _{CC} = Com | | |
| | | Min | Max | Min | Max | Min | Max | |
| t _s (H) t _s (L) | Setup Time, HIGH or LOW P _n to \overline{PL} | 4.5 | | 6.0 | | 5.0 | | ns |
| t _h (H) t _h (L) | Hold Time, HIGH or LOW P _n to \overline{PL} | 2.0 | | 2.0 | | 2.0 | | |
| t _s (L) | Setup Time LOW \overline{CE} to CP | 10.0 | | 10.5 | | 10.0 | | ns |
| t _h (L) | Hold Time LOW \overline{CE} to CP | 0 | | 0 | | 0 | | |
| t _s (H) t _s (L) | Setup Time, HIGH or LOW $\overline{U/D}$ to CP | 12.0 | | 12.0 | | 12.0 | | ns |
| t _h (H) t _h (L) | Hold Time, HIGH or LOW $\overline{U/D}$ to CP | 0 | | 0 | | 0 | | |
| t _w (L) | \overline{PL} Pulse Width LOW | 6.0 | | 8.5 | | 6.0 | | ns |
| t _w (L) | CP Pulse Width LOW | 5.0 | | 7.0 | | 5.0 | | ns |
| t _{rec} | Recovery Time \overline{PL} to CP | 6.0 | | 7.5 | | 6.0 | | ns |

Ordering Information

The device number is used to form part of a simplified purchasing code where the package type and temperature range are defined as follows:

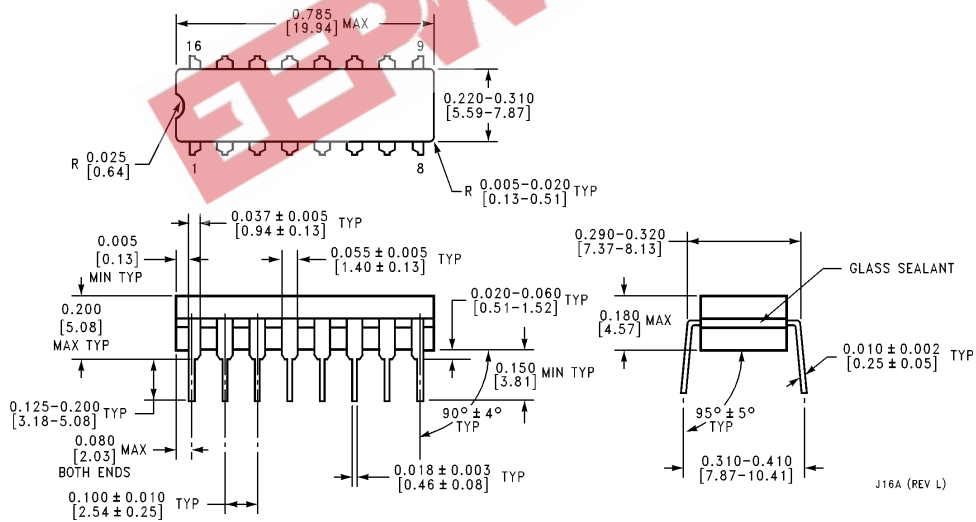


Physical Dimensions inches (millimeters)



20-Lead Ceramic Leadless Chip Carrier (L)
NS Package Number E20A

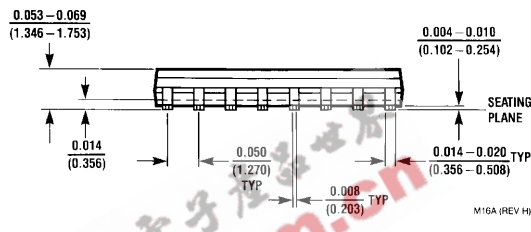
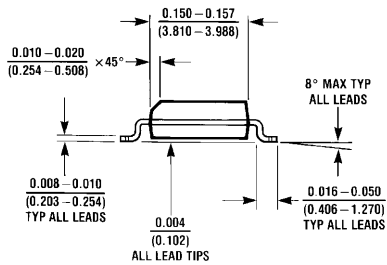
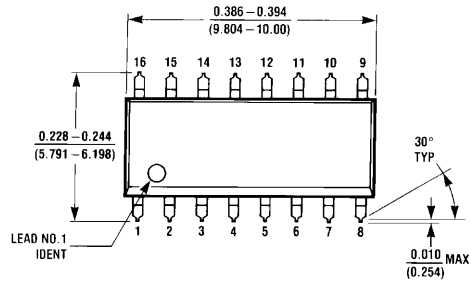
E20A (REV D)



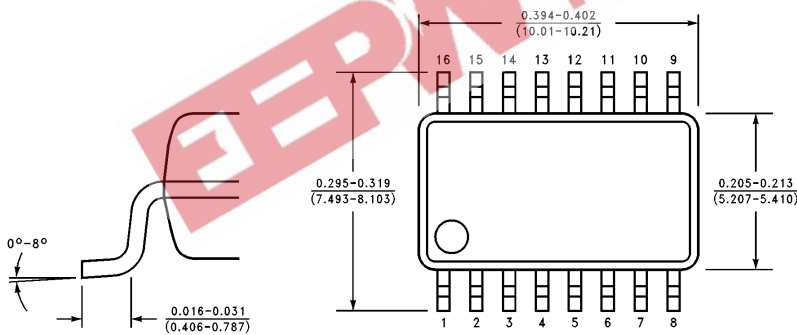
16-Lead Ceramic Dual-In-Line Package (D)
NS Package Number J16A

J16A (REV L)

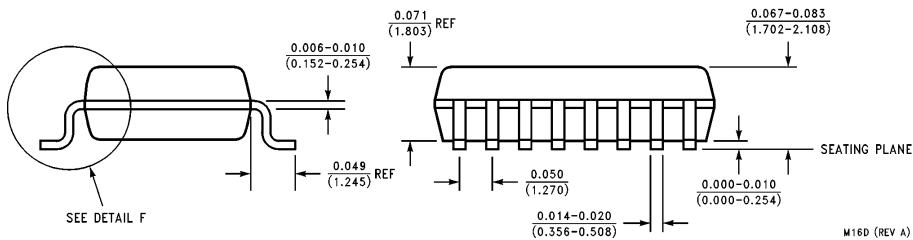
Physical Dimensions inches (millimeters) (Continued)



16-Lead (0.150" Wide) Molded Small Outline Package, JEDEC (S)
NS Package Number M16A

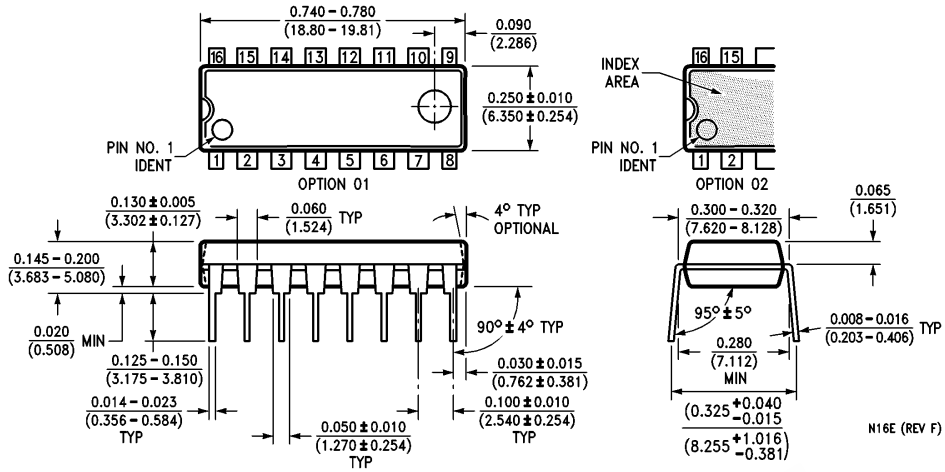


DETAIL F



16-Lead (0.300" Wide) Molded Small Outline Package, EIAJ (SJ)
NS Package Number M16D

Physical Dimensions inches (millimeters) (Continued)

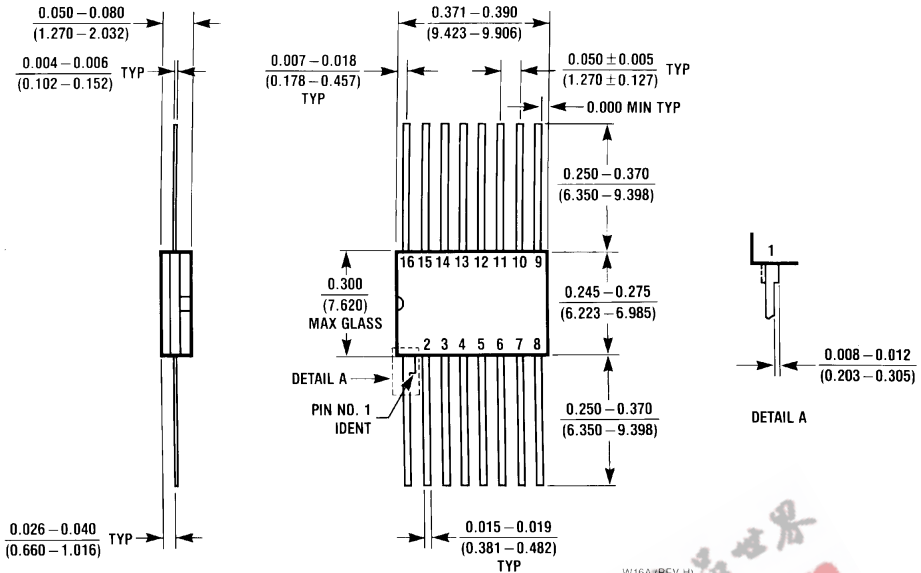


16-Lead (0.300" Wide) Molded Dual-In-Line Package (P)
NS Package Number N16E

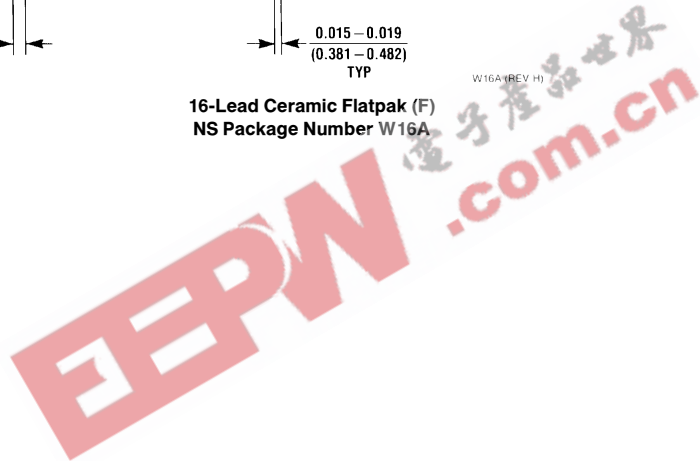
N16E (REV F)



Physical Dimensions inches (millimeters) (Continued)



**16-Lead Ceramic Flatpak (F)
NS Package Number W16A**



LIFE SUPPORT POLICY

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

| | | | | | |
|---|---|---|---|--|---|
|  <p>National Semiconductor Corporation 2900 Semiconductor Drive P.O. Box 58090 Santa Clara, CA 95052-8090 Tel: 1 (800) 272-9959 TWX: (910) 339-9240</p> | <p>National Semiconductor GmbH Livry-Gargan-Str. 10 D-82256 Fürstenfeldbruck Germany Tel: (81-41) 35-0 Telex: 527649 Fax: (81-41) 35-1</p> | <p>National Semiconductor Japan Ltd. Sumitomo Chemical Engineering Center Bldg. 7F 1-7-1, Nakase, Mihama-Ku Chiba-City, Chiba Prefecture 261 Tel: (043) 299-2300 Fax: (043) 299-2500</p> | <p>National Semiconductor Hong Kong Ltd. 13th Floor, Straight Block, Ocean Centre, 5 Canton Rd. Tsimshatsui, Kowloon Hong Kong Tel: (852) 2737-1600 Fax: (852) 2736-9960</p> | <p>National Semiconductores Do Brazil Ltda. Rue Deputado Lacorda Franco 120-3A Sao Paulo-SP Brazil 05418-000 Tel: (55-11) 212-5066 Telex: 391-1131931 NSBR BR Fax: (55-11) 212-1181</p> | <p>National Semiconductor (Australia) Pty, Ltd. Building 16 Business Park Drive Monash Business Park Nottingham, Melbourne Victoria 3168 Australia Tel: (3) 558-9889 Fax: (3) 558-9898</p> |
|---|---|---|---|--|---|

National does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied and National reserves the right at any time without notice to change said circuitry and specifications.