

August 1986 Revised March 2000

## DM74LS74A

# **Dual Positive-Edge-Triggered D Flip-Flops with Preset, Clear and Complementary Outputs**

## **General Description**

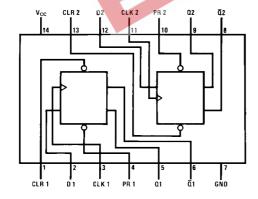
This device contains two independent positive-edge-triggered D flip-flops with complementary outputs. The information on the D input is accepted by the flip-flops on the positive going edge of the clock pulse. The triggering occurs at a voltage level and is not directly related to the transition time of the rising edge of the clock. The data on the D input may be changed while the clock is LOW or HIGH without affecting the outputs as long as the data setup and hold times are not violated. A low logic level on the preset or clear inputs will set or reset the outputs regardless of the logic levels of the other inputs.

## **Ordering Code:**

HIGH without aff setup and hold tir the preset or cle	ecting the outputs a	the clock is LOW or as long as the data  I. A low logic level on or reset the outputs her inputs.
Ordering C	Code:	a gom.
Order Number	Package Number	Package Description
DM74LS74AM	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150 Narrow
DM74LS85ASJ	M14D	14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
DM74LS74AN	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code

#### **Connection Diagram**



#### **Function Table**

Inputs				Outputs			
PR	CLR	CLK	D	Q	Q		
L	Н	Х	Х	Н	L		
Н	L	Χ	Χ	L	Н		
L	L	Х	Х	H (Note 1)	H (Note 1)		
Н	Н	1	Н	Н	L		
Н	Н	1	L	L	Н		
Н	Н	L	Х	$Q_0$	$\overline{Q}_0$		

- H = HIGH Logic Level
- X = Either LOW or HIGH Logic Level
- L = LOW Logic Level
- ↑ = Positive-going Transition
- $\mathbf{Q}_0 = \mathsf{The}\ \mathsf{output}\ \mathsf{logic}\ \mathsf{level}\ \mathsf{of}\ \mathsf{Q}\ \mathsf{before}\ \mathsf{the}\ \mathsf{indicated}\ \mathsf{input}\ \mathsf{conditions}\ \mathsf{were}$

Note 1: This configuration is nonstable; that is, it will not persist when either the preset and/or clear inputs return to their inactive (HIGH) level.

## **Absolute Maximum Ratings**(Note 2)

Supply Voltage Input Voltage Operating Free Air Temperature Range 0°C to +70°C -65°C to +150°C Storage Temperature Range

Note 2: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

## **Recommended Operating Conditions**

Symbol	Parameter		Min	Nom	Max	Units
V <sub>CC</sub>	Supply Voltage		4.75	5	5.25	V
V <sub>IH</sub>	HIGH Level Input Voltag	е	2			V
V <sub>IL</sub>	LOW Level Input Voltage	е			0.8	V
I <sub>ОН</sub>	HIGH Level Output Curr	ent			-0.4	mA
I <sub>OL</sub>	LOW Level Output Curre	ent			8	mA
f <sub>CLK</sub>	Clock Frequency (Note 3)		0		25	MHz
f <sub>CLK</sub>	Clock Frequency (Note 4)		0	48	20	MHz
t <sub>W</sub>	Pulse Width	Clock HIGH	18	正原		
	(Note 3)	Preset LOW	15	7.0	A .	ns
		Clear LOW	15			
t <sub>W</sub>	Pulse Width	Clock HIGH	25	-0.		
	(Note 4)	Preset LOW	20			ns
		Clear LOW	20	,		
t <sub>SU</sub>	Setup Time (Note 3)(Note 5)		20↑	_		ns
t <sub>SU</sub>	Setup Time (Note 4)(Note 5)		25↑			ns
t <sub>H</sub>	Hold Time (Note 5)(Note 6)		01			ns
T <sub>A</sub>	Free Air Operating Temperature		0		70	°C

Note 3:  $C_L$  = 15 pF,  $R_L$  = 2 k $\Omega$ ,  $T_A$  = 25°C, and  $V_{CC}$  = 5V. Note 4:  $C_L$  = 50 pF,  $R_L$  = 2 k $\Omega$ ,  $T_A$  = 25°C, and  $V_{CC}$  = 5V. Note 5: The symbol (1) indicates the rising edge of the clock pulse is used for reference. Note 6:  $T_A$  = 25°C and  $V_{CC}$  = 5V.

#### **Electrical Characteristics**

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ (Note 7)	Max	Units
VI	Input Clamp Voltage	$V_{CC} = Min, I_I = -18 \text{ mA}$				-1.5	V
V <sub>OH</sub>	HIGH Level	V <sub>CC</sub> = Min, I <sub>OH</sub> = Max		2.7	3.4		V
	Output Voltage	$V_{IL} = Max, V_{IH} = Min$		2.1	3.4		V
V <sub>OL</sub>	LOW Level	V <sub>CC</sub> = Min, I <sub>OL</sub> = Max			0.35	0.5	
	Output Voltage	$V_{IL} = Max, V_{IH} = Min$			0.35	0.5	V
		I <sub>OL</sub> = 4 mA, V <sub>CC</sub> = Min			0.25	0.4	
I	Input Current @ Max	V <sub>CC</sub> = Max	Data			0.1	
	Input Voltage	$V_I = 7V$	Clock			0.1	mA
			Preset			0.2	IIIA
			Clear			0.2	
I <sub>IH</sub>	HIGH Level	V <sub>CC</sub> = Max	Data			20	
	Input Current	$V_I = 2.7V$	Clock			20	μА
			Clear			40	μΛ
			Preset			40	
I <sub>IL</sub>	LOW Level	V <sub>CC</sub> = Max	Data		- The same	-0.4	
	Input Current	$V_I = 0.4V$	Clock	4.4	, /10	-0.4	mA
			Preset	- 34		-0.8	IIIA
			Clear	9	( C / )	-0.8	
los	Short Circuit Output Current	V <sub>CC</sub> = Max (Note 8)	20 13	-20	A. C.	-100	mA
Icc	Supply Current	V <sub>CC</sub> = Max (Note 9)	CIL	411	4	8	mA

Note 7: All typicals are at  $V_{CC} = 5V$ ,  $T_A = 25^{\circ}C$ .

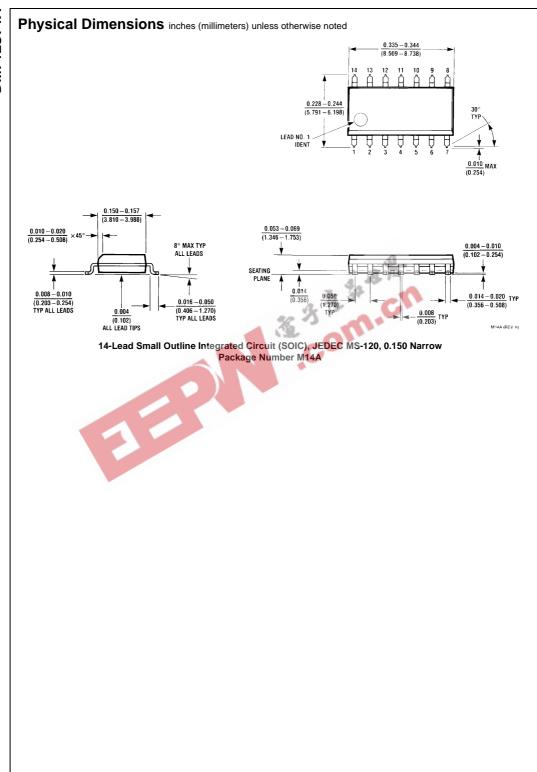
Note 8: Not more than one output should be shorted at a time, and the duration should not exceed one second. For devices, with feedback from the outputs, where shorting the outputs to ground may cause the outputs to change logic state an equivalent test may be performed where V<sub>O</sub> = 2.125V with the minimum and maximum limits reduced by one half from their stated values. This is very useful when using automatic test equipment.

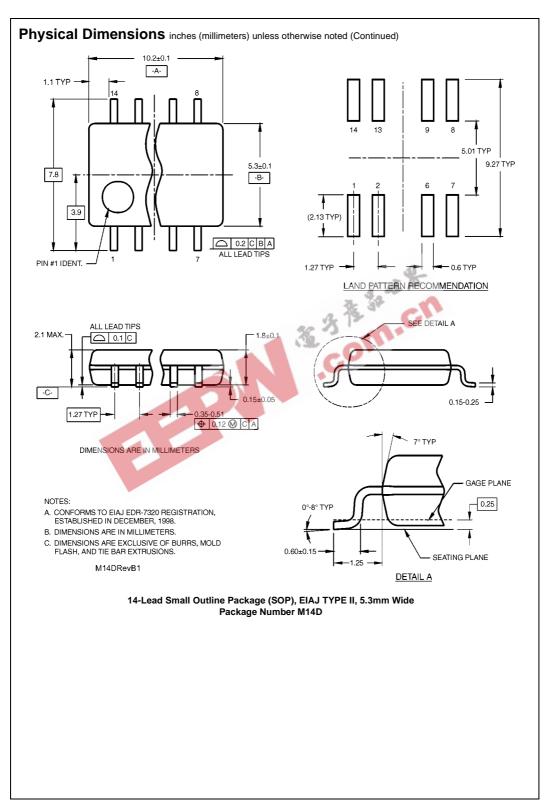
Note 9: With all outputs OPEN, I<sub>CC</sub> is measured with CLOCK grounded after setting the Q and Q outputs HIGH in turn.

## **Switching Characteristics**

at  $V_{CC} = 5V$  and  $T_A = 25^{\circ}C$ 

	Parameter	From (Input)		R <sub>L</sub> =	<b>2 k</b> Ω		
Symbol		To (Output)	C <sub>L</sub> = 15 pF		C <sub>L</sub> = 50 pF		Units
			Min	Max	Min	Max	
f <sub>MAX</sub>	Maximum Clock Frequency		25		20		MHz
t <sub>PLH</sub>	Propagation Delay Time LOW-to-HIGH Level Output	Clock to Q or Q		25		35	ns
t <sub>PHL</sub>	Propagation Delay Time HIGH-to-LOW Level Output	Clock to Q or Q		30		35	ns
t <sub>PLH</sub>	Propagation Delay Time LOW-to-HIGH Level Output	Preset to Q		25		35	ns
t <sub>PHL</sub>	Propagation Delay Time HIGH-to-LOW Level Output	Preset to Q		30		35	ns
t <sub>PLH</sub>	Propagation Delay Time LOW-to-HIGH Level Output	Clear to Q		25		35	ns
t <sub>PHL</sub>	Propagation Delay Time HIGH-to-LOW Level Output	Clear to Q		30		35	ns





#### Physical Dimensions inches (millimeters) unless otherwise noted (Continued) 0.740 - 0.770(18.80 - 19.56)(2.286) 14 13 12 14 13 12 11 10 9 8 INDEX AREA $0.250 \pm 0.010$ (6.350 ± 0.254) PIN NO. 1 IDENT PIN NO. 1 IDENT 1 2 3 4 5 6 7 1 2 3 $\frac{0.092}{(2.337)}$ DIA $\frac{0.030}{(0.762)}$ MAX OPTION 1 OPTION 02 $\frac{0.135 \pm 0.005}{(3.429 \pm 0.127)}$ 0.300 - 0.320 $\overline{(7.620 - 8.128)}$ 0.065 0.145 - 0.2000.060 TYP 4° TYP (3.683 - 5.080)(1.524) OPTIONAL \* $\frac{0.008 - 0.016}{(0.203 - 0.406)}$ TYP 0.020 $\frac{0.125 - 0.150}{(3.175 - 3.810)}$ 0.280 $\overline{(1.905\pm0.381)}$ (7.112)-MIN $\frac{0.014-0.023}{(0.356-0.584)}\,\mathrm{TYP}$ 0.100 ± 0.010 (2.540 ± 0.254) 0.050 ± 0.010 (1.270 - 0.254) $0.325 + 0.040 \\ -0.015$ $\left(8.255 + 1.016\right) - 0.381$ N14A (REV F) 14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide Package Number N14A

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