CY74FCT16543T
CY74FCT162543T
CY74FCT162H543T

16-Bit Latched Transceivers

SCCS059 - August 1994 - Revised March 2000

Features

- **FCT-E speed at 3.4 ns**
- **Power-off disable outputs permits live insertion**
- **Edge-rate control circuitry for significantly improved noise characteristics**
- **Typical output skew < 250 ps**
- **ESD > 2000V**
- **TSSOP (19.6-mil pitch) and SSOP (25-mil pitch) packages**
- **Industrial temperature range of −40˚C to +85˚C**
- **V_{CC} = 5V ± 10%**

CY74FCT16543T Features:

- **64 mA sink current, 32 mA source current**
- **Typical V_{OLP} (ground bounce) <1.0V at V_{CC} = 5V, T_A = 25˚C**

CY74FCT162543T Features:

- **Balanced 24 mA output drivers**
- **Reduced system switching noise**
- **Typical V_{OLP} (ground bounce) <0.6V at V_{CC} = 5V, T_A= 25˚C**

CY74FCT162H543T Features:

- **Bus hold retains last active state**
- **Eliminates the need for external pull-up or pull-down resistors**

Functional Description

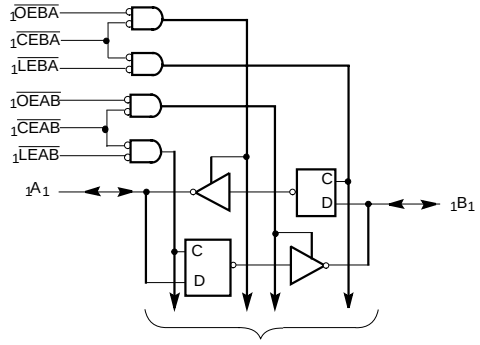
The CY74FCT16543T and CY74FCT162543T are 16-bit, high-speed, low power latched transceivers that are organized as two independent 8-bit D-type latched transceivers containing two sets of eight D-type latches with separate Latch Enable ($\overline{LEAB}$, $\overline{LEAB}$) and Output Enable ($\overline{OEAB}$, $\overline{OEAB}$) controls for each set to permit independent control of inputting and outputting in either direction of data flow. For data flow from A to B, for example, the A-to-B input Enable ($\overline{CEAB}$) must be LOW in order to enter data from A or to take data from B as indicated in the truth table. With $\overline{CAEB}$ LOW, a LOW signal on the A-to-B Latch Enable ($\overline{LEAB}$) makes the A-to-B latches transparent; a subsequent LOW-to-HIGH transition of the $\overline{LEAB}$ signal puts the A latches in the storage mode and their outputs no longer change with the A inputs. With $\overline{CEAB}$ and $\overline{OEAB}$ both LOW, the three-state B output buffers are active and reflect the data present at the output of the A latches. Control of data from B to A is similar, but uses $\overline{CEAB}$, $\overline{LEAB}$, and $\overline{OEAB}$ inputs flow-through pinout and small shrink packaging and in simplifying board design. The output buffers are designed with a power-off disable feature to allow live insertion of boards.

The CY74FCT16543T is ideally suited for driving high-capacitance loads and low-impedance backplanes.

The CY74FCT162543T has 24-mA balanced output drivers with current limiting resistors in the outputs. This reduces the need for external terminating resistors and provides for minimal undershoot and reduced ground bounce. The CY74FCT162543T is ideal for driving transmission lines.

The CY74FCT162H543T is a 24-mA balanced output part that has “bus hold” on the data inputs. The device retains the input’s last state whenever the input goes to high impedance. This eliminates the need for pull-up/down resistors and prevents floating inputs.

Logic Block Diagrams



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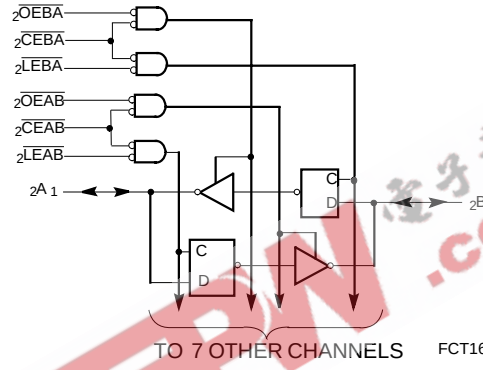

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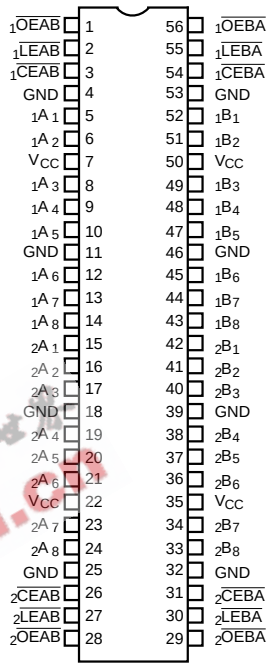
Pin Configuration

Top View
SSOP/TSSOP



FCT16543T-3

Pin Description

Name	Description
$\overline{OEAB}$	A-to-B Output Enable Input (Active LOW)
$\overline{OEBA}$	B-to-A Output Enable Input (Active LOW)
$\overline{CEAB}$	A-to-B Enable Input (Active LOW)
$\overline{CEBA}$	B-to-A Enable Input (Active LOW)
$\overline{LEAB}$	A-to-B Latch Enable Input (Active LOW)
$\overline{LEBA}$	B-to-A Latch Enable Input (Active LOW)
A	A-to-B Data Inputs or B-to-A Three-State Outputs[9]
B	B-to-A Data Inputs or A-to-B Three-State Outputs[9]

Function Table[1]

Inputs			Latch Status	Output Buffers
$\overline{CEAB}$	$\overline{LEAB}$	$\overline{OEAB}$	A to B	B
H	X	X	Storing	High Z
X	H	X	Storing	X
X	X	H	X	High Z
L	L	L	Transparent	Current A Inputs
L	H	L	Storing	Previous A Inputs[2]

Maximum Ratings[3, 4]

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .....Com'l –55°C to +125°C

Ambient Temperature with Power Applied .....Com'l –55°C to +125°C

DC Input Voltage .....–0.5V to +7.0V

DC Output Voltage .....–0.5V to +7.0V

DC Output Current (Maximum Sink Current/Pin) .....–60 to +120 mA

Power Dissipation 1.0W

Static Discharge Voltage.....>2001V (per MIL-STD-883, Method 3015)

Operating Range

Range	Ambient Temperature	V_{CC}
Industrial	–40°C to +85°C	5V ± 10%

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	Min.	Typ.[5]	Max.	Unit
V_{IH}	Input HIGH Voltage		2.0			V
V_{IL}	Input LOW Voltage				0.8	V
V_H	Input Hysteresis[6]			100		mV
V_{IK}	Input Clamp Diode Voltage	V_{CC}=Min., I_{IN}=−18 mA		–0.7	–1.2	V
I_{IH}	Input HIGH Current	V_{CC}=Max., V_I=V_{CC}			±1	µA
I_{IL}	Input LOW Current	V_{CC}=Max., V_I=GND			±1	µA
I_{OZH}	High Impedance Output Current (Three-State Output pins)	V_{CC}=Max., V_{OUT}=2.7V			±1	µA
I_{OZL}	High Impedance Output Current (Three-State Output pins)	V_{CC}=Max., V_{OUT}=0.5V			±1	µA
I_{OS}	Short Circuit Current[7]	V_{CC}=Max., V_{OUT}=GND	–80	–140	–200	mA
I_O	Output Drive Current[7]	V_{CC}=Max., V_{OUT}=2.5V	–50		–180	mA
I_{OFF}	Power-Off Disable	V_{CC}=0V, V_{OUT}≤4.5V[8]			±1	µA

Notes:

1. A-to-B data flow shown; B-to-A flow control is the same, except using $\overline{CEBA}$, LEBA, and $\overline{OEBA}$.
2. Data prior to $\overline{LEAB}$ LOW-to-HIGH Transition
   H = HIGH Voltage Level. L = LOW Voltage Level.
   X = Don't Care. Z = High Impedance.
3. Operation beyond the limits set forth may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.
4. Unused inputs must always be connected to an appropriate logic voltage level, preferably either V_{CC} or ground.
5. Typical values are at V_{CC}= 5.0V, T_A= +25˚C ambient.
6. This parameter is specified but not tested.
7. Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parametric tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
8. Tested at +25˚C.
9. On the 74FCT162H543T, these pins have bus hold.

Output Drive Characteristics for CY74FCT16543T

Parameter	Description	Test Conditions	Min.	Typ.[5]	Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC}=Min., I_{OH}=−3 mA	2.5	3.5		V
		V_{CC}=Min., I_{OH}=−15 mA	2.4	3.5		
		V_{CC}=Min., I_{OH}=−32 mA	2.0	3.0		
V_{OL}	Output LOW Voltage	V_{CC}=Min., I_{OL}=64 mA		0.2	0.55	V

Output Drive Characteristics for CY74FCT162543T, CY74FCT162H543T

Parameter	Description	Test Conditions	Min.	Typ.[5]	Max.	Unit
I_{ODL}	Output LOW Current[7]	V_{CC}=5V, V_{IN}=V_{IH} or V_{IL}, V_{OUT}=1.5V	60	115	150	mA
I_{ODH}	Output HIGH Current[7]	V_{CC}=5V, V_{IN}=V_{IH} or V_{IL}, V_{OUT}=1.5V	−60	−115	−150	mA
V_{OH}	Output HIGH Voltage	V_{CC}=Min., I_{OH}=−24 mA	2.4	3.3		V
V_{OL}	Output LOW Voltage	V_{CC}=Min., I_{OL}=24 mA		0.3	0.55	V

Capacitance[6] (T_A = +25°C, f = 1.0 MHz)

Parameter	Description	Test Conditions	Typ.[5]	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	4.5	6.0	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	5.5	8.0	pF

Power Supply Characteristics

Parameter	Description	Test Conditions		Typ.[5]	Max.	Unit
I_{CC}	Quiescent Power Supply Current	V_{CC}=Max.	V_{IN}≤0.2V, V_{IN}≥V_{CC}−0.2V	5	500	µA
ΔI_{CC}	Quiescent Power Supply Current (TTL inputs HIGH)	V_{CC}=Max.	V_{IN}=3.4V[10]	0.5	1.5	mA
I_{CCD}	Dynamic Power Supply Current[11]	V_{CC}=Max., One Input Toggling, 50% Duty Cycle, Outputs Open, $\overline{OE}$=GND	V_{IN}=V_{CC} or V_{IN}=GND	60	100	µA/MHz
I_C	Total Power Supply Current[12]	V_{CC}=Max., f_1=10 MHz, 50% Duty Cycle, Outputs Open, One Bit Toggling, $\overline{OE}$=GND	V_{IN}=V_{CC} or V_{IN}=GND	0.6	1.5	mA
			V_{IN}=3.4V or V_{IN}=GND	0.9	2.3	mA
		V_{CC}=Max., f_1=2.5 MHz, 50% Duty Cycle, Outputs Open, Sixteen Bits Toggling, $\overline{OE}$=GND	V_{IN}=V_{CC} or V_{IN}=GND	2.4	4.5[13]	mA
			V_{IN}=3.4V or V_{IN}=GND	6.4	16.5[13]	mA

Notes:

10. Per TTL driven input (V_{IN}=3.4V); all other inputs at V_{CC} or GND.
11. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
12. I_C = $I_{QUIESCENT}$ + I_{INPUTS} + $I_{DYNAMIC}$
    I_C = I_{CC}+$\Delta I_{CC} D_H N_T$+$I_{CCD}(f_0/2 + f_1 N_1)$
    I_{CC} = Quiescent Current with CMOS input levels
    ΔI_{CC} = Power Supply Current for a TTL HIGH input (V_{IN}=3.4V)
    D_H = Duty Cycle for TTL inputs HIGH
    N_T = Number of TTL inputs at D_H
    I_{CCD} = Dynamic Current caused by an input transition pair (HLH or LHL)
    f_0 = Clock frequency for registered devices, otherwise zero
    f_1 = Input signal frequency
    N_1 = Number of inputs changing at f_1
    All currents are in milliamps and all frequencies are in megahertz.
13. Values for these conditions are examples of the I_{CC} formula. These limits are specified but not tested.

Switching Characteristics Over the Operating Range[14]

Parameter	Description	CY74FCT16543T CY74FCT162543T		CY74FCT16543AT CY74FCT162543AT		Unit	Fig. No.[15]
		Min.	Max.	Min.	Max.		
t_{PLH} t_{PHL}	Propagation Delay Transparent Mode A to B or B to A	1.5	8.5	1.5	6.5	ns	1, 3
t_{PLH} t_{PHL}	Propagation Delay $\overline{LEBA}$ to A, $\overline{LEAB}$ to B	1.5	12.5	1.5	8.0	ns	1, 5
t_{PZH} t_{PZL}	Output Enable Time $\overline{OEBA}$ or $\overline{OEAB}$ to A or B $\overline{CEBA}$ or $\overline{CEAB}$ to A or B	1.5	12.0	1.5	9.0	ns	1, 7, 8
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OEBA}$ or $\overline{OEAB}$ to A or B $\overline{CEBA}$ or $\overline{CEAB}$ to A or B	1.5	9.0	1.5	7.5	ns	1, 7, 8
t_{SU}	Set-up Time HIGH or LOW A or B to $\overline{LEAB}$ or $\overline{LEBA}$	2.0	—	2.0	—	ns	4
t_H	Hold Time HIGH or LOW A or B to $\overline{LEAB}$ or $\overline{LEBA}$	2.0	—	2.0	—	ns	4
t_W	$\overline{LEBA}$ or $\overline{LEAB}$ Pulse Width LOW	4.0	—	4.0	—	ns	5
$t_{SK(O)}$	Output Skew[16]	—	0.5	—	0.5	ns	—

Parameter	Description	CY74FCT16543CT CY74FCT162543CT CY74FCT162H543CT		CY74FCT16543ET CY74FCT162543ET		Unit	Fig. No.[15]
		Min.	Max.	Min.	Max.		
t_{PLH} t_{PHL}	Propagation Delay Transparent Mode A to B or B to A	1.5	5.1	1.5	3.4	ns	1, 3
t_{PLH} t_{PHL}	Propagation Delay $\overline{LEBA}$ to A, $\overline{LEAB}$ to B	1.5	5.6	1.5	3.7	ns	1, 5
t_{PZH} t_{PZL}	Output Enable Time $\overline{OEBA}$ or $\overline{OEAB}$ to A or B $\overline{CEBA}$ or $\overline{CEAB}$ to A or B	1.5	7.8	1.5	4.8	ns	1, 7, 8
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OEBA}$ or $\overline{OEAB}$ to A or B $\overline{CEBA}$ or $\overline{CEAB}$ to A or B	1.5	6.5	1.5	4.0	ns	1, 7, 8
t_{SU}	Set-up Time HIGH or LOW A or B to $\overline{LEAB}$ or $\overline{LEBA}$	2.0	—	1.0	—	ns	4
t_H	Hold Time HIGH or LOW A or B to $\overline{LEAB}$ or $\overline{LEBA}$	2.0	—	1.0	—	ns	4
t_W	$\overline{LEBA}$ or $\overline{LEAB}$ Pulse Width LOW	4.0	—	3.0	—	ns	5
$t_{SK(O)}$	Output Skew[16]	—	0.5	—	0.5	ns	—

Notes:

14. Minimum limits are specified but not tested on Propagation Delays.
15. See “Parameter Measurement Information” in the General Information section.
16. Skew between any two outputs of the same package switching in the same directional. This parameter is ensured by design.

Ordering Information CY74FCT16543

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
3.4	CY74FCT16543ETPACT	Z56	56-Lead (240-Mil) TSSOP	Industrial
	CY74FCT16543ETPVC/PVCT	O56	56-Lead (300-Mil) SSOP	
5.1	CY74FCT16543CTPVC/PVCT	O56	56-Lead (300-Mil) SSOP	Industrial
6.5	CY74FCT16543ATPACT	Z56	56-Lead (240-Mil) TSSOP	Industrial
8.5	CY74FCT16543TPVC/PVCT	O56	56-Lead (300-Mil) SSOP	Industrial

Ordering Information CY74FCT162543

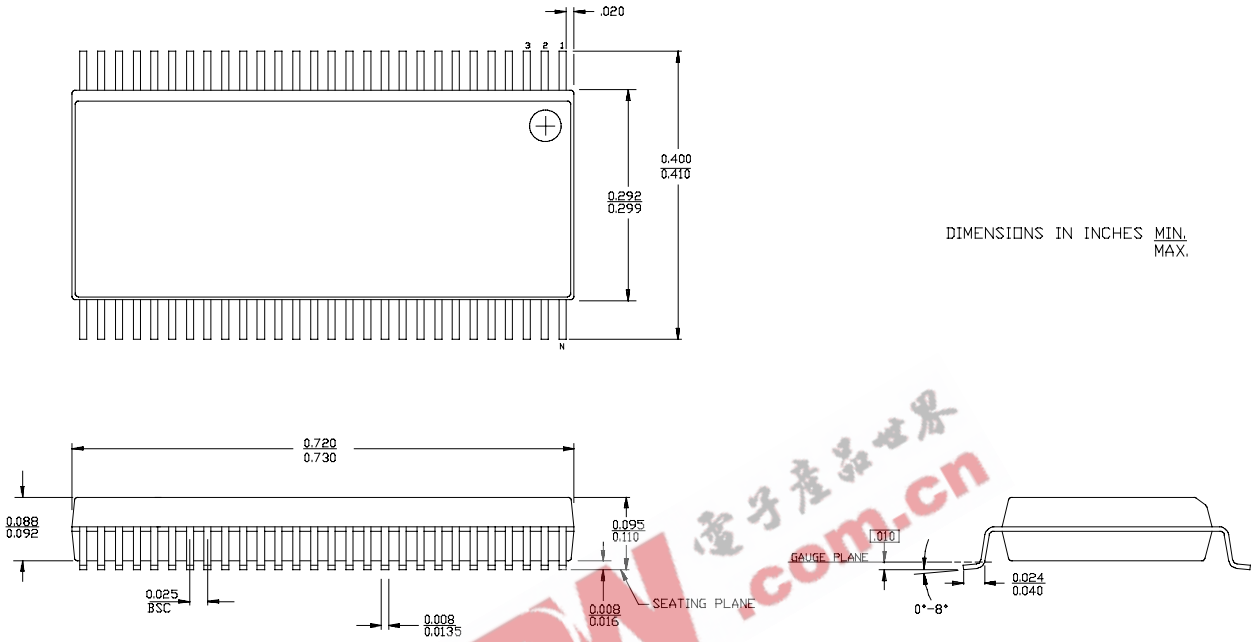
Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
3.4	74FCT162543ETPACT	Z56	56-Lead (240-Mil) TSSOP	Industrial
	CY74FCT162543ETPVC	O56	56-Lead (300-Mil) SSOP	
	74FCT162543ETPVCT	O56	56-Lead (300-Mil) SSOP	
5.1	74FCT162543CTPACT	Z56	56-Lead (240-Mil) TSSOP	Industrial
	CY74FCT162543CTPVC	O56	56-Lead (300-Mil) SSOP	
	74FCT162543CTPVCT	O56	56-Lead (300-Mil) SSOP	
6.5	74FCT162543ATPACT	Z56	56-Lead (240-Mil) TSSOP	Industrial
8.5	CY74FCT162543TPVC/PVCT	O56	56-Lead (300-Mil) SSOP	Industrial

Ordering Information CY74FCT162H543T

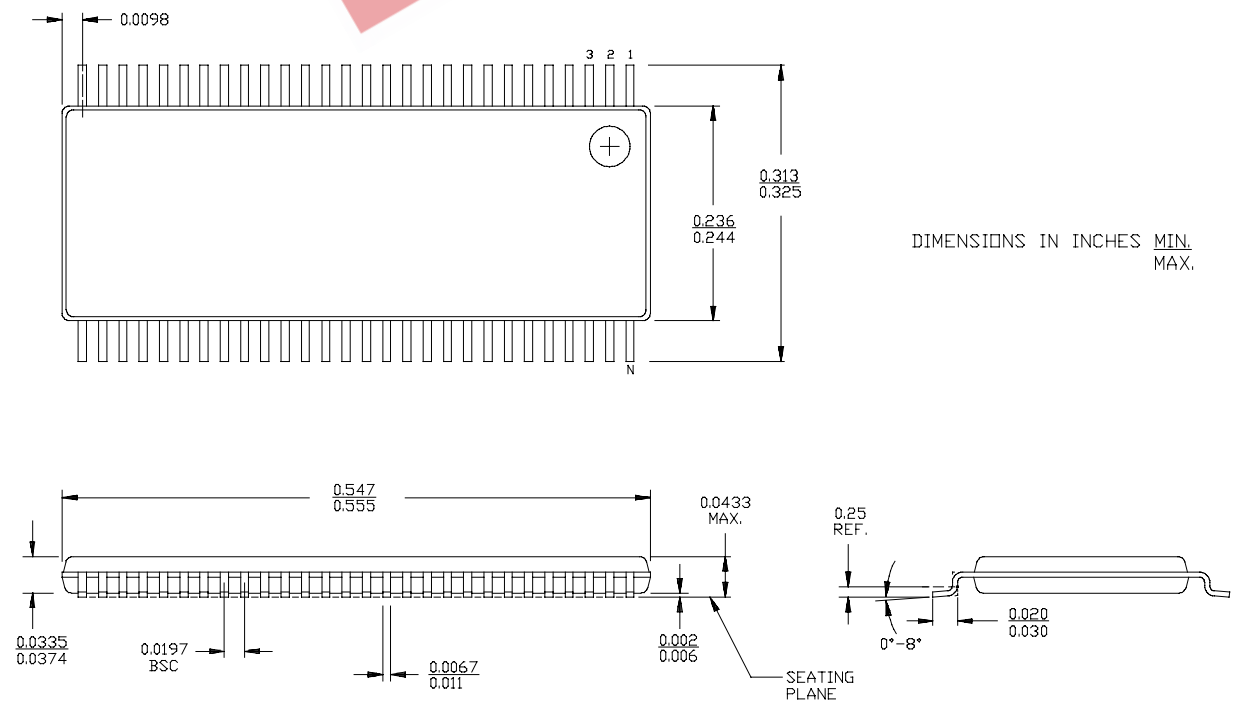
Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
5.1	74FCT162H543CTPACT	Z56	56-Lead (240-Mil) TSSOP	Industrial

Package Diagrams

56-Lead Shrunk Small Outline Package O56



56-Lead Thin Shrunk Small Outline Package Z56



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