DATA SHEET

For a complete data sheet, please also download:

- The IC06 74HC/HCT/HCU/HCMOS Logic Family Specifications
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Information
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Outlines

74HC/HCT4060

14-stage binary ripple counter with oscillator

Product specification
File under Integrated Circuits, IC06

December 1990

Philips Semiconductors

PHILIPS

14-stage binary ripple counter with oscillator 74HC/HCT4060

FEATURES

- All active components on chip
- RC or crystal oscillator configuration
- Output capability: standard (except for R_{TC} and C_{TC})
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT4060 are high-speed Si-gate CMOS devices and are pin compatible with “4060” of the “4000B” series. They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT4060 are 14-stage ripple-carry counter/dividers and oscillators with three oscillator terminals (RS, R_{TC} and C_{TC}), ten buffered outputs (Q_3 to Q_9 and Q_{11} to Q_{13}) and an overriding asynchronous master reset (MR).
The oscillator configuration allows design of either RC or crystal oscillator circuits. The oscillator may be replaced by an external clock signal at input RS. In this case keep the other oscillator pins (R_{TC} and C_{TC}) floating.

The counter advances on the negative-going transition of RS. A HIGH level on MR resets the counter (Q_3 to Q_9 and Q_{11} to Q_{13} = LOW), independent of other input conditions.

In the HCT version, the MR input is TTL compatible, but the RS input has CMOS input switching levels and can be driven by a TTL output by using a pull-up resistor to V_{CC}.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/ t_{PLH}	propagation delay	C_L = 15 pF; V_{CC} = 5 V			
	RS to Q_3		31	31	ns
	Q_n to Q_{n+1}		6	6	ns
t_{PHL}	MR to Q_n		17	18	ns
f_{max}	maximum clock frequency		87	88	MHz
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per package	notes 1, 2 and 3	40	40	pF

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):

   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$ where:

   f_i = input frequency in MHz

   f_o = output frequency in MHz

   $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs

   C_L = output load capacitance in pF

   V_{CC} = supply voltage in V
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} – 1.5 V
3. For formula on dynamic power dissipation see next pages.

ORDERING INFORMATION

See *“74HC/HCT/HCU/HCMOS Logic Package Information”*.

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 2, 3	Q_{11} to Q_{13}	counter outputs
7, 5, 4, 6, 14, 13, 15	Q_3 to Q_9	counter outputs
8	GND	ground (0 V)
9	C_{TC}	external capacitor connection
10	R_{TC}	external resistor connection
11	RS	clock input/oscillator pin
12	MR	master reset
16	V_{CC}	positive supply voltage

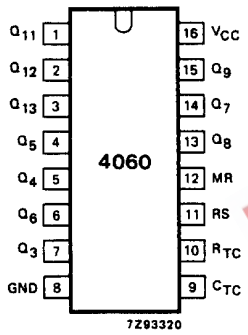


Fig.1 Pin configuration.

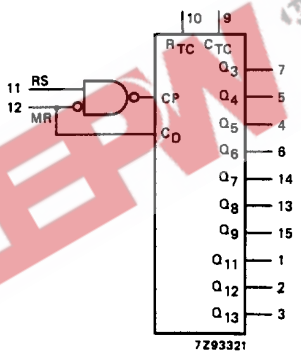


Fig.2 Logic symbol.

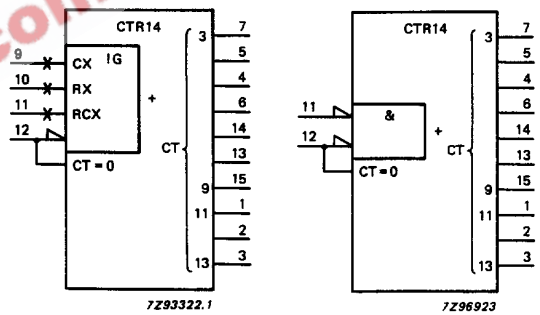


Fig.3 IEC logic symbol.

DYNAMIC POWER DISSIPATION FOR 74HC

PARAMETER	V_{CC} (V)	TYPICAL FORMULA FOR P_D (μW) (note 1)
total dynamic power dissipation when using the on-chip oscillator (P_D)	2.0	$C_{PD} \times f_{osc} \times V_{CC}^2 + \sum (C_L \times V_{CC}^2 \times f_o) + 2C_t \times V_{CC}^2 \times f_{osc} + 60 \times V_{CC}$
	4.5	$C_{PD} \times f_{osc} \times V_{CC}^2 + \sum (C_L \times V_{CC}^2 \times f_o) + 2C_t \times V_{CC}^2 \times f_{osc} + 1\,750 \times V_{CC}$
	6.0	$C_{PD} \times f_{osc} \times V_{CC}^2 + \sum (C_L \times V_{CC}^2 \times f_o) + 2C_t \times V_{CC}^2 \times f_{osc} + 3\,800 \times V_{CC}$

Note

1. GND = 0 V; T_{amb} = 25 °C

DYNAMIC POWER DISSIPATION FOR 74HCT

PARAMETER	V_{CC} (V)	TYPICAL FORMULA FOR P_D (μW) (note 1)
total dynamic power dissipation when using the on-chip oscillator (P_D)	4.5	$C_{PD} \times f_{osc} \times V_{CC}^2 + \sum (C_L \times V_{CC}^2 \times f_o) + 2C_t \times V_{CC}^2 \times f_{osc} + 1\,750 \times V_{CC}$

Notes

1. GND = 0 V; T_{amb} = 25 °C
2. Where: f_o = output frequency in MHz
   f_{osc} = oscillator frequency in MHz
   $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
   C_L = output load capacitance in pF
   C_t = timing capacitance in pF
   V_{CC} = supply voltage in V

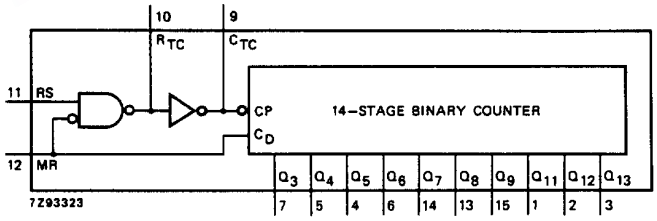


Fig.4 Functional diagram.

APPLICATIONS

- Control counters
- Timers
- Frequency dividers
- Time-delay circuits

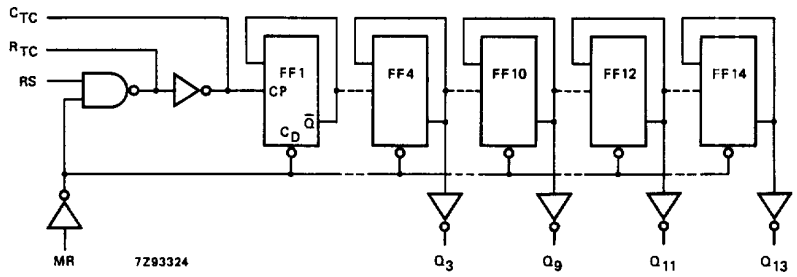


Fig.5 Logic diagram.

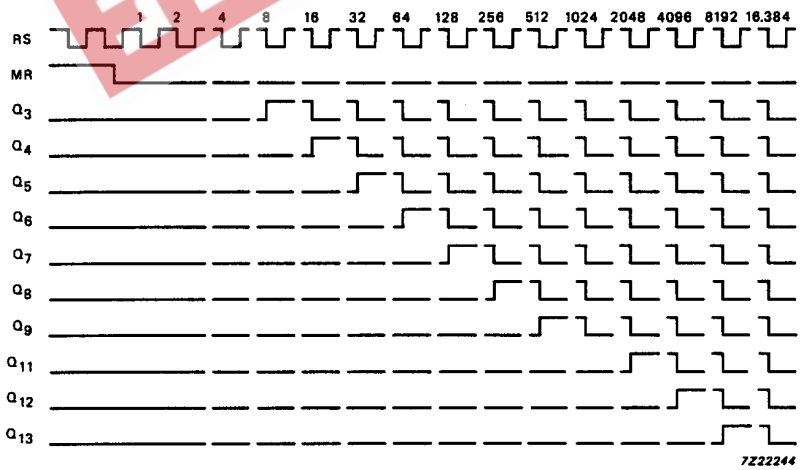


Fig.6 Timing diagram.

DC CHARACTERISTICS FOR 74HC

Output capability: standard (except for R_{TC} and C_{TC})

I_{CC} category: MSI

Voltages are referenced to GND (ground = 0 V)

SYM-BOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		74HC								V_{CC} (V)	V_I	OTHER
		+25			−40 to +85		−40 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
V_{IH}	HIGH level input voltage MR input	1.5 3.15 4.2	1.3 2.4 3.1		1.5 3.15 4.2		1.5 3.15 4.2		V	2.0 4.5 6.0		
V_{IL}	LOW level input voltage MR input		0.8 2.1 2.8	0.5 1.35 1.8		0.5 1.35 1.8		0.5 1.35 1.8	V	2.0 4.5 6.0		
V_{IH}	HIGH level input voltage RS input	1.7 3.6 4.8			1.7 3.6 4.8		1.7 3.6 4.8		V	2.0 4.5 6.0		
V_{IL}	LOW level input voltage RS input			0.3 0.9 1.2		0.3 0.9 1.2		0.3 0.9 1.2	V	2.0 4.5 6.0		
V_{OH}	HIGH level output voltage R_{TC} output	3.98 5.48			3.84 5.34		3.7 5.2		V	4.5 6.0	RS=GND and MR=GND	$-I_O$ = 2.6 mA $-I_O$ = 3.3 mA
		3.98 5.48			3.84 5.34		3.7 5.2		V	4.5 6.0	RS=V_{CC} and MR=V_{CC}	$-I_O$ = 0.65 mA $-I_O$ = 0.85 mA
		1.9 4.4 5.9	2.0 4.5 6.0		1.9 4.4 5.9		1.9 4.4 5.9		V	2.0 4.5 6.0	RS=GND and MR=GND	$-I_O$ = 20 µA $-I_O$ = 20 µA $-I_O$ = 20 µA
		1.9 4.4 5.9	2.0 4.5 6.0		1.9 4.4 5.9		1.9 4.4 5.9		V	2.0 4.5 6.0	RS=V_{CC} and MR=V_{CC}	$-I_O$ = 20 µA $-I_O$ = 20 µA $-I_O$ = 20 µA
V_{OH}	HIGH level output voltage C_{TC} output	3.98 5.48			3.84 5.34		3.7 5.2		V	4.5 6.0	RS=V_{IH} and MR=V_{IL}	$-I_O$ = 3.2 mA $-I_O$ = 4.2 mA
V_{OH}	HIGH level output voltage except R_{TC} output	1.9 4.4 5.9	2.0 4.5 6.0		1.9 4.4 5.9		1.9 4.4 5.9		V	2.0 4.5 6.0	V_{IH} or V_{IL}	$-I_O$ = 20 µA $-I_O$ = 20 µA $-I_O$ = 20 µA
V_{OH}	HIGH level output voltage except R_{TC} and C_{TC} outputs	3.98 5.48			3.84 5.34		3.7 5.2		V	4.5 6.0	V_{IH} or V_{IL}	$-I_O$ = 4.0 mA $-I_O$ = 5.2 mA
V_{OL}	LOW level output voltage R_{TC} output			0.26 0.26		0.33 0.33		0.4 0.4		4.5 6.0	RS=V_{CC} and MR=GND	I_O = 2.6 mA I_O = 3.3 mA
			0 0 0	0.1 0.1 0.1		0.1 0.1 0.1		0.1 0.1 0.1	V	2.0 4.5 6.0	RS=V_{CC} and MR=GND	I_O = 20 µA I_O = 20 µA I_O = 20 µA

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		74HC								V_{CC} (V)	V_I	OTHER
		+25			−40 to +85		−40 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
V_{OL}	LOW level output voltage C_{TC} output			0.26 0.26		0.33 0.33		0.4 0.4	V	4.5 6.0	RS=V_{IL} and MR=V_{IH}	I_O = 3.2 mA I_O = 4.2 mA
V_{OL}	LOW level output voltage except R_{TC} output		0 0 0	0.1 0.1 0.1		0.1 0.1 0.1		0.1 0.1 0.1	V	2.0 4.5 6.0	V_{IH} or V_{IL}	I_O = 20 µA I_O = 20 µA I_O = 20 µA
V_{OL}	LOW level output voltage except R_{TC} and C_{TC} outputs			0.26 0.26		0.33 0.33		0.4 0.4	V	4.5 6.0	V_{IH} or V_{IL}	I_O = 4.0 mA I_O = 5.2 mA
$\pm I_I$	input leakage current			0.1		1.0		1.0	µA	6.0	V_{CC} or GND	
I_{CC}	quiescent supply current			8.0		80.0		160.0	µA	6.0	V_{CC} or GND	I_O = 0

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} (V)	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/ t_{PLH}	propagation delay RS to Q_3		99 36 29	300 60 51		375 75 64		450 90 77	ns	2.0 4.5 6.0	Fig.12
t_{PHL}/ t_{PLH}	propagation delay Q_n to Q_{n+1}		22 8 6	80 16 14		100 20 17		120 24 20	ns	2.0 4.5 6.0	Fig.14
t_{PHL}	propagation delay MR to Q_n		55 20 16	175 35 30		220 44 37		265 53 45	ns	2.0 4.5 6.0	Fig.13
t_{THL}/ t_{TLH}	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig.12
t_W	clock pulse width RS; HIGH or LOW	80 16 14	17 6 5		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig.12
t_W	master reset pulse width MR; HIGH	80 16 14	25 9 7		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig.13
t_{rem}	removal time MR to RS	100 20 17	28 10 8		125 25 21		150 30 26		ns	2.0 4.5 6.0	Fig.13
f_{max}	maximum clock pulse frequency	6.0 30 35	26 80 95		4.8 24 28		4.0 20 24		MHz	2.0 4.5 6.0	Fig.12

DC CHARACTERISTICS FOR 74HCT

Output capability: standard (except for R_{TC} and C_{TC})

I_{CC} category: MSI

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS		
		74HCT								V_{CC} (V)	V_I	OTHER
		+25			−40 to +85		−40 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
V_{IH}	HIGH level input voltage	2.0			2.0		2.0		V	4.5 to 5.5		note 2
V_{IL}	LOW level input voltage			0.8		0.8		0.8	V	4.5 to 5.5		note 2
V_{OH}	HIGH level output voltage R_{TC} output	3.98			3.84		3.7		V	4.5	RS=GND and MR=GND	$-I_O$ = 2.6 mA
		3.98			3.84		3.7		V	4.5	RS = V_{CC} and MR = V_{CC}	$-I_O$ = 0.65 mA
		4.4	4.5		4.4		4.4		V	4.5	RS=GND and MR=GND	$-I_O$ = 20 μA
		4.4	4.5		4.4		4.4		V	4.5	RS=V_{CC} and MR=V_{CC}	$-I_O$ = 20 μA
V_{OH}	HIGH level output voltage C_{TC} output	3.98			3.84		3.7		V	4.5	RS = V_{IH} and MR = V_{IL}	$-I_O$ = 3.2 mA
V_{OH}	HIGH level output voltage except R_{TC} output	4.4	4.5		4.4		4.4		V	4.5	V_{IH} or V_{IL}	$-I_O$ = 20 μA
V_{OH}	HIGH level output voltage except R_{TC} and C_{TC} outputs	3.98			3.84		3.7		V	4.5	V_{IH} or V_{IL}	$-I_O$ = 4.0 mA
V_{OL}	LOW level output voltage R_{TC} output			0.26		0.33		0.4	V	4.5	RS=V_{CC} and MR=GND	I_O = 2.6 mA
			0	0.1		0.1		0.1	V	4.5	RS=V_{CC} and MR=GND	I_O = 20 μA
V_{OL}	LOW level output voltage C_{TC} output			0.26		0.33		0.4	V	4.5	RS = V_{IL} and MR = V_{IH}	I_O = 3.2 mA
V_{OL}	LOW level output voltage except R_{TC} output		0	0.1		0.1		0.1	V	4.5	V_{IH} or V_{IL}	I_O = 20 μA
V_{OL}	LOW level output voltage except R_{TC} and C_{TC} outputs			0.26		0.33		0.4	V	4.5	V_{IH} or V_{IL}	I_O = 4.0 mA
±I	input leakage current			0.1		1.0		1.0	μA	5.5	V_{CC} or GND	
I_{CC}	quiescent supply current			8.0		80.0		160.0	μA	5.5	V_{CC} or GND	I_O = 0
ΔI_{CC}	additional quiescent supply current per input pin for unit load coefficient is 1 (note 1)		100	360		450		490	μA	4.5 to 5.5	V_{CC} – 2.1 V	other inputs at V_{CC} or GND; I_O = 0

Notes

1. The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given here. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.
2. Only input MR (pin 12) has TTL input switching levels for the HCT versions.

INPUT	UNIT LOAD COEFFICIENT
MR	0.40

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} (V)	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/ t_{PLH}	propagation delay RS to Q_3		33	66		83		99	ns	4.5	Fig.12
t_{PHL}/ t_{PLH}	propagation delay Q_n to Q_{n+1}		8	16		20		24	ns	4.5	Fig.14
t_{PHL}	propagation delay MR to Q_n		21	44		55		66	ns	4.5	Fig.13
t_{THL}/ t_{TLH}	output transition time		7	15		19		22	ns	4.5	Fig.12
t_W	clock pulse width RS; HIGH or LOW	16	6		20		24		ns	4.5	Fig.12
t_W	master reset pulse width MR; HIGH	16	6		20		24		ns	4.5	Fig.13
t_{rem}	removal time MR to RS	26	13		33		39		ns	4.5	Fig.13
f_{max}	maximum clock pulse frequency	30	80		24		20		MHz	4.5	Fig.12

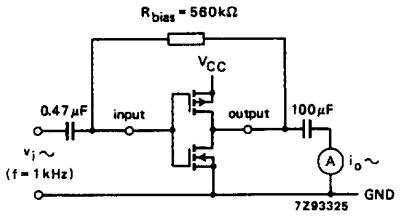


Fig.7 Test set-up for measuring forward transconductance $g_{fs} = di_o / dv_i$ at v_o is constant (see also graph Fig.8); MR = LOW.

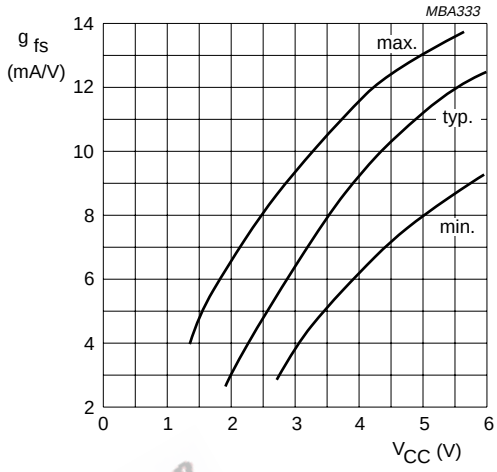


Fig.8 Typical forward transconductance g_{fs} as a function of the supply voltage V_{CC} at T_{amb} = 25 °C.

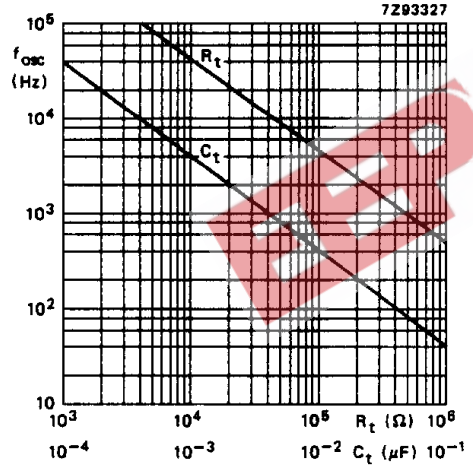
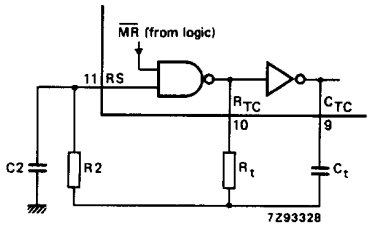


Fig.9 RC oscillator frequency as a function of R_t and C_t at V_{CC} = 2.0 to 6.0 V; T_{amb} = 25 °C. C_t curve at R_t = 100 kΩ; R2 = 200 kΩ. R_t curve at C_t = 1 nF; R2 = 2 × R_t.

RC OSCILLATOR



Typical formula for oscillator frequency:

$$f_{osc} = \frac{1}{2.5 \times R_t \times C_t}$$

Fig.10 Example of a RC oscillator.

TIMING COMPONENT LIMITATIONS

The oscillator frequency is mainly determined by R_tC_t, provided R2 ≈ 2R_t and R2C2 << R_tC_t. The function of R2 is to minimize the influence of the forward voltage across the input protection diodes on the frequency. The stray capacitance C2 should be kept as small as possible. In consideration of accuracy, C_t must be larger than the inherent stray capacitance. R_t must be larger than the "ON" resistance in series with it, which typically is 280 Ω at V_{CC} = 2.0 V, 130 Ω at V_{CC} = 4.5 V and 100 Ω at V_{CC} = 6.0 V.

The recommended values for these components to maintain agreement with the typical oscillation formula are:

C_t > 50 pF, up to any practical value,

10 kΩ < R_t < 1 MΩ.

In order to avoid start-up problems, R_t ≥ 1 kΩ.

TYPICAL CRYSTAL OSCILLATOR

In Fig.11, R2 is the power limiting resistor. For starting and maintaining oscillation a minimum transconductance is necessary, so R2 should not be too large. A practical value for R2 is 2.2 kΩ.

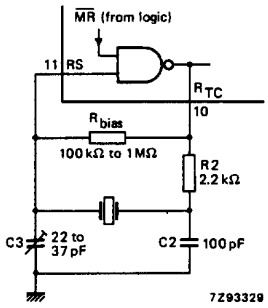
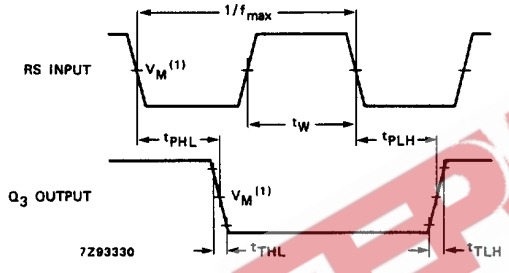


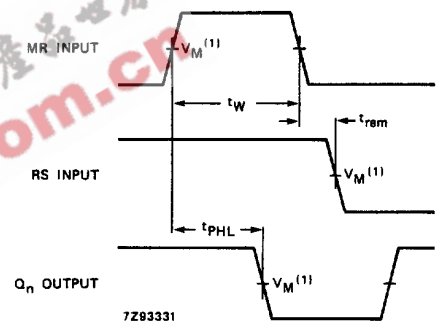
Fig.11 External components connection for a crystal oscillator.

AC WAVEFORMS



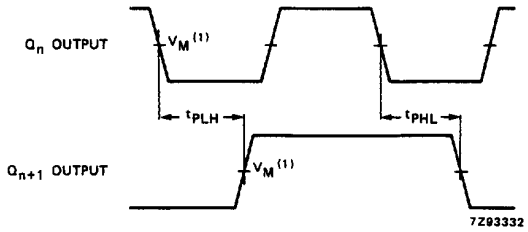
(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

Fig.12 Waveforms showing the clock (RS) to output (Q_3) propagation delays, the clock pulse width, the output transition times and the maximum clock frequency.



(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

Fig.13 Waveforms showing the master reset (MR) pulse width, the master reset to output (Q_n) propagation delays and the master reset to clock (RS) removal time.



(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.

Fig.14 Waveforms showing the output (Q_n) to Q_{n+1} propagation delays.

PACKAGE OUTLINES

See *"74HC/HCT/HCU/HCMOS Logic Package Outlines"*.