

# DATA SHEET

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## 74ABT5074

Synchronizing dual D-type flip-flop with metastable immune characteristics

Product data  
Supersedes data of 1994 Dec 15

2002 Dec 17

# Synchronizing dual D-type flip-flop with metastable immune characteristics

## 74ABT5074

### FEATURES

- Metastable immune characteristics
- Pin compatible with 74F74 and 74F5074
- Typical  $f_{MAX} = 200$  MHz
- Output skew guaranteed less than 2.0 ns
- High source current ( $I_{OH} = 15$  mA) ideal for clock driver applications
- Output capability: +20 mA / -15 mA
- Latch-up protection exceeds 50 0mA per Jedec Std 17
- ESD protection exceeds 2000 V per MIL STD 883 Method 3015 and 200 V per Machine Model

### DESCRIPTION

The 74ABT5074 is a dual positive edge-triggered D-type flip-flop featuring individual data, clock, set and reset inputs; also true and complementary outputs.

Set ( $\overline{SDn}$ ) and reset ( $\overline{RDn}$ ) are asynchronous active-LOW inputs and operate independently of the clock (CPn) input. Data must be stable just one set-up time prior to the LOW-to-HIGH transition of the clock for guaranteed propagation delays.

Clock triggering occurs at a voltage level and is not directly related to the transition time of the positive-going pulse. Following the hold time interval, data at the Dn input may be changed without affecting the levels of the output.

The 74ABT5074 is designed so that the outputs can never display a metastable state due to set-up and hold time violations. If set-up time and hold time are violated the propagation delays may be extended beyond the specifications, but the outputs will not glitch or display a metastable state. Typical metastability parameters for the 74ABT5074 are:

$$\tau \approx 94 \text{ ps and } T_0 \approx 1.3 \times 10^7 \text{ sec}$$

where  $\tau$  represents a function of the rate at which a latch in a metastable state resolves that condition and  $T_0$  represents a function of the measurement of the propensity of a latch to enter a metastable state.

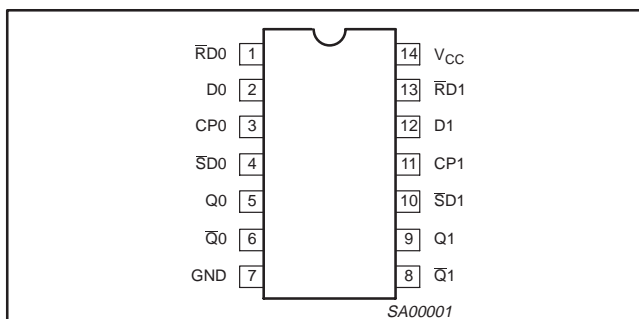
### QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS $T_{amb} = 25^\circ\text{C}; \text{GND} = 0 \text{ V}$	TYPICAL	UNIT
$t_{PLH}$ $t_{PHL}$	Propagation delay CPn to Qn or $\overline{Qn}$	$C_L = 50 \text{ pF}; V_{CC} = 5 \text{ V}$	2.8 2.4	ns
$C_{IN}$	Input capacitance	$V_I = 0 \text{ V or } V_{CC}$	3	pF
$I_{CC}$	Total supply current	Outputs disabled; $V_{CC} = 5.5 \text{ V}$	2	$\mu\text{A}$

### ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	PART NUMBER	DWG NUMBER
14-Pin plastic SO	-40 °C to +85 °C	74ABT5074D	SOT108-1
14-Pin Plastic SSOP Type II	-40 °C to +85 °C	74ABT5074DB	SOT337-1
14-Pin Plastic TSSOP Type I	-40 °C to +85 °C	74ABT5074PW	SOT402-1

### PIN CONFIGURATION



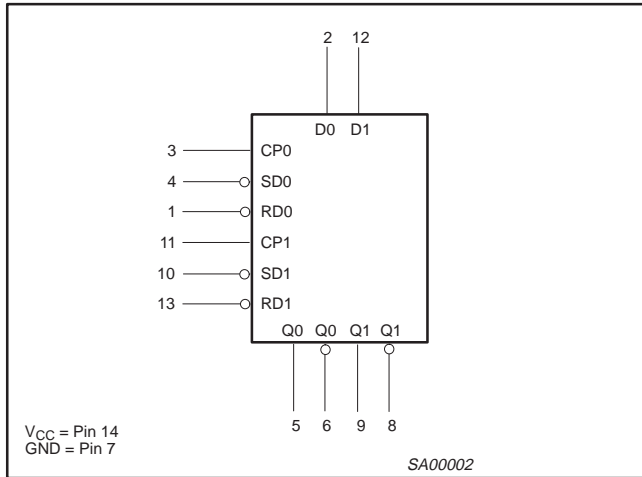
### PIN DESCRIPTION

PIN	SYMBOL	NAME AND FUNCTION
2, 12	D0, D1	Data inputs
3, 11	CP0, CP1	Clock inputs (active rising edge)
4, 10	$\overline{SD0}, \overline{SD1}$	Set inputs (active-LOW)
1, 13	$\overline{RD0}, \overline{RD1}$	Reset inputs (active-LOW)
5, 9	Q0, Q1	Data outputs (active-LOW), non-inverting
6, 8	$\overline{Q0}, \overline{Q1}$	Data outputs (active-LOW), inverting
7	GND	Ground (0 V)
14	$V_{CC}$	Positive supply voltage

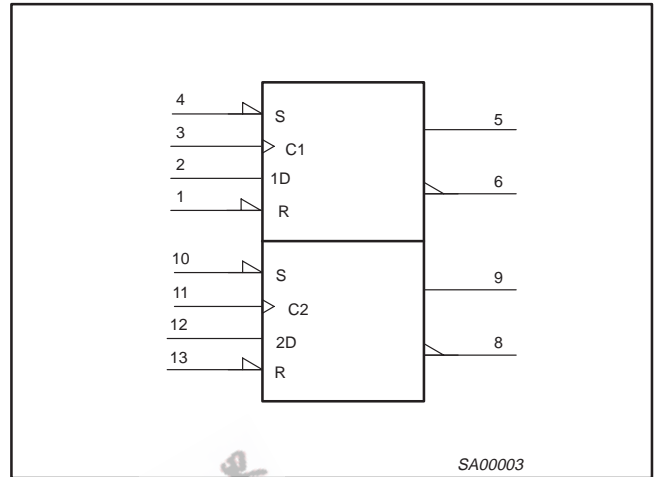
# Synchronizing dual D-type flip-flop with metastable immune characteristics

74ABT5074

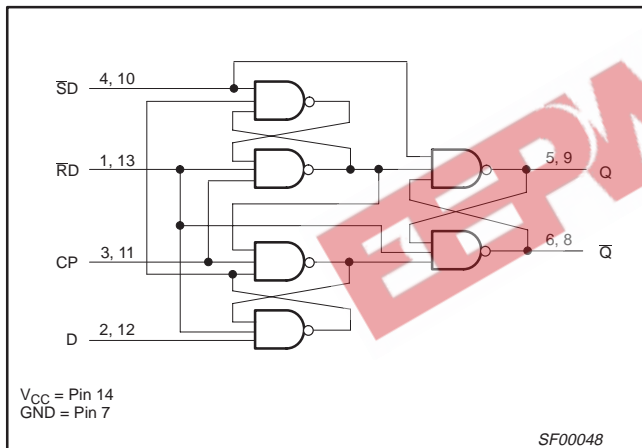
## LOGIC SYMBOL



## IEC/IEEE SYMBOL



## LOGIC DIAGRAM



## FUNCTION TABLE

INPUTS				OUTPUTS		OPERATING MODE
SD	RD	CP	D	Q	Q̄	
L	H	X	X	H	L	Asynchronous set
H	L	X	X	L	H	Asynchronous reset
L	L	X	X	L	H	Undetermined*
H	H	↑	h	H	L	Load "1"
H	H	↑	l	L	H	Load "0"
H	H	↕	X	NC	NC	Hold

### NOTES:

- H = HIGH voltage level
- h = HIGH voltage level one set-up time prior to LOW-to-HIGH clock transition
- L = LOW voltage level
- l = LOW voltage level one set-up time prior to LOW-to-HIGH clock transition
- NC = No change from the previous set-up
- X = Don't care
- ↑ = LOW-to-HIGH clock transition
- ↕ = Not LOW-to-HIGH clock transition
- \* = This set-up is unstable and will change when either set or reset return to the HIGH level

# Synchronizing dual D-type flip-flop with metastable immune characteristics

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## METASTABLE IMMUNE CHARACTERISTICS

Philips Semiconductors uses the term 'metastable immune' to describe characteristics of some of the products in its family. By running two independent signal generators (see Figure 1) at nearly the same frequency (in this case 10 MHz clock and 10.02 MHz data) the device-under-test can often be driven into a metastable state. If the Q output is then used to trigger a digital scope set to infinite persistence the  $\bar{Q}$  output will build a waveform. An experiment was run by continuously operating the devices in the region where metastability will occur.

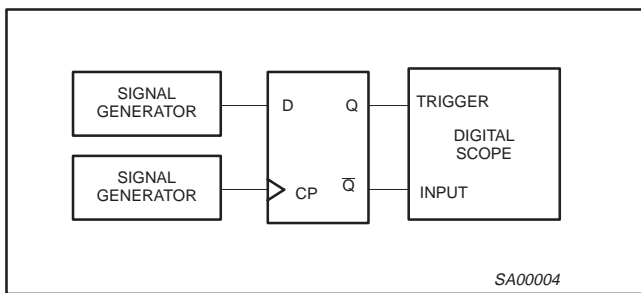


Figure 1. Test Setup

After determining the  $T_0$  and  $\tau$  of the flop, calculating the mean time between failures (MTBF) is simple. Suppose a designer wants to use the 74ABT5074 for synchronizing asynchronous data that is arriving at 10 MHz (as measured by a frequency counter), has a clock frequency of 50 MHz, and has decided that he would like to sample the output of the 74ABT5074 7 nanoseconds after the clock edge. He simply plugs his number into the following equation:

$$MTBF = e^{(t'/\tau)} / T_0 * f_C * f_I$$

In this formula,  $f_C$  is the frequency of the clock,  $f_I$  is the average input event frequency, and  $t'$  is the time after the clock pulse that the output is sampled ( $t' > h$ ,  $h$  being the normal propagation delay). In this situation the  $f_I$  will be twice the data frequency of 20 MHz because input events consist of both of low and high transitions. Multiplying  $f_I$  by  $f_C$  gives an answer of  $10^{15} \text{ Hz}^2$ . From Figure 2 it is clear that the MTBF is greater than  $10^{10}$  seconds. Using the above formula the actual MTBF is  $1.69 \times 10^{10}$  seconds or about 535 years.

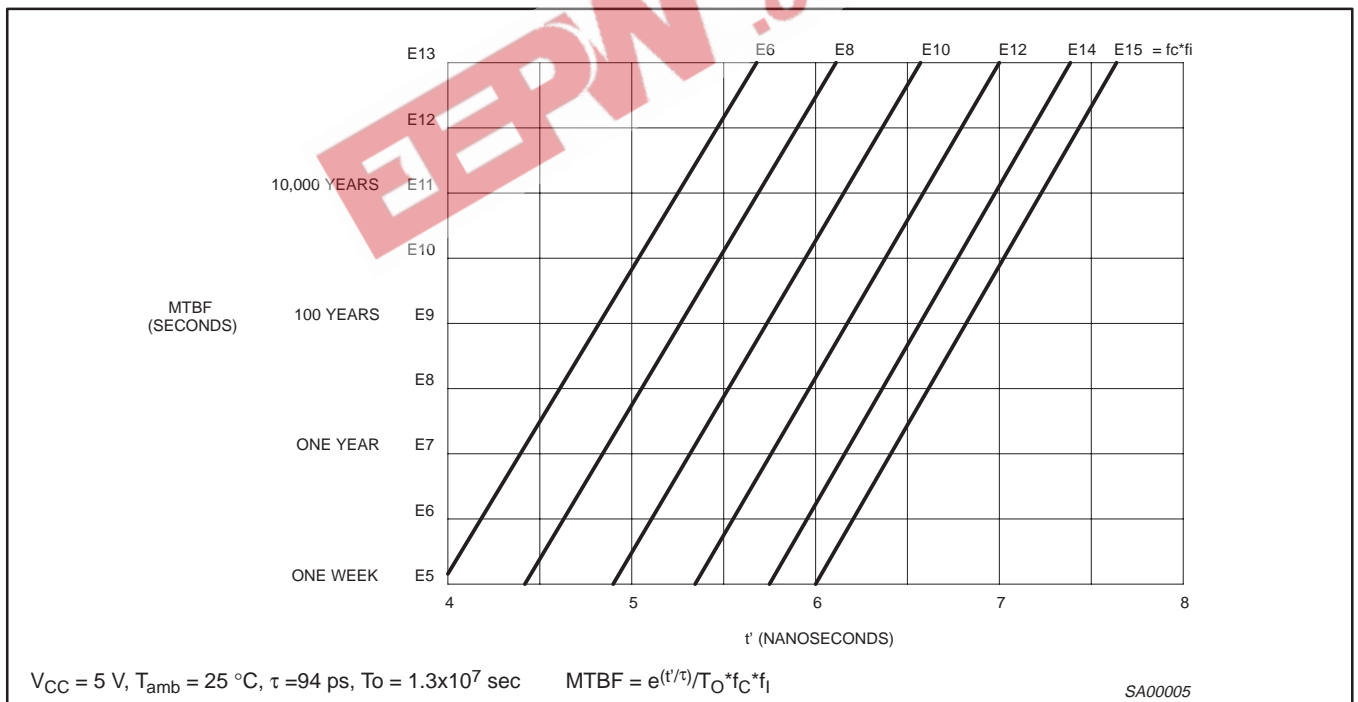


Figure 2. Mean Time Between Failures (MTBF) versus  $t'$

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## TYPICAL VALUES FOR $\tau$ AND $T_0$ AT VARIOUS $V_{CC}$ S AND TEMPERATURES

$V_{CC}$	$T_{amb} = -40\text{ }^{\circ}\text{C}$		$T_{amb} = 25\text{ }^{\circ}\text{C}$		$T_{amb} = 85\text{ }^{\circ}\text{C}$	
	$\tau$	$T_0$	$\tau$	$T_0$	$\tau$	$T_0$
5.5 V	84 ps	$1.0 \times 10^6$ sec	93 ps	$3.8 \times 10^6$ sec	89 ps	$1.5 \times 10^9$ sec
5.0 V	84 ps	$2.7 \times 10^8$ sec	94 ps	$1.3 \times 10^7$ sec	106 ps	$2.2 \times 10^6$ sec
4.5 V	89 ps	$1.0 \times 10^9$ sec	103 ps	$2.1 \times 10^7$ sec	115 ps	$4.4 \times 10^6$ sec

## ABSOLUTE MAXIMUM RATINGS<sup>1, 2</sup>

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
$V_{CC}$	DC supply voltage		-0.5 to +7.0	V
$I_{IK}$	DC input diode current	$V_I < 0$ V	-18	mA
$V_I$	DC input voltage <sup>3</sup>		-1.2 to +7.0	V
$I_{OK}$	DC output diode current	$V_O < 0$ V	-50	mA
$V_{OUT}$	DC output voltage <sup>3</sup>	Output in Off or HIGH state	-0.5 to +5.5	V
$I_{OUT}$	DC output current	Output in LOW state	40	mA
$T_{stg}$	Storage temperature range		-65 to 150	$^{\circ}\text{C}$

### NOTES:

- Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150  $^{\circ}\text{C}$ .
- The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

## RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
$V_{CC}$	DC supply voltage	4.5	5.5	V
$V_I$	Input voltage	0	$V_{CC}$	V
$V_{IH}$	HIGH-level input voltage	2.0	-	V
$V_{IL}$	LOW-level Input voltage	-	0.8	V
$I_{OH}$	HIGH-level output current	-	-15	mA
$I_{OL}$	LOW-level output current	-	20	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	10	ns/V
$T_{amb}$	Operating free-air temperature range	-40	+85	$^{\circ}\text{C}$

# Synchronizing dual D-type flip-flop with metastable immune characteristics

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## DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T <sub>amb</sub> = +25 °C			T <sub>amb</sub> = -40 °C to +85 °C		
			MIN	TYP	MAX	MIN	MAX	
V <sub>IK</sub>	Input clamp voltage	V <sub>CC</sub> = 4.5 V; I <sub>IK</sub> = -18 mA	-	-0.9	-1.2	-	-1.2	V
V <sub>OH</sub>	HIGH-level output voltage	V <sub>CC</sub> = 4.5 V; I <sub>OH</sub> = -15 mA; V <sub>I</sub> = V <sub>IL</sub> or V <sub>IH</sub>	2.5	2.9	-	2.5	-	V
V <sub>OL</sub>	LOW-level output voltage	V <sub>CC</sub> = 4.5 V; I <sub>OL</sub> = 20 mA; V <sub>I</sub> = V <sub>IL</sub> or V <sub>IH</sub>	-	0.35	0.5	-	0.5	V
I <sub>I</sub>	Input leakage current	V <sub>CC</sub> = 5.5 V; V <sub>I</sub> = GND or 5.5 V	-	±0.01	±1.0	-	±1.0	μA
I <sub>OFF</sub>	Power-off leakage current	V <sub>CC</sub> = 0.0 V; V <sub>O</sub> or V <sub>I</sub> ≤ 4.5 V	-	±5.0	±100	-	±100	μA
I <sub>O</sub>	Output current <sup>1</sup>	V <sub>CC</sub> = 5.5 V; V <sub>O</sub> = 2.5 V	-50	-75	-180	-50	-180	mA
I <sub>CC</sub>	Quiescent supply current	V <sub>CC</sub> = 5.5 V; V <sub>I</sub> = GND or V <sub>CC</sub>	-	2	50	-	50	μA
ΔI <sub>CC</sub>	Additional supply current per input pin <sup>2</sup>	V <sub>CC</sub> = 5.5 V; one input at 3.4 V, other inputs at V <sub>CC</sub> or GND	-	0.25	500	-	500	μA

### NOTES:

- Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
- This is the increase in supply current for each input at 3.4 V.

## AC CHARACTERISTICS

GND = 0 V, t<sub>R</sub> = t<sub>F</sub> = 2.5 ns, C<sub>L</sub> = 50 pF, R<sub>L</sub> = 500 Ω

SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			T <sub>amb</sub> = +25 °C V <sub>CC</sub> = +5.0 V			T <sub>amb</sub> = -40 °C to +85 °C V <sub>CC</sub> = +5.0 V ±0.5 V		
			MIN	TYP	MAX	MIN	MAX	
f <sub>max</sub>	Maximum clock frequency	1	180	250	-	150	-	ns
t <sub>pLH</sub> t <sub>pHL</sub>	Propagation delay CPn to Qn or Q̄n	1	1.0 1.0	2.8 2.4	3.9 3.5	1.0 1.0	4.5 3.7	ns
t <sub>pLH</sub> t <sub>pHL</sub>	Propagation delay SDn, RDn to Qn or Q̄n	2	1.0 1.0	3.5 3.1	4.6 4.2	1.0 1.0	5.5 4.7	ns
t <sub>sk(o)</sub>	Output skew <sup>1, 2</sup> CPn to Qn to Q̄n	4	-	-	1.5	-	2.0	ns

### NOTES:

- | t<sub>pN</sub> actual - t<sub>pM</sub> actual | for any output compared to any other output where N and M are either LH or HL.
- Skew times are valid only under same test conditions (temperature, V<sub>CC</sub>, loading, etc.).

## AC SET-UP REQUIREMENTS

GND = 0 V, t<sub>R</sub> = t<sub>F</sub> = 2.5 ns, C<sub>L</sub> = 50 pF, R<sub>L</sub> = 500 Ω

SYMBOL	PARAMETER	WAVEFORM	LIMITS			UNIT
			T <sub>amb</sub> = +25 °C V <sub>CC</sub> = +5.0 V		T <sub>amb</sub> = -40 °C to +85 °C V <sub>CC</sub> = +5.0 V ±0.5 V	
			MIN	TYP	MIN	
t <sub>s</sub> (H) t <sub>s</sub> (L)	Set-up time, HIGH or LOW Dn to CPn	1	2.5 2.5	1.5 1.5	2.5 2.5	ns
t <sub>h</sub> (H) t <sub>h</sub> (L)	Hold time, HIGH or LOW Dn to CPn	1	0 0	-1.4 -1.4	0 0	ns
t <sub>w</sub> (H) t <sub>w</sub> (L)	CPn pulse width, HIGH or LOW	1	1.5 2.4	0.6 1.8	1.5 2.9	ns
t <sub>w</sub> (L)	SDn or RDn pulse width, LOW	2	2.0	1.3	2.2	ns
t <sub>rec</sub>	Recovery time SDn or RDn to CPn	3	2.4	1.3	2.8	ns

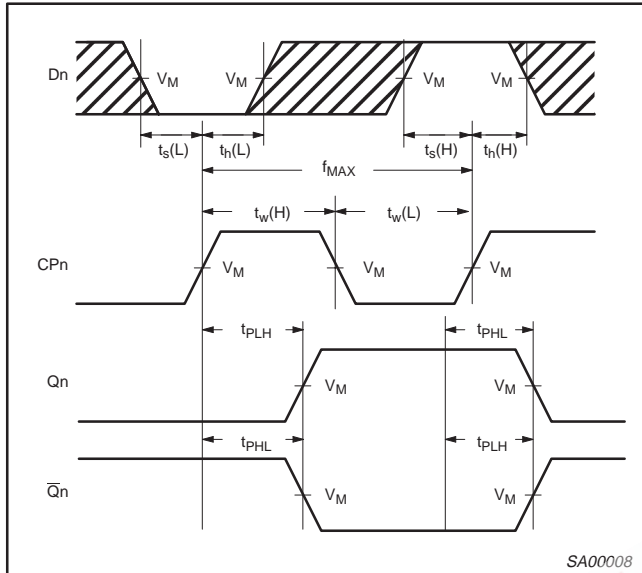
# Synchronizing dual D-type flip-flop with metastable immune characteristics

74ABT5074

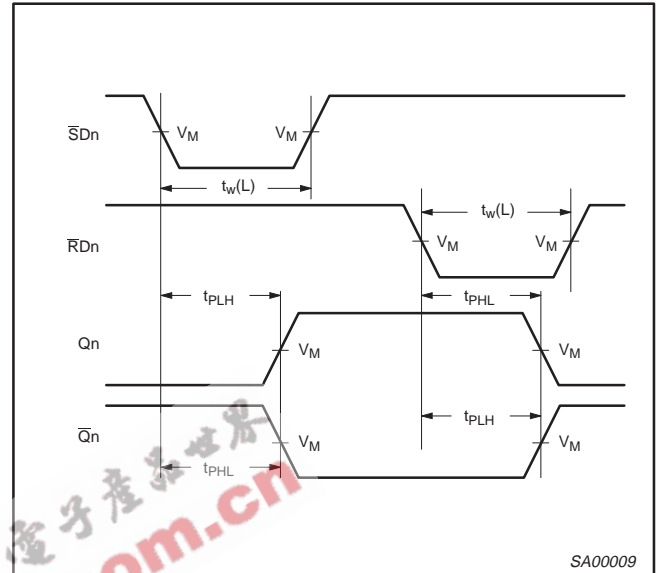
## AC WAVEFORMS

$V_M = 1.5\text{ V}$ ,  $V_{IN} = \text{GND to } 3.0\text{ V}$

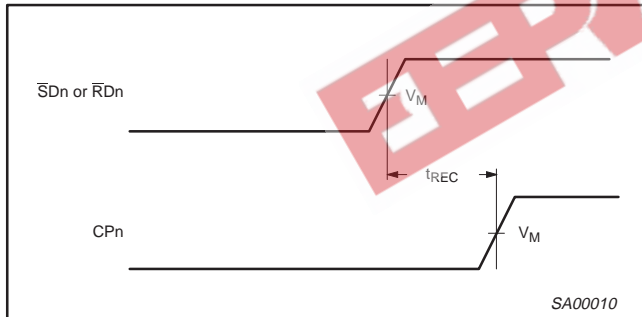
The shaded areas indicate when the input is permitted to change for the predictable output performance.



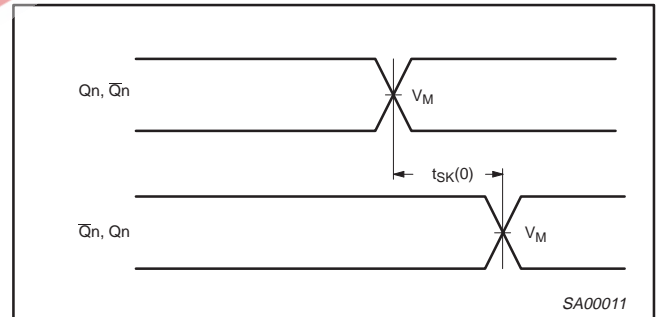
Waveform 1. Propagation Delay for Data to Output, Data Set-up Time and Hold Time, and Clock Width



Waveform 2. Propagation Delay for Set and Reset to Output, Set and Reset Pulse Width



Waveform 3. Recovery Time for Set or Reset to Output

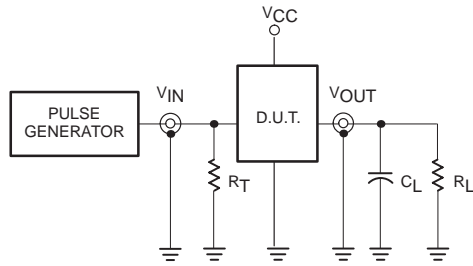


Waveform 4. Output Skew

# Synchronizing dual D-type flip-flop with metastable immune characteristics

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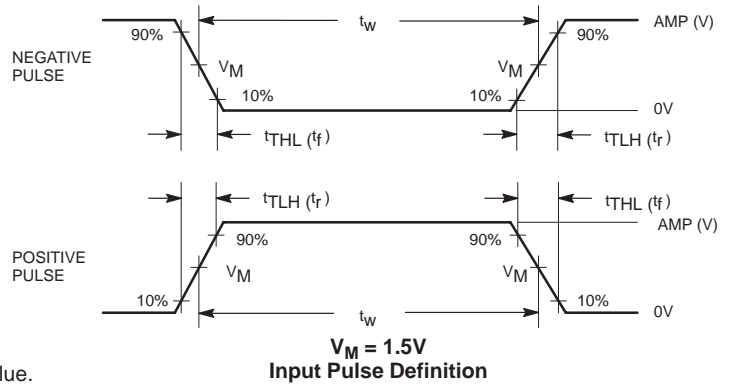
## TEST CIRCUIT AND WAVEFORM



Test Circuit for 3-State Outputs

**DEFINITIONS:**

- $R_L$  = Load resistor; see AC CHARACTERISTICS for value.
- $C_L$  = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.
- $R_T$  = Termination resistance should be equal to  $Z_{OUT}$  of pulse generators.



FAMILY	INPUT PULSE REQUIREMENTS				
	amplitude	rep. rate	$t_w$	$t_R$	$t_F$
74ABT	3.0V	1MHz	500ns	2.5ns	2.5ns

SA00058

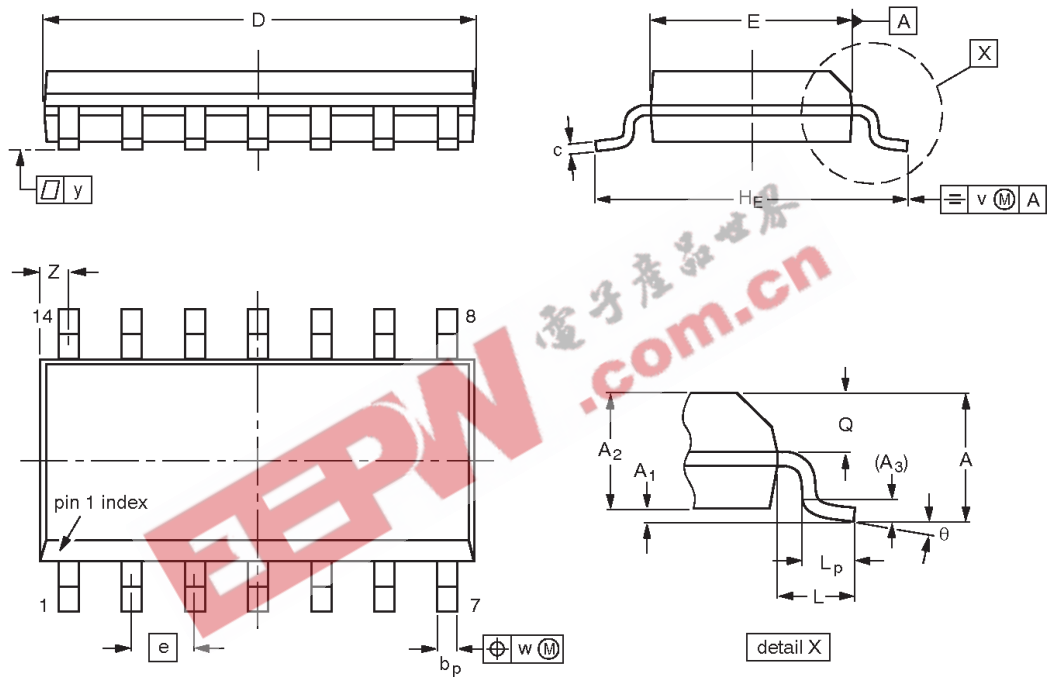


# Synchronizing dual D-type flip-flop with metastable immune characteristics

74ABT5074

SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1



**DIMENSIONS (inch dimensions are derived from the original mm dimensions)**

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	Z <sup>(1)</sup>	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	8.75 8.55	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.35 0.34	0.16 0.15	0.050	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

**Note**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

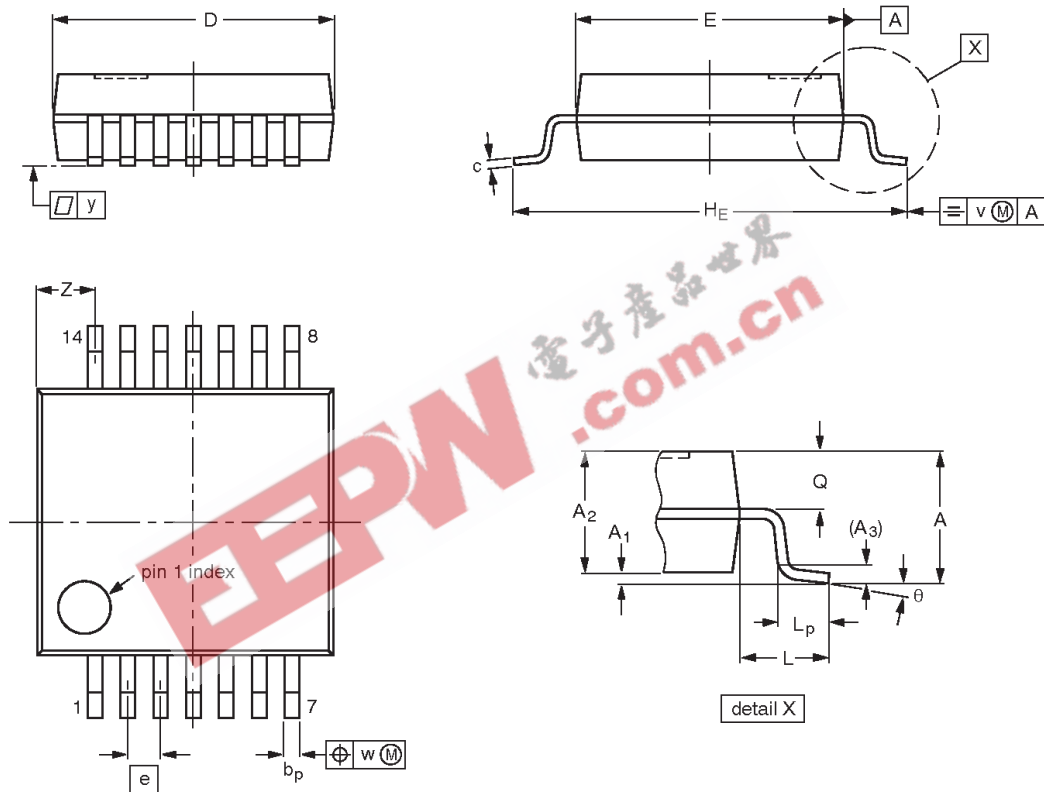
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT108-1	076E06	MS-012				97-05-22 99-12-27

Synchronizing dual D-type flip-flop  
with metastable immune characteristics

74ABT5074

SSOP14: plastic shrink small outline package; 14 leads; body width 5.3 mm

SOT337-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	Z <sup>(1)</sup>	θ
mm	2.0	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	6.4 6.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	1.4 0.9	8° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

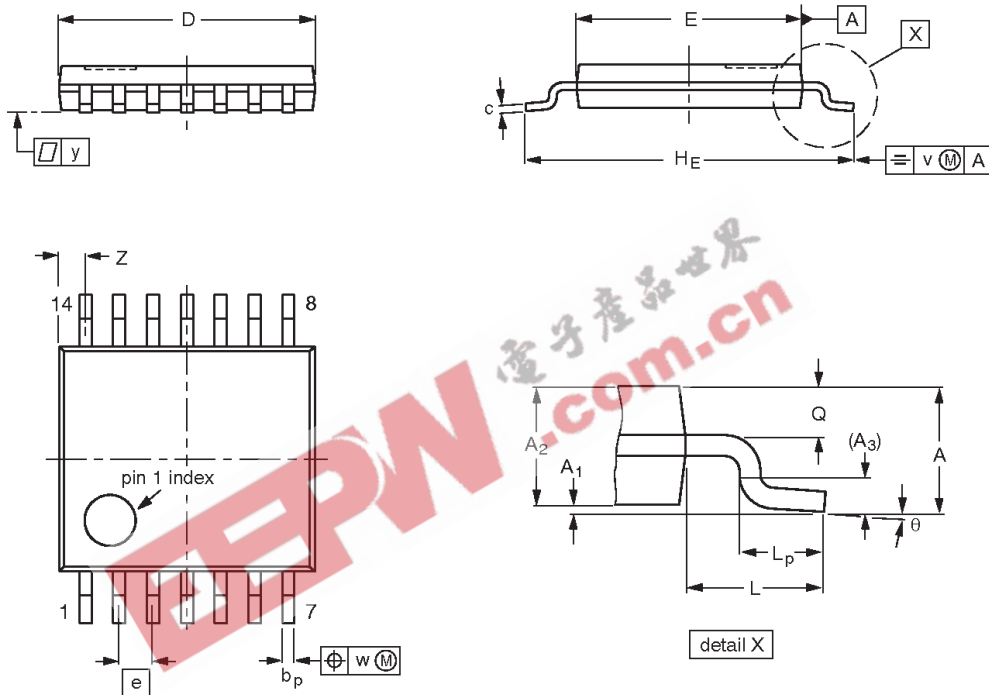
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT337-1		MO-150				<del>96-01-16</del> 99-12-27

# Synchronizing dual D-type flip-flop with metastable immune characteristics

74ABT5074

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm

SOT402-1



**DIMENSIONS (mm are the original dimensions)**

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(2)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	Z <sup>(1)</sup>	θ
mm	1.10	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1.0	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.72 0.38	8° 0°

**Notes**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT402-1		MO-153				-95-04-04 99-12-27

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**Synchronizing dual D-type flip-flop  
with metastable immune characteristics**

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**74ABT5074****REVISION HISTORY**

Rev	Date	Description
_2	20021217	<b>Product data (9397 750 10847); ECN 853-1775 29293 of 12 December 2002. Supersedes data of 15 December 1994.</b> Modifications: <ul style="list-style-type: none"><li>• Ordering information table: remove 74ABT5074N package offering.</li></ul>
_1	19941215	<b>Product specification. ECN 853-1775 14470 of 15 December 1994.</b>

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74ABT5074

## Data sheet status

Level	Data sheet status <sup>[1]</sup>	Product status <sup>[2]</sup> <sup>[3]</sup>	Definitions
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
III	Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Relevant changes will be communicated via a Customer Product/Process Change Notification (CPCN).

[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL <http://www.semiconductors.philips.com>.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

## Definitions

**Short-form specification** — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

**Limiting values definition** — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

**Application information** — Applications that are described herein for any of these products are for illustrative purposes only. Philips Semiconductors make no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

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Date of release: 12-02

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