

74F269 8-Bit Bidirectional Binary Counter

General Description

The 74F269 is a fully synchronous 8-stage up/down counter featuring a preset capability for programmable operation, carry lookahead for easy cascading and a U/\bar{D} input to control the direction of counting. All state changes, whether in counting or parallel loading, are initiated by the rising edge of the clock.

Features

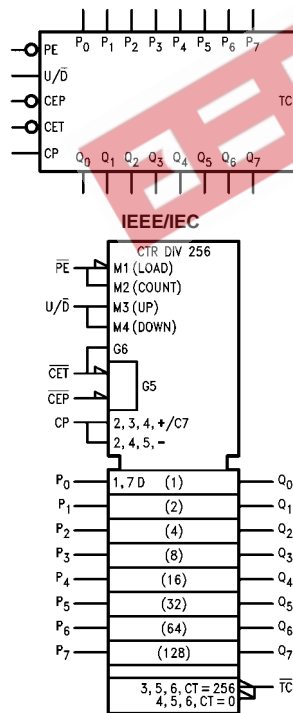
- Synchronous counting and loading
- Built-in lookahead carry capability
- Count frequency 100 MHz
- Supply current 113 mA typ
- 300 mil slimline package

Ordering Code:

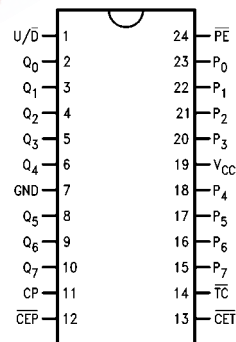
Order Number	Package Number	Package Description
74F269SC	M24B	24-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide
74F269SPC	N24C	24-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Logic Symbols



Connection Diagram



Function Table

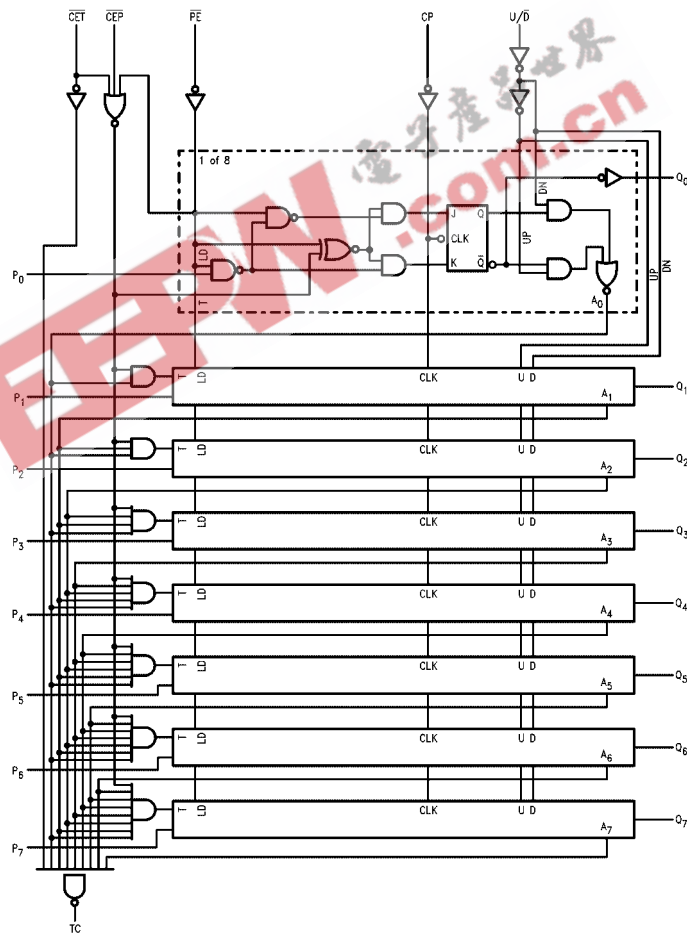
$\bar{P}\bar{E}$	$\bar{C}E\bar{P}$	$\bar{C}E\bar{T}$	U/\bar{D}	CP	Function
L	X	X	X	↗	Parallel Load All Flip-Flops
H	H	X	X	↗	Hold
H	X	H	X	↗	Hold ($\bar{T}C$ Held HIGH)
H	L	L	H	↗	Count Up
H	L	L	L	↗	Count Down

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
↗ = Transition LOW-to-HIGH

Unit Loading/Fan Out

Pin Names	Description	U.L.	
		HIGH/LOW	Input I_{IH}/I_{IL} Output I_{OH}/I_{OL}
P_0 – P_7	Parallel Data Inputs	1.0/1.0	20 μ A/–0.6 mA
\overline{PE}	Parallel Enable Input (Active LOW)	1.0/1.0	20 μ A/–0.6 mA
U/\overline{D}	Up-Down Count Control Input	1.0/1.0	20 μ A/–0.6 mA
\overline{CEP}	Count Enable Parallel Input (Active LOW)	1.0/1.0	20 μ A/–0.6 mA
\overline{CET}	Count Enable Trickle Input (Active LOW)	1.0/1.0	20 μ A/–0.6 mA
CP	Clock Input	1.0/1.0	20 μ A/–0.6 mA
\overline{TC}	Terminal Count Output (Active LOW)	5.0/33.3	–1 mA/20 mA
Q_0 – Q_7	Flip-Flop Outputs	50/33.3	–1 mA/20 mA

Logic Diagram



Absolute Maximum Ratings (Note 1)

Storage Temperature	-65°C to +150°C
Ambient Temperature under Bias	-55°C to +125°C
Junction Temperature under Bias	-55°C to +150°C
V _{CC} Pin Potential to Ground Pin	-0.5V to +7.0V
Input Voltage (Note 2)	-0.5V to +7.0V
Input Current (Note 2)	-30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V _{CC} = 0V)	
Standard Output	-0.5V to V _{CC}
3-STATE Output	-0.5V to +5.5V
Current Applied to Output in LOW State (Max)	twice the rated I _{OL} (mA)

Recommended Operating Conditions

Free Air Ambient Temperature	0°C to +70°C
Supply Voltage	+4.5V to +5.5V

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

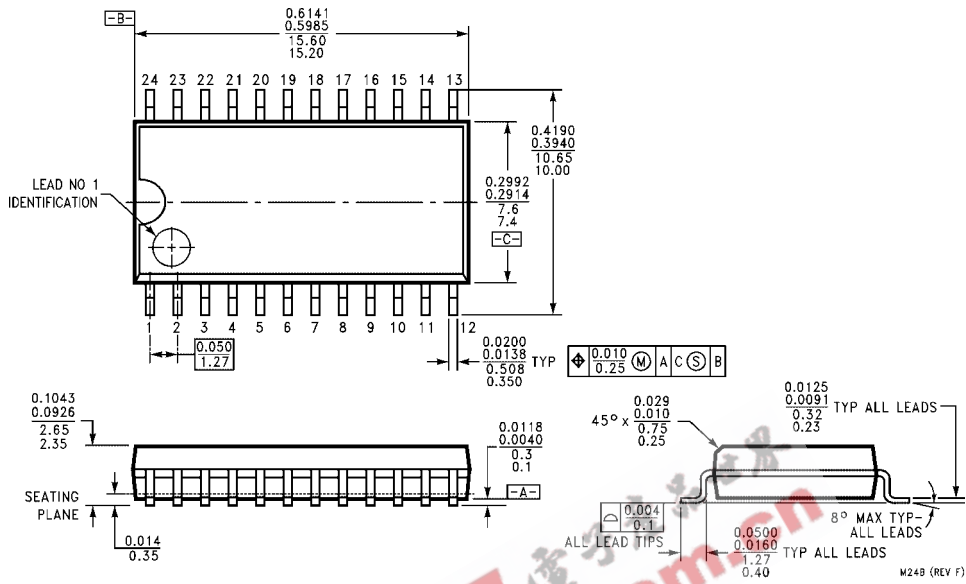
DC Electrical Characteristics

Symbol	Parameter	Min	Typ	Max	Units	V _{CC}	Conditions
V _{IH}	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V _{IL}	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V _{CD}	Input Clamp Diode Voltage			-1.2	V	Min	I _{IN} = -18 mA
V _{OH}	Output HIGH Voltage	10% V _{CC}	2.5		V	Min	I _{OH} = -1 mA
		5% V _{CC}	2.7		V	Min	I _{OH} = -1 mA
V _{OL}	Output LOW Voltage	10% V _{CC}		0.5	V	Min	I _{OL} = 20 mA
I _{IH}	Input HIGH Current			5.0	μA	Max	V _{IN} = 2.7V
I _{BVI}	Input HIGH Current Breakdown Test			7.0	μA	Max	V _{IN} = 7.0V
I _{CEX}	Output HIGH Leakage Current			50	μA	Max	V _{OUT} = V _{CC}
V _{ID}	Input Leakage Test	4.75			V	0.0	I _{ID} = 1.9 μA, All Other Pins Grounded
I _{OD}	Output Leakage Circuit Current			3.75	μA	0.0	V _{IOD} = 150 mV All Other Pins Grounded
I _{IL}	Input LOW Current			-0.6	mA	Max	V _{IN} = 0.5V
I _{OS}	Output Short-Circuit Current	-60		-150	mA	Max	V _{OUT} = 0V
I _{CCH}	Power Supply Current		104	125	mA	Max	V _O = HIGH
I _{CCL}	Power Supply Current		113	135	mA	Max	V _O = LOW

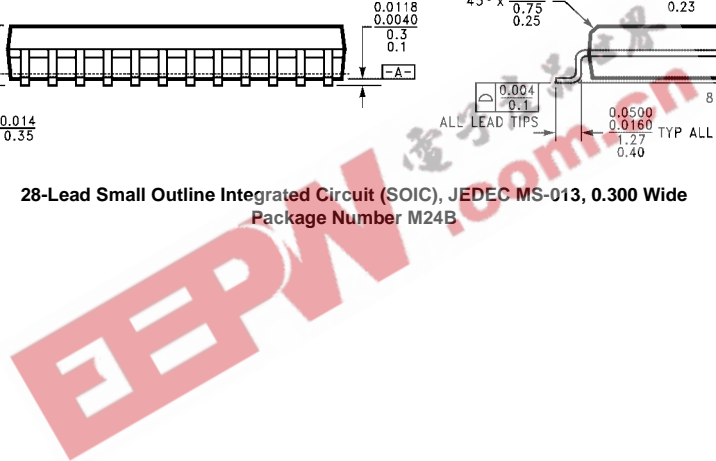
AC Electrical Characteristics							
Symbol	Parameter	T _A = +25°C V _{CC} = +5.0V C _L = 50 pF			T _A = 0°C to +70°C V _{CC} = 5.0V C _L = 50 pF		Units
		Min	Typ	Max	Min	Max	
t _{MAX}	Maximum Clock Frequency	100			85		MHz
t _{PLH}	Propagation Delay	3.5		8.0	3.5	7.0	ns
t _{PHL}	CP to Q _n (Count-Up)	4.5		10.5	4.5	11.0	
t _{PLH}	Propagation Delay	3.5		7.5	3.5	10.0	ns
t _{PHL}	U/D to \overline{TC}	4.5		7.5	4.5	11.0	
t _{PLH}	Propagation Delay	3.5		7.0	3.5	10.5	ns
t _{PHL}	CET to \overline{TC}	3.0		10.5	3.0	11.5	
t _{PLH}	Propagation Delay	4.5		10.0	4.5	10.5	ns
t _{PHL}	CP to \overline{TC}	5.0		10.0	4.5	10.5	
t _{PLH}	Propagation Delay	3.5		10.5	3.5	11.0	ns
t _{PHL}	CP to Q _n (Count-Down)	4.5		10.5	4.5	11.0	
t _{PLH}	Propagation Delay	3.5		7.0	3.5	10.0	ns
t _{PHL}	CP to Q _n (Load)	4.0		7.0	4.0	7.0	

AC Operating Requirements						
Symbol	Parameter	T _A = +25°C V _{CC} = +5.0V		T _A = 0°C to +70°C V _{CC} = 5.0V		Units
		Min	Max	Min	Max	
t _S (H)	Setup Time, HIGH or LOW	3.5		4.0		ns
t _S (L)	Data to CP	3.0		3.0		
t _H (H)	Hold Time, HIGH or LOW	1.0		2.0		ns
t _H (L)	Data to CP	1.0		1.0		
t _S (H)	Setup Time, HIGH or LOW	5.5		6.5		ns
t _S (L)	\overline{PE} to CP	5.5		6.5		
t _H (H)	Hold Time, HIGH or LOW	0		0		ns
t _H (L)	\overline{PE} to CP	0		0		
t _S (H)	Setup Time, HIGH or LOW	6.0		6.5		ns
t _S (L)	CET or \overline{CEP} to CP	8.0		9.0		
t _H (H)	Hold Time, HIGH or LOW	0		0		ns
t _H (L)	\overline{CET} or \overline{CEP} to CP	0		0		
t _W (H)	Clock Pulse Width, HIGH or LOW	3.5		3.5		ns
t _W (L)			3.5		4.0	
t _S (H)	Setup Time, HIGH or LOW	8.0		9.5		ns
t _S (L)	U/D to CP	6.0		7.0		
t _H (H)	Hold Time, HIGH or LOW	0.0		0.0		ns
t _H (L)	U/D to CP	0.0		0.0		

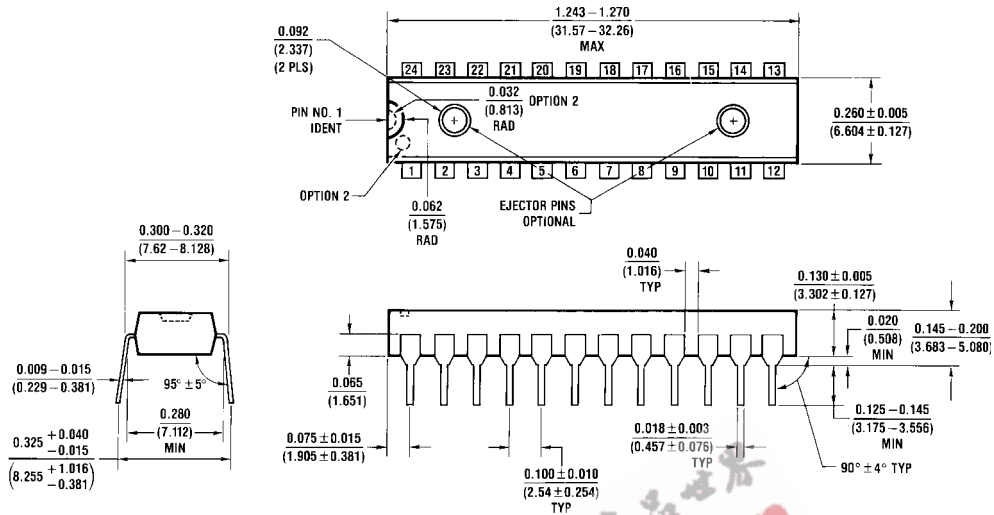
Physical Dimensions inches (millimeters) unless otherwise noted



**28-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide
Package Number M24B**



Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



24-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide Package Number N24C

N24C (REV F)

Fairchild does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied and Fairchild reserves the right at any time without notice to change said circuitry and specifications.

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

www.fairchildsemi.com