HD74HC164

8-bit Parallel-out Shift Register

HITACHI

Description

This 8-bit shift register has gated serial inputs and clear. Each register bit is a D-type master/slave flip-flop. Inputs A & B permit complete control over the incoming data. A low at either or both inputs inhibits entry of new data and resets the first flip-vlop to the low level at the next clock pulse. A high level on the input enables the other input which will then determine the state of the first flip-flop. Data at the serial inputs may be changed while the clock is high or low, but only information meeting the setup and hold time requirements will be entered. Data is serially shifted in and out of the 8-bit register during the positive going transition of the clock pulse. Clear is independent of the clock and accomplished by a low level at the clear input.

Features

- High Speed Operation: t_{pd} (Clock to Q) = 14.5 ns typ (C_L = 50 pF)
- High Output Current: Fanout of 10 LSTTL Loads
- Wide Operating Voltage: V_{CC} = 2 to 6 V
- Low Input Current: 1 µA max
- Low Quiescent Supply Current: I_{CC} (static) = 4 µA max

Function Table

Inputs				Outputs			
Clear	**Clock**	**A**	**B**	**Q_A**	**Q_B**	·····	**Q_H**
L	X	X	X	L	L	·····	L
H	⎍	X	X	Q_{Ao}	Q_{Bo}	·····	Q_{Ho}
H	⎍⎲	L	X	L	Q_{An}	·····	Q_{Gn}
H	⎍⎲	X	L	L	Q_{An}	·····	Q_{Gn}
H	⎍⎲	H	H	H	Q_{An}	·····	Q_{Gn}

Q_{Ao} to Q_{Ho} = Outputs remain unchanged.

Q_{An} to Q_{Gn} = Data shifted from the previous stage on a positive edge at the clock input.

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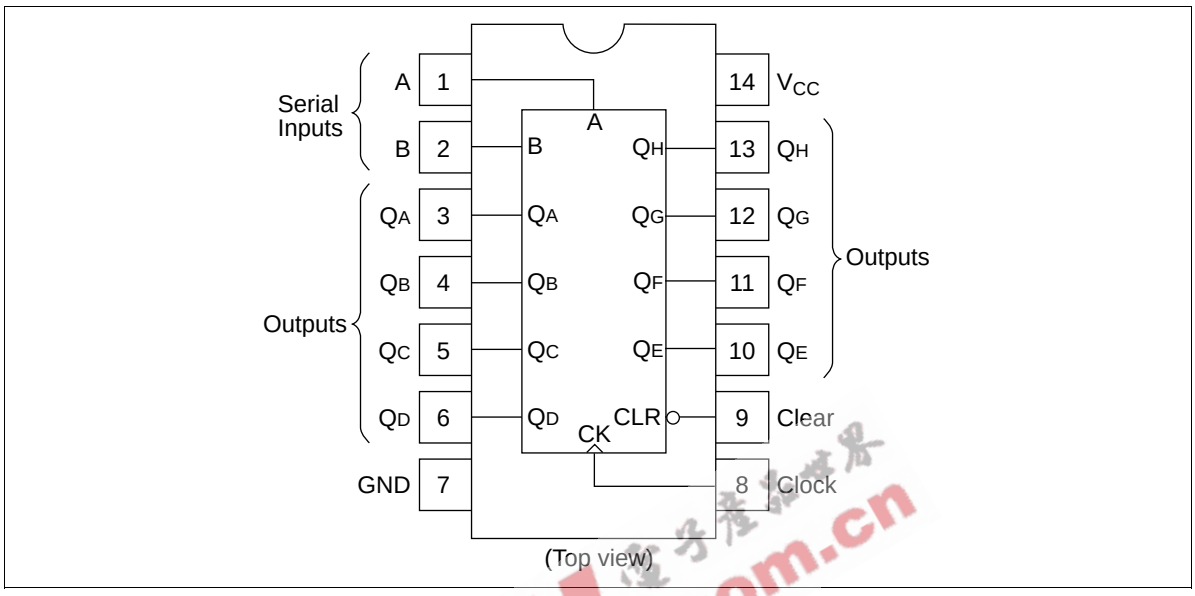
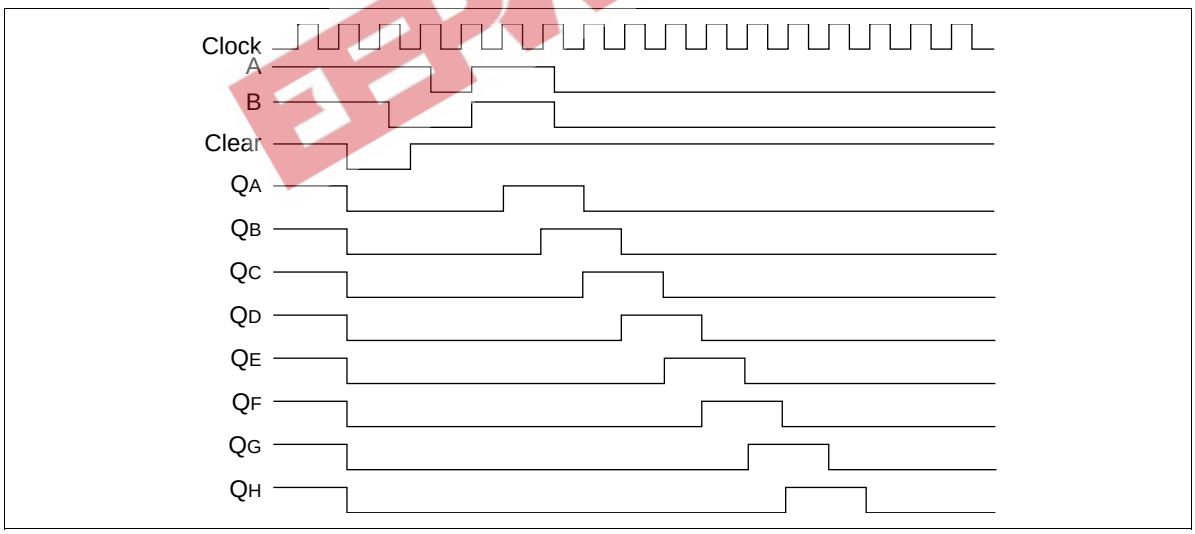
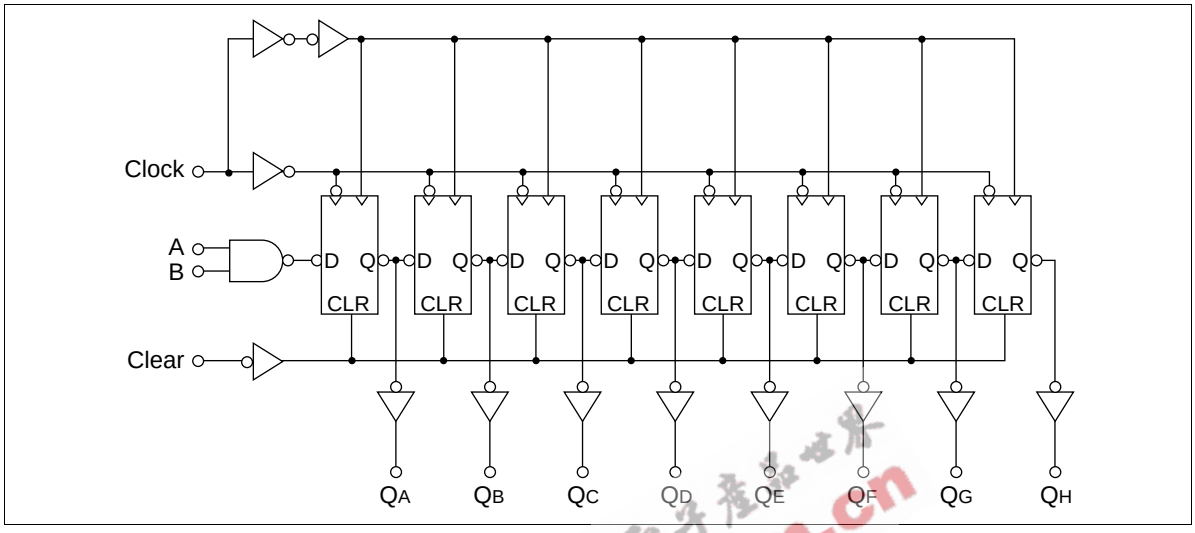
Pin Arrangement



Timing Diagram



Logic Diagram



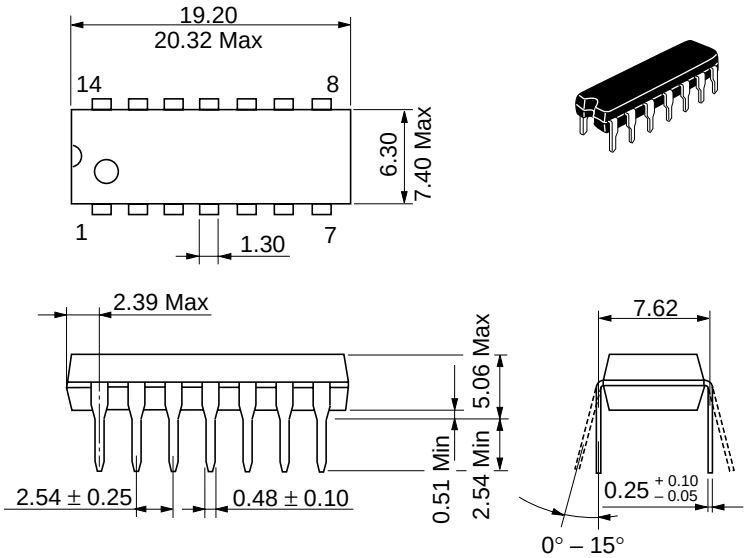
DC Characteristics

Item	Symbol	V_{CC} (V)	Ta = 25°C Min	Typ	Max	Ta = –40 to +85°C Min	Max	Unit	Test Conditions
Input voltage	V_{IH}	2.0	1.5	—	—	1.5	—	V	
		4.5	3.15	—	—	3.15	—		
		6.0	4.2	—	—	4.2	—		
	V_{IL}	2.0	—	—	0.5	—	0.5	V	
		4.5	—	—	1.35	—	1.35		
		6.0	—	—	1.8	—	1.8		
Output voltage	V_{OH}	2.0	1.9	2.0	—	1.9	—	V	Vin = V_{IH} or V_{IL} I_{OH} = –20 µA
		4.5	4.4	4.5	—	4.4	—		
		6.0	5.9	6.0	—	5.9	—		
		4.5	4.18	—	—	4.13	—		I_{OH} = –4 mA
		6.0	5.68	—	—	5.63	—		I_{OH} = –5.2 mA
	V_{OL}	2.0	—	0.0	0.1	—	0.1	V	Vin = V_{IH} or V_{IL} I_{OL} = 20 µA
		4.5	—	0.0	0.1	—	0.1		
		6.0	—	0.0	0.1	—	0.1		
		4.5	—	—	0.26	—	0.33		I_{OL} = 4 mA
		6.0	—	—	0.26	—	0.33		I_{OL} = 5.2 mA
Input current	Iin	6.0	—	—	±0.1	—	±1.0	µA	Vin = V_{CC} or GND
Quiescent supply current	I_{CC}	6.0	—	—	4.0	—	40	µA	Vin = V_{CC} or GND, Iout = 0 µA

AC Characteristics (C_L = 50 pF, Input $t_r = t_f$ = 6 ns)

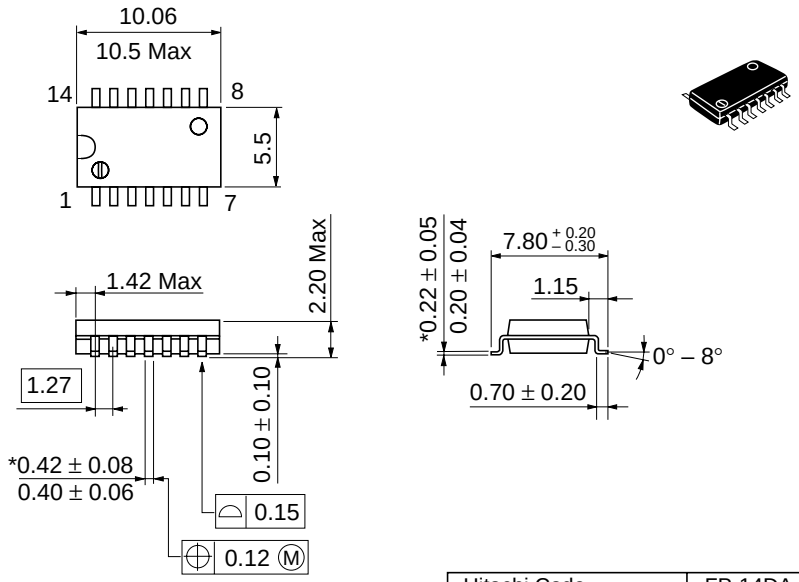
Item	Symbol	V_{cc} (V)	Ta = 25°C			Ta = –40 to +85°C		Unit	Test Conditions
			Min	Typ	Max	Min	Max		
Maximum clock frequency	f_{max}	2.0	—	—	5	—	4	MHz	
		4.5	—	—	25	—	20		
		6.0	—	—	29	—	24		
Propagation delay time	t_{PHL}	2.0	—	—	160	—	200	ns	Clock to Q
		4.5	—	14	32	—	40		
		6.0	—	—	27	—	34		
	t_{PLH}	2.0	—	—	160	—	200	ns	
		4.5	—	15	32	—	40		
		6.0	—	—	27	—	34		
	t_{PHL}	2.0	—	—	175	—	220	ns	Clear to Q
		4.5	—	17	35	—	44		
		6.0	—	—	30	—	37		
Setup time	t_{su}	2.0	100	—	—	125	—	ns	A, B to Clock
		4.5	20	1	—	25	—		
		6.0	17	—	—	21	—		
Hold time	t_h	2.0	5	—	—	5	—	ns	Clock to A, B
		4.5	5	0	—	5	—		
		6.0	5	—	—	5	—		
Removal time	t_{rem}	2.0	5	—	—	5	—	ns	Clear to Clock
		4.5	5	0	—	5	—		
		6.0	5	—	—	5	—		
Pulse width	t_w	2.0	80	—	—	100	—	ns	Clock
		4.5	16	8	—	20	—		
		6.0	14	—	—	17	—		
		2.0	80	—	—	100	—	ns	Clear
		4.5	16	5	—	20	—		
		6.0	14	—	—	17	—		
Output rise/fall time	t_{TLH} t_{THL}	2.0	—	—	75	—	95	ns	
		4.5	—	5	15	—	19		
		6.0	—	—	13	—	16		
Input capacitance	Cin	—	—	5	10	—	10	pF	

Unit: mm



Hitachi Code	DP-14
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	0.97 g

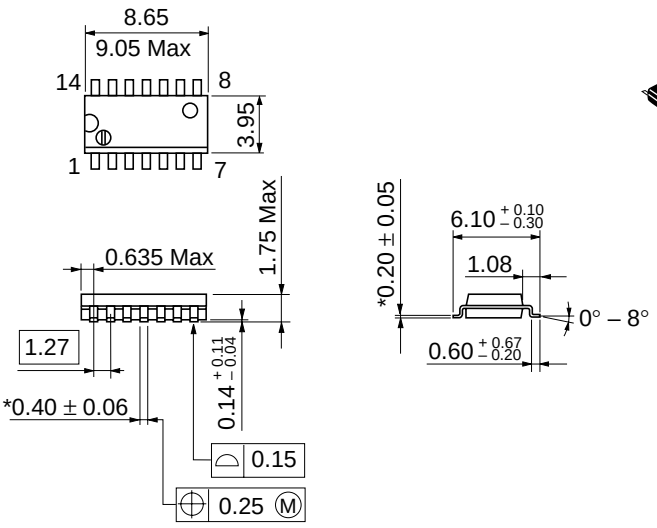
Unit: mm



Hitachi Code	FP-14DA
JEDEC	—
EIAJ	Conforms
Weight (reference value)	0.23 g

*Dimension including the plating thickness
Base material dimension

Unit: mm



Hitachi Code	FP-14DN
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	0.13 g

*Pd plating

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