

# MC74LVX541

## Octal Bus Buffer

The MC74LVX541 is an advanced high speed CMOS octal bus buffer fabricated with silicon gate CMOS technology. It achieves high speed operation similar to equivalent Bipolar Schottky TTL while maintaining CMOS low power dissipation.

The MC74LVX541 is a noninverting type. When either  $\overline{OE1}$  or  $\overline{OE2}$  are high, the terminal outputs are in the high impedance state.

The internal circuit is composed of three stages, including a buffer output which provides high noise immunity and stable output. The inputs tolerate voltages up to 7.0 V, allowing the interface of 5.0 V systems to 3.0 V systems.

### Features

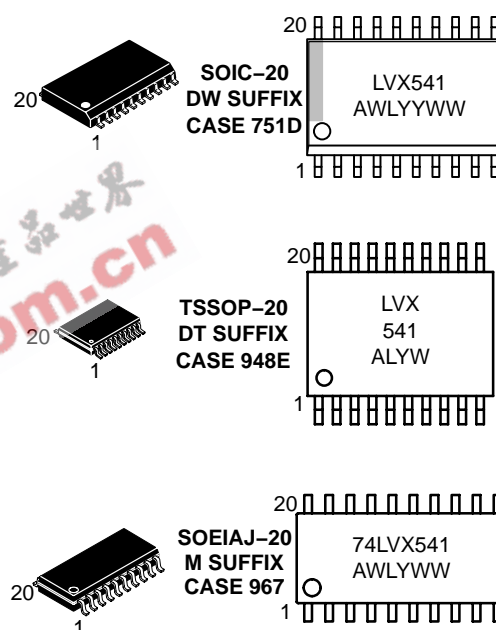
- High Speed:  $t_{PD} = 5.0$  ns (Typ) at  $V_{CC} = 3.3$  V
- Low Power Dissipation:  $I_{CC} = 4$   $\mu$ A (Max) at  $T_A = 25^\circ$ C
- High Noise Immunity:  $V_{NIH} = V_{NIL} = 28\%$   $V_{CC}$
- Power Down Protection Provided on Inputs
- Balanced Propagation Delays
- Designed for 2 V to 3.6 V Operating Range
- Low Noise:  $V_{OLP} = 1.2$  V (Max)
- Pin and Function Compatible with Other Standard Logic Families
- Latchup Performance Exceeds 300 mA
- Chip Complexity: 134 FETs or 33.5 Equivalent Gates
- ESD Performance:
  - Human Body Model > 2000 V;
  - Machine Model > 200 V
- Pb-Free Packages are Available\*



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### MARKING DIAGRAMS



A = Assembly Location  
L, WL = Wafer Lot  
Y, YY = Year  
W, WW = Work Week

### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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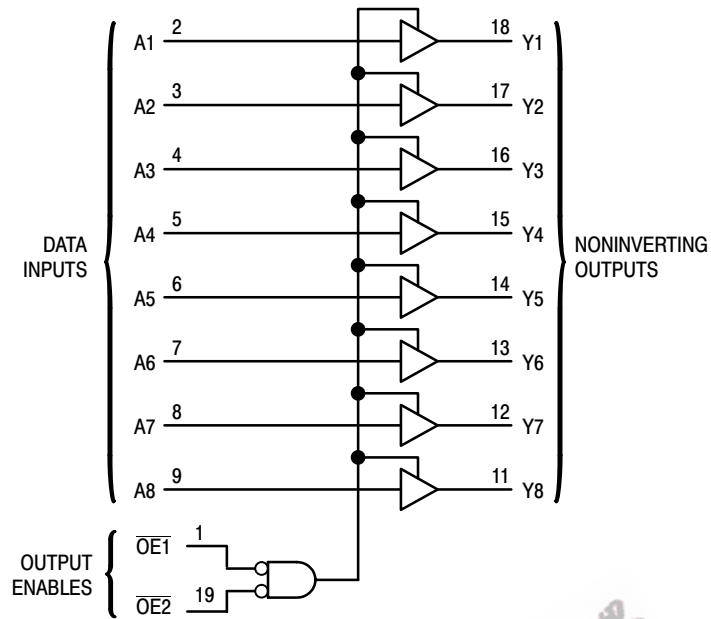


Figure 1. LOGIC DIAGRAM

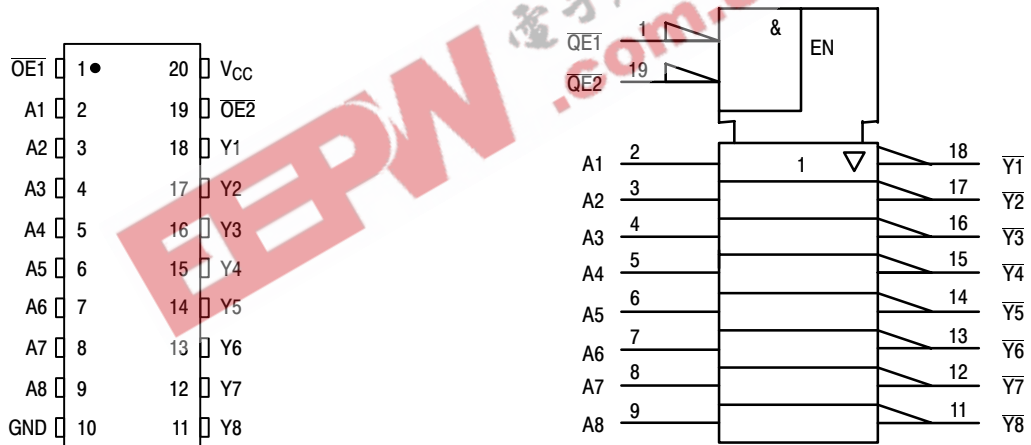


Figure 2. PIN ASSIGNMENT

Figure 3. IEC LOGIC DIAGRAM

## FUNCTION TABLE

Inputs			Output Y
$\overline{OE1}$	$\overline{OE2}$	A	
L	L	L	L
L	L	H	H
H	X	X	Z
X	H	X	Z

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## MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
$V_{CC}$	DC Supply Voltage	- 0.5 to + 7.0	V
$V_{in}$	DC Input Voltage	- 0.5 to + 7.0	V
$V_{out}$	DC Output Voltage	- 0.5 to $V_{CC} + 0.5$	V
$I_{IK}$	Input Diode Current	- 20	mA
$I_{OK}$	Output Diode Current	$\pm 20$	mA
$I_{out}$	DC Output Current, per Pin	$\pm 25$	mA
$I_{CC}$	DC Supply Current, $V_{CC}$ and GND Pins	$\pm 50$	mA
$P_D$	Power Dissipation in Still Air, SOIC Packages† TSSOP Package†	500 450	mW
$T_{stg}$	Storage Temperature	- 65 to + 150	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation,  $V_{in}$  and  $V_{out}$  should be constrained to the range  $GND \leq (V_{in} \text{ or } V_{out}) \leq V_{CC}$ . Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or  $V_{CC}$ ). Unused outputs must be left open.

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

†Derating — SOIC Packages: - 7 mW/°C from 65° to 125°C  
TSSOP Package: - 6.1 mW/°C from 65° to 125°C

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
$V_{CC}$	DC Supply Voltage	2.0	3.6	V
$V_{in}$	DC Input Voltage	0	5.5	V
$V_{out}$	DC Output Voltage	0	$V_{CC}$	V
$T_A$	Operating Temperature, All Package Types	-40	+ 85	°C
$t_r, t_f$	Input Rise and Fall Time $V_{CC} = 3.3V \pm 0.3V$	0	100	ns/V

## DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	$V_{CC}$ V	$T_A = 25^\circ\text{C}$			$T_A = -40 \text{ to } 85^\circ\text{C}$		Unit
				Min	Typ	Max	Min	Max	
$V_{IH}$	Minimum High-Level Input Voltage		2.0 3.0 3.6	1.50 2.0 2.4			1.50 2.0 2.4		V
$V_{IL}$	Maximum Low-Level Input Voltage		2.0 3.0 3.6			0.50 0.80 0.80		0.50 0.80 0.80	V
$V_{OH}$	Minimum High-Level Output Voltage $V_{in} = V_{IH}$ or $V_{IL}$	$I_{OH} = -50 \mu\text{A}$ $I_{OH} = -50 \mu\text{A}$ $I_{OH} = -4 \text{ mA}$	2.0 3.0 3.0	1.9 2.9 2.58	2.0 3.0		1.9 2.9 2.48		V
$V_{OL}$	Maximum Low-Level Output Voltage $V_{in} = V_{IH}$ or $V_{IL}$	$I_{OL} = 50 \mu\text{A}$ $I_{OL} = 50 \mu\text{A}$ $I_{OL} = 4 \text{ mA}$	2.0 3.0 3.0		0.0 0.0	0.1 0.1 0.36		0.1 0.1 0.44	V
$I_{in}$	Maximum Input Leakage Current	$V_{in} = 5.5 \text{ V}$ or GND	0 to 3.6			$\pm 0.1$		$\pm 1.0$	$\mu\text{A}$
$I_{OZ}$	Maximum Three-State Leakage Current	$V_{in} = V_{IL}$ or $V_{IH}$ $V_{out} = V_{CC}$ or GND	3.6			$\pm 0.2$ 5		$\pm 2.5$	$\mu\text{A}$
$I_{CC}$	Maximum Quiescent Supply Current	$V_{in} = V_{CC}$ or GND	3.6			4.0		40.0	$\mu\text{A}$

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## AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 3.0$ ns)

Symbol	Parameter	Test Conditions	$T_A = 25^\circ\text{C}$			$T_A = -40$ to $85^\circ\text{C}$		Unit
			Min	Typ	Max	Min	Max	
$t_{PLH}$ , $t_{PHL}$	Maximum Propagation Delay, A to Y	$V_{CC} = 2.7$ V $C_L = 15$ pF $C_L = 50$ pF		5.0 7.5	7.0 10.5	1.0 1.0	8.5 12.0	ns
		$V_{CC} = 3.3 \pm 0.3$ V $C_L = 15$ pF $C_L = 50$ pF		3.5 5.0	5.0 7.0	1.0 1.0	6.0 8.0	
$t_{PZL}$ , $t_{PZH}$	Output Enable Time, OE to Y	$V_{CC} = 2.7$ V $R_L = 1$ k $\Omega$ $C_L = 15$ pF $C_L = 50$ pF		6.8 9.3	10.5 14.0	1.0 1.0	12.5 16.0	ns
		$V_{CC} = 3.3 \pm 0.3$ V $R_L = 1$ k $\Omega$ $C_L = 15$ pF $C_L = 50$ pF		4.7 6.2	7.2 9.2	1.0 1.0	8.5 10.5	
$t_{PLZ}$ , $t_{PHZ}$	Output Disable Time, OE to Y	$V_{CC} = 2.7$ V $R_L = 1$ k $\Omega$ $C_L = 50$ pF		11.2	15.4	1.0	17.5	ns
		$V_{CC} = 3.3 \pm 0.3$ V $R_L = 1$ k $\Omega$ $C_L = 50$ pF		6.0	8.8	1.0	10.0	
$t_{OSLH}$ , $t_{OSHL}$	Output to Output Skew	$V_{CC} = 2.7$ V (Note 1) $C_L = 50$ pF			1.5		1.5	ns
		$V_{CC} = 3.3 \pm 0.3$ V (Note 1) $C_L = 50$ pF			1.0		1.0	ns
$C_{in}$	Maximum Input Capacitance			4.0	10		10	pF
$C_{out}$	Maximum Three-State Output Capacitance (Output in High Impedance State)			6.0				pF
$C_{PD}$	Power Dissipation Capacitance (Note 2)		Typical @ $25^\circ\text{C}$ , $V_{CC} = 5.0\text{V}$					pF
			18					

- Parameter guaranteed by design.  $t_{OSLH} = |t_{PLHm} - t_{PLHn}|$ ,  $t_{OSHL} = |t_{PHLm} - t_{PHLn}|$ .
- $C_{PD}$  is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation:  $I_{CC(OPR)} = C_{PD} \cdot V_{CC} \cdot f_{in} + I_{CC}/8$  (per bit).  $C_{PD}$  is used to determine the no-load dynamic power consumption;  $P_D = C_{PD} \cdot V_{CC}^2 \cdot f_{in} + I_{CC} \cdot V_{CC}$ .

## NOISE CHARACTERISTICS (Input $t_r = t_f = 3.0$ ns, $C_L = 50$ pF, $V_{CC} = 3.3$ V)

Symbol	Parameter	$T_A = 25^\circ\text{C}$		Unit
		Typ	Max	
$V_{OLP}$	Quiet Output Maximum Dynamic $V_{OL}$	0.5	0.8	V
$V_{OLV}$	Quiet Output Minimum Dynamic $V_{OL}$	-0.5	-0.8	V
$V_{IHD}$	Minimum High Level Dynamic Input Voltage		2.0	V
$V_{ILD}$	Maximum Low Level Dynamic Input Voltage		0.8	V

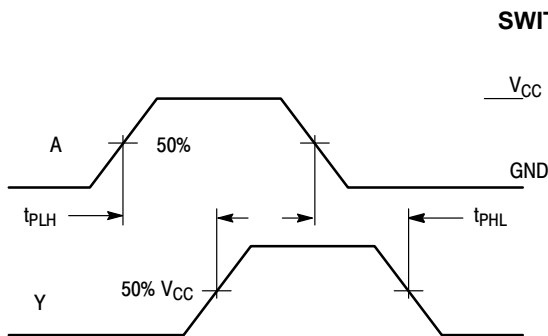


Figure 4.

## SWITCHING WAVEFORMS

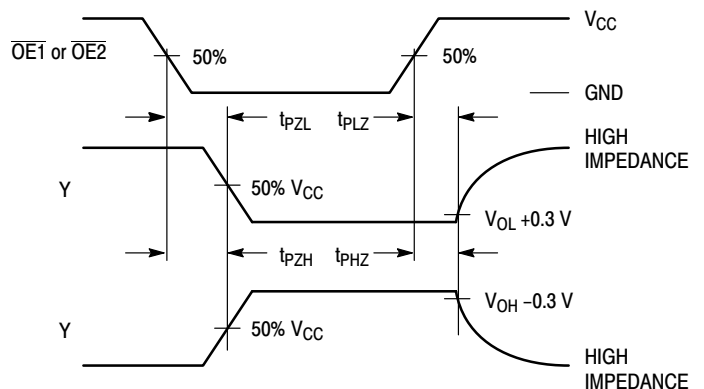
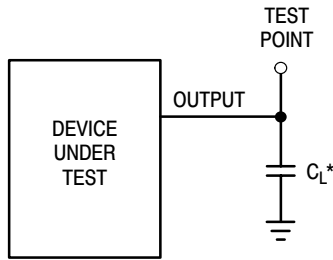


Figure 5.

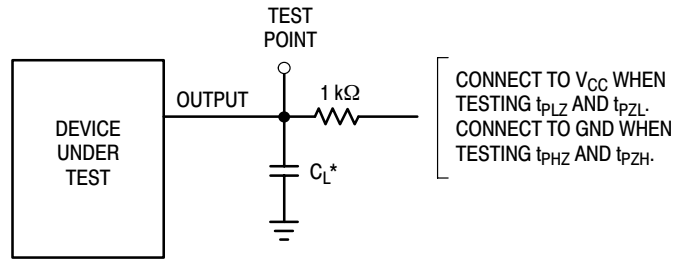
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## TEST CIRCUITS



\*Includes all probe and jig capacitance

Figure 6.



\*Includes all probe and jig capacitance

Figure 7.

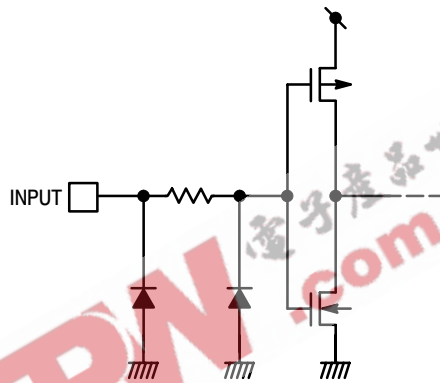


Figure 8. INPUT EQUIVALENT CIRCUIT

## ORDERING INFORMATION

Device	Package	Shipping†
MC74LVX541DW	SOIC-20	38 Units / Rail
MC74LVX541DWG	SOIC-20 (Pb-Free)	38 Units / Rail
MC74LVX541DTR2	TSSOP-20*	2500 Tape & Reel
MC74LVX541M	SOEIAJ-20	40 Units / Rail
MC74LVX541MG	SOEIAJ-20 (Pb-Free)	40 Units / Rail
MC74LVX541MEL	SOEIAJ-20	2000 Tape & Reel
MC74LVX541MELG	SOEIAJ-20 (Pb-Free)	2000 Tape & Reel

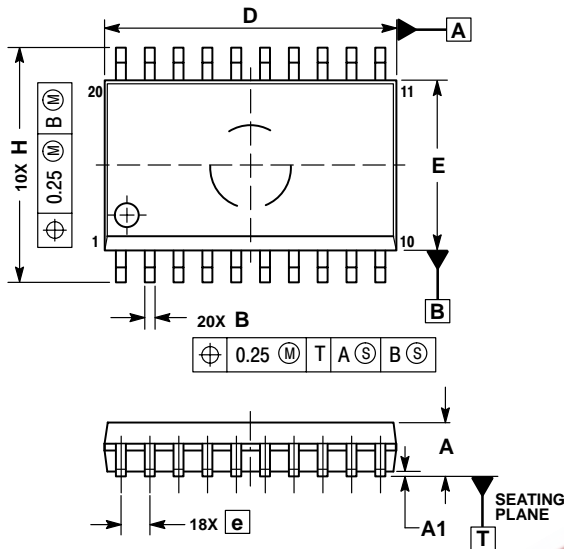
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

\*This package is inherently Pb-Free.

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## PACKAGE DIMENSIONS

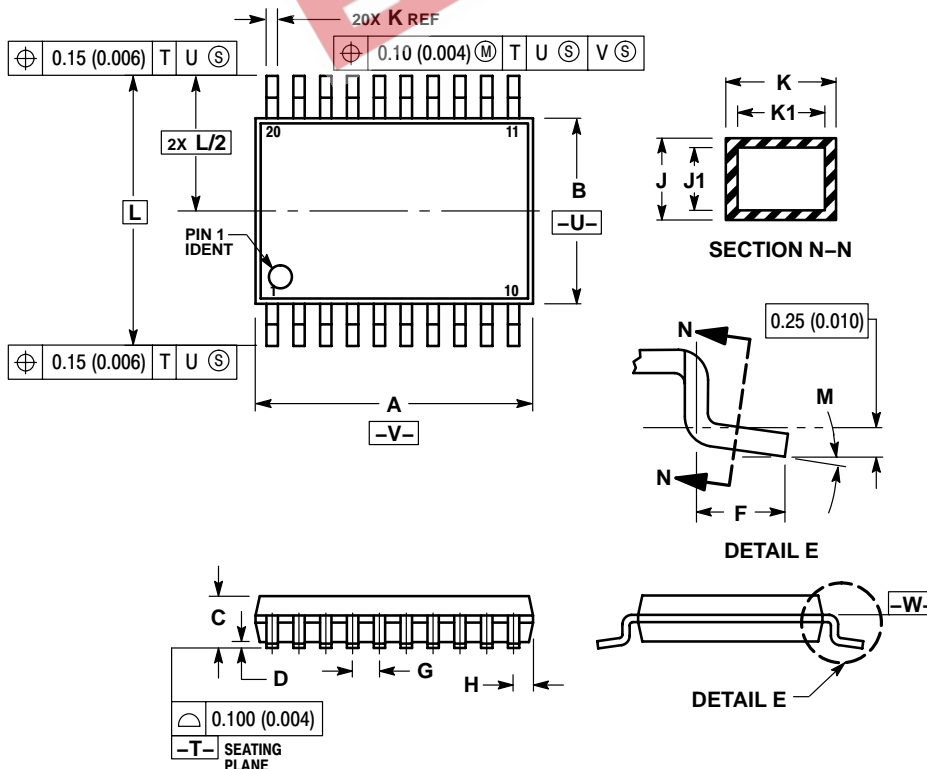
### SOIC-20 DW SUFFIX CASE 751D-05 ISSUE G



- NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
  2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
  3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
  4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
  5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS	
	MIN	MAX
A	2.35	2.65
A1	0.10	0.25
B	0.35	0.49
C	0.23	0.32
D	12.65	12.95
E	7.40	7.60
e	1.27 BSC	
H	10.05	10.55
h	0.25	0.75
L	0.50	0.90
theta	0°	7°

### TSSOP-20 DT SUFFIX CASE 948E-02 ISSUE B



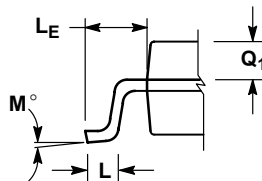
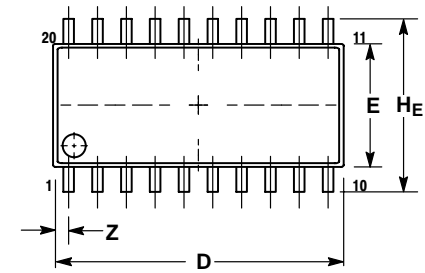
- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: MILLIMETER.
  3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
  4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
  5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
  6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
  7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	6.40	6.60	0.252	0.260
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.27	0.37	0.011	0.015
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

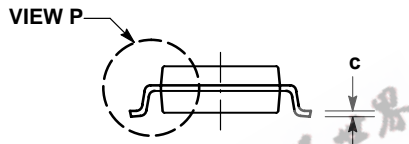
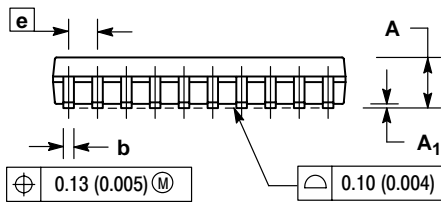
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## PACKAGE DIMENSIONS

SOEIAJ-20  
M SUFFIX  
CASE 967-01  
ISSUE O



DETAIL P




NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
5. THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 (0.018).

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	---	2.05	---	0.081
A <sub>1</sub>	0.05	0.20	0.002	0.008
b	0.35	0.50	0.014	0.020
c	0.18	0.27	0.007	0.011
D	12.35	12.80	0.486	0.504
E	5.10	5.45	0.201	0.215
e	1.27 BSC		0.050 BSC	
H <sub>E</sub>	7.40	8.20	0.291	0.323
L	0.50	0.85	0.020	0.033
L <sub>E</sub>	1.10	1.50	0.043	0.059
M	0°	10°	0°	10°
Q <sub>1</sub>	0.70	0.90	0.028	0.035
Z	---	0.81	---	0.032

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