Document No.	853-1508
ECN No.	00730
Date of Issue	October 17, 1990
Status	Product Specification
ACL Products	

74AC/ACT11160

Synchronous presettable synchronous BCD decade counter, asynchronous reset

FEATURES

- Synchronous counting and loading
- Two count enable inputs for n-bit cascading
- Positive edge-triggered clock
- Asynchronous reset
- Output capability: ±24mA
- CMOS (AC) and TTL (ACT) voltage level inputs
- 50Ω incident wave switching
- Center-pin V_{CC} and ground configuration to minimize high-speed switching noise
- I_{CC} category: MSI

DESCRIPTION

The 74AC/ACT11160 high-performance CMOS devices combine very high speed and high output drive comparable to the most advanced TTL families.

The 74AC/ACT11160 4-bit synchronous presettable decade counters feature an internal carry look-ahead and can be used for high-speed counting. Synchronous operation is provided by having all flip-flops clocked simultaneously on the positive-going edge of the clock.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V; V_{CC} = 5.0V	TYPICAL AC	TYPICAL ACT	UNIT
t_{PLH}/ t_{PHL}	Propagation delay CP_n to Q_n ($\overline{PE}$ = High)	C_L = 50pF	6.9	6.4	ns
C_{PD}	Power dissipation capacitance[1]	f = 1MHz; C_L = 50pF	48	60	pF
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	4.0	4.0	pF
I_{LATCH}	Latch-up current	Per Jedec JC40.2 Standard 17	500	500	mA
f_{MAX}	Maximum clock frequency	C_L = 50pF	140	125	MHz

Note:

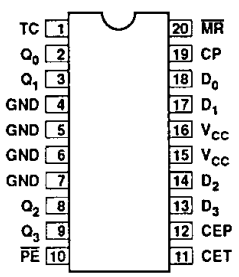
1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_O)$ where:
   f_i = input frequency in MHz, C_L = output load capacitance in pF,
   f_O = output frequency in MHz, V_{CC} = supply voltage in V,
   $\Sigma (C_L \times V_{CC}^2 \times f_O)$ = sum of outputs

ORDERING INFORMATION

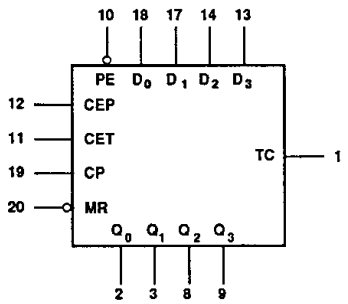
PACKAGES	TEMPERATURE RANGE	ORDER CODE
20-pin plastic DIP (300mil-wide)	-40°C to +85°C	74AC11160N 74ACT11160N
20-pin plastic SOL (300mil-wide)	-40°C to +85°C	74AC11160D 74ACT11160D

PIN CONFIGURATION

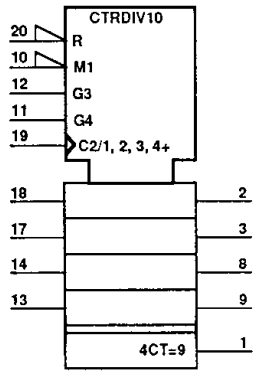
N and D Packages



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



Synchronous presettable synchronous BCD decade counter, asynchronous reset

74AC/ACT11160

The outputs of the counters may be preset to High or Low levels. A Low level at the Parallel Enable ($\overline{PE}$) input disables the counting action and causes the data at the D_0 - D_3 inputs to be loaded into the counter on the rising edge of the clock. Preset takes place regardless of the levels at Count Enable (CEP, CET) inputs.

A Low level at the Master Reset ($\overline{MR}$) input sets all four outputs of the flip-flops (Q_0 - Q_3) to Low levels, regardless of the levels at CP, $\overline{PE}$, CET, and CEP inputs (thus providing an asynchronous clear function).

The carry look-ahead simplifies serial cascading of the counters. Both Count Enable inputs (CEP and CET) must be High to count. The CET input is fed forward to enable the Terminal Count (TC) output. The TC output thus enabled will produce a High output pulse of a duration approximately equal to the High level output of Q_0. This pulse can be used to enable the next cascaded stage.

PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
20	$\overline{MR}$	Asynchronous master reset (active Low)
19	CP	Clock input (Low-to-High, edge-triggered)
18, 17, 14, 13	D_0 - D_3	Data inputs
12	CEP	Count enable input
10	$\overline{PE}$	Parallel enable input (active Low)
11	CET	Count enable carry input
18, 17, 14, 13	Q_0 - Q_3	Counter outputs
1	TC	Terminal count output
4, 5, 6, 7	GND	Ground (0V)
15, 16	V_{CC}	Positive supply voltage

FUNCTION TABLE

OPERATING MODE	INPUTS						OUTPUTS	
	$\overline{MR}$	CP	CEP	CET	$\overline{PE}$	D_n	Q_n	TC
Reset (clear)	L	X	X	X	X	X	L	L
Parallel load	H	↑	X	X	l	l	L	L
	H	↑	X	X	l	h	H	(1)
Count	H	↑	h	h	h	X	count	(1)
Hold (do nothing)	H	X	l	X	h	X	q_n	(1)
	H	X	X	l	h	X	q_n	L

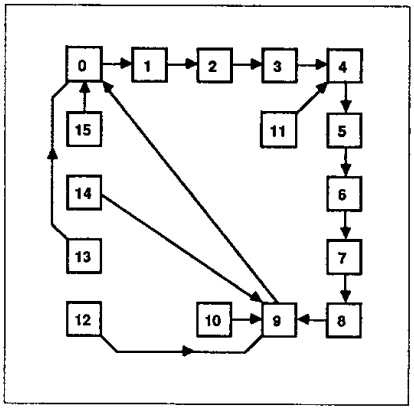
H = High voltage level
L = Low voltage level
h = High voltage level one setup time prior to the Low-to High clock transition
l = Low voltage level one setup time prior to the Low-to High clock transition
X = Don't care
q = State of the referenced output prior to the Low-to High clock transition
↑ = Low-to-High clock transition

NOTE:
1. The TC output is High when CET is High and the counter is at Terminal Count (HLLH).

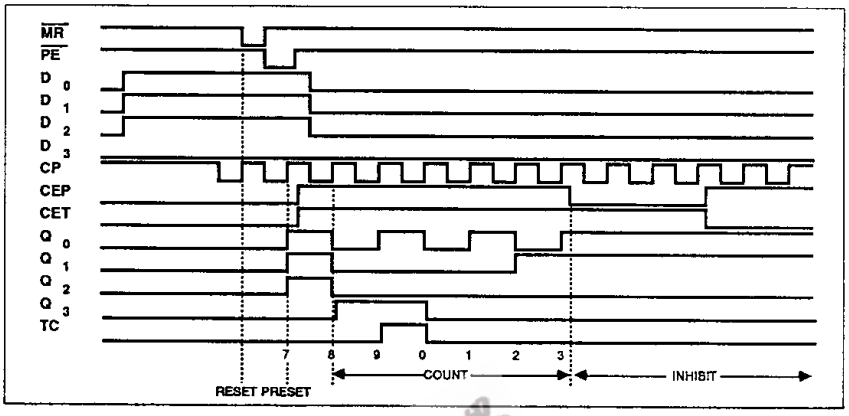
Synchronous presettable synchronous BCD decade counter, asynchronous reset

74AC/ACT11160

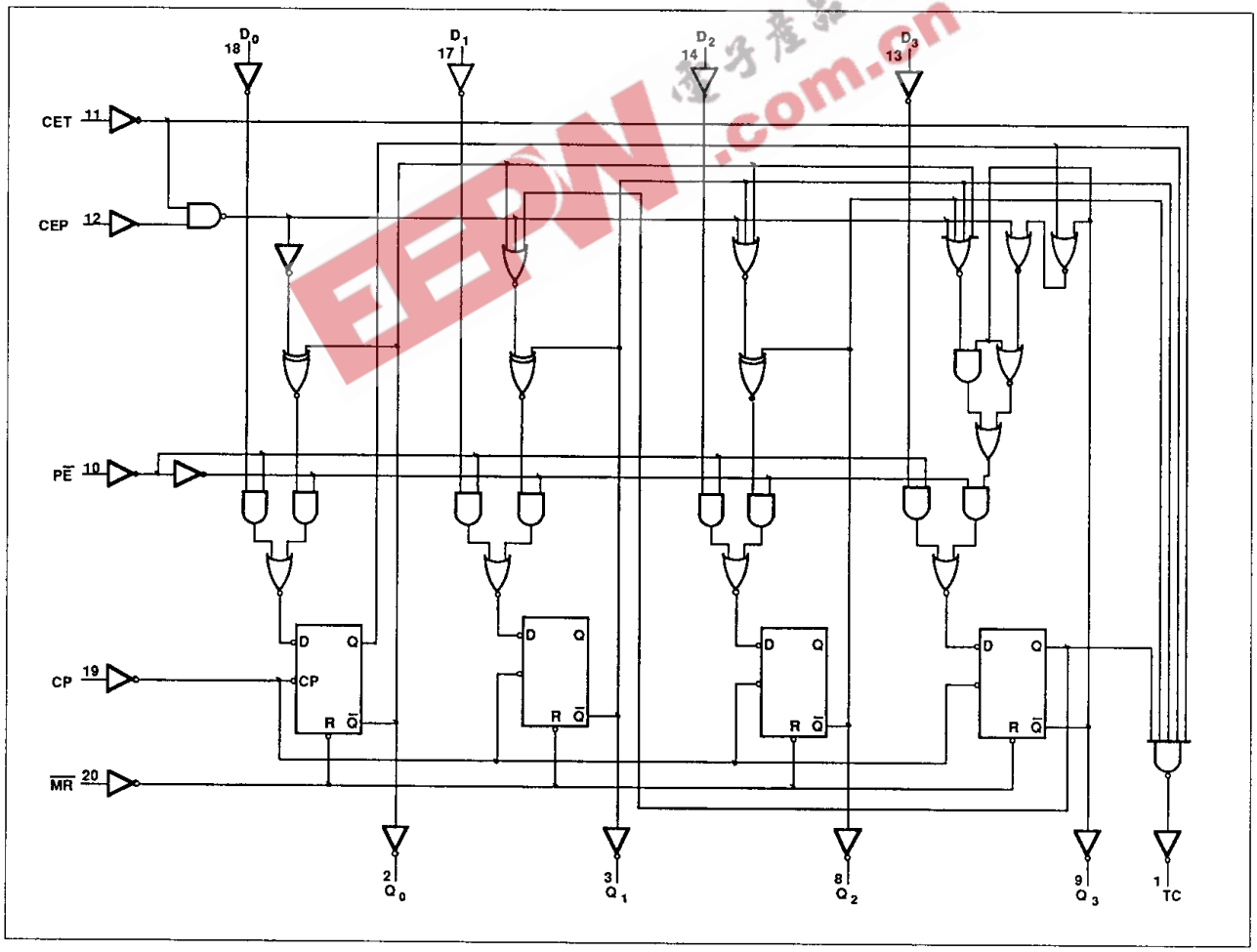
STATE DIAGRAM



TIMING DIAGRAM



LOGIC DIAGRAM



Synchronous presettable synchronous BCD decade counter, asynchronous reset

74AC/ACT11160

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	AC11160			ACT11160			UNIT
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	DC supply voltage	3.0[1]	5.0	5.5	4.5	5.0	5.5	V
V_I	Input voltage	0		V_{CC}	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	0		V_{CC}	V
$\Delta t/\Delta v$	Input transition rise or fall rate	0		10	0		10	ns/V
T_{amb}	Operating free-air temperature range	-40		+85	-40		+85	°C

NOTE:
1. No electrical or switching characteristics are specified at V_{CC} < 3V. Operation between 2V and 3V is not recommended, but within that range, a device output will maintain a previously established logic state.

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	TEST CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 TO +7.0	V
I_{IK} or V_I	DC input diode current[2]	V_I < 0	-20	mA
		V_I > V_{CC}	20	
	DC input voltage		-0.5 to V_{CC} +0.5	V
I_{OK} or V_O	DC output diode current[2]	V_O < 0	-50	mA
		V_O > V_{CC}	50	
	DCoutput voltage		-0.5 to V_{CC} +0.5	V
I_O	DC output source or sink current per output pin	V_O = 0 to V_{CC}	±50	mA
I_{CC} or I_{GND}	DC V_{CC} current		±125	mA
	DC ground current		±125	
T_{STG}	Storage temperature		-65 to 150	°C
P_{TOT}	Power dissipation per package	Above 70°C; derate linearly by 8mW/K	500	mW
	Power dissipation per package Plastic surface mount (SO)	Above 70°C; derate linearly by 8mW/K	400	mW

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

Synchronous presettable synchronous BCD decade counter, asynchronous reset

74AC/ACT11160

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		V_{CC}	74AC11160				74ACT11160				UNIT
					T_{amb} = +25°C		T_{amb} = -40°C to +85°C		T_{amb} = +25°C		T_{amb} = -40°C to +85°C		
				V	Min	Max	Min	Max	Min	Max	Min	Max	
V_{IH}	High-level input voltage			3.0	2.10		2.10						V
				4.5	3.15		3.15		2.0		2.0		
				5.5	3.85		3.85		2.0		2.0		
V_{IL}	Low-level input voltage			3.0		0.90		0.90					V
				4.5		1.35		1.35		0.8		0.8	
				5.5		1.65		1.65		0.8		0.8	
V_{OH}	High-level output voltage	V_I = V_{IL} or V_{IH}	I_{OH} = -50μA	3.0	2.9		2.9						V
				4.5	4.4		4.4		4.4		4.4		
				5.5	5.4		5.4		5.4		5.4		
			I_{OH} = -4mA	3.0	2.58		2.48						
			I_{OH} = -24mA	4.5	3.94		3.8		3.94		3.8		
				5.5	4.94		4.8		4.94		4.8		
			I_{OH} = -75mA[1]	5.5			3.85				3.85		
V_{OL}	Low-level output voltage	V_I = V_{IL} or V_{IH}	I_{OL} = 50μA	3.0		0.1		0.1					V
				4.5		0.1		0.1		0.1		0.1	
				5.5		0.1		0.1		0.1		0.1	
			I_{OL} = 12mA	3.0		0.36		0.44					
			I_{OL} = 24mA	4.5		0.36		0.44		0.36		0.44	
				5.5		0.36		0.44		0.36		0.44	
			I_{OL} = 75mA[1]	5.5				1.65				1.65	
I_I	Input leakage current	V_I = V_{CC} or GND		5.5		±0.1		±1.0		±0.1		±1.0	μA
I_{CC}	Quiescent supply current	V_I = V_{CC} or GND, I_O = 0mA		5.5		8.0		80		8.0		80	μA
ΔI_{CC}	Supply current, TTL inputs High[2]	One input at 3.4V, other inputs at V_{CC} or GND		5.5						0.9		1.0	mA

NOTES:

1. Not more than one output should be tested at a time, and the duration of the test should not exceed 10ms.
2. This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0V or V_{CC}.

Synchronous presettable synchronous BCD decade counter, asynchronous reset

74AC/ACT11160

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	WAVEFORM	74AC11160					UNIT
			T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	1	66	90		66		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n ($\overline{PE}$ = "H")	1	1.5 1.5	9.0 10.6	11.2 13.4	1.5 1.5	12.5 15.1	ns
t_{PLH} t_{PHL}	Propagation delay CP to Q_n ($\overline{PE}$ = "L")	1	1.5 1.5	8.6 10.1	10.8 12.8	1.5 1.5	12.1 14.4	ns
t_{PLH} t_{PHL}	Propagation delay CP to TC	1	1.5 1.5	11.2 12.2	13.6 15.1	1.5 1.5	15.2 17.2	ns
t_{PLH} t_{PHL}	Propagation delay CET to TC	3	1.5 1.5	6.0 6.8	7.6 8.9	1.5 1.5	8.3 9.9	ns
t_{PHL}	Propagation delay $\overline{MR}$ to Q_n	2	1.5	12.0	15.2	1.5	17.3	ns
t_{PHL}	Propagation delay $\overline{MR}$ to TC	2	1.5	14.1	17.3	1.5	19.7	ns
t_S	Setup time, High or Low D_n to CP	4	6.5			6.5		ns
t_H	Hold time, High or Low D_n to CP	4	1.0			1.0		ns
t_S	Setup time, High or Low $\overline{PE}$ to CP	4	6.5			6.5		ns
t_H	Hold time, High or Low $\overline{PE}$ to CP	4	1.0			1.0		ns
t_S	Setup time, High or Low CEP or CET to CP	5	6.0			6.0		ns
t_H	Hold time, High or Low CEP or CET to CP	5	1.0			1.0		ns
t_W	Clock pulse width (load) High or Low	1	7.5			7.5		ns
t_W	Clock pulse width (count) High or Low	1	7.5			7.5		ns
t_W	$\overline{MR}$ pulse width, Low	2	6.0			6.0		ns
t_{REC}	Recovery time $\overline{MR}$ to CP	2	6.0			6.0		ns

Synchronous presettable synchronous BCD decade counter, asynchronous reset

74AC/ACT11160

AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V

SYMBOL	PARAMETER	WAVEFORM	74AC11160					UNIT
			T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	1	110	140		110		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n ($\overline{PE}$ = "H")	1	1.5 1.5	6.3 7.4	8.0 9.8	1.5 1.5	8.9 11.2	ns
t_{PLH} t_{PHL}	Propagation delay CP to Q_n ($\overline{PE}$ = "L")	1	1.5 1.5	6.0 7.1	7.5 9.4	1.5 1.5	8.4 10.7	ns
t_{PLH} t_{PHL}	Propagation delay CP to TC	1	1.5 1.5	7.8 8.5	9.5 10.6	1.5 1.5	10.7 12.1	ns
t_{PLH} t_{PHL}	Propagation delay CET to TC	3	1.5 1.5	4.2 5.0	5.5 6.7	1.5 1.5	6.0 7.5	ns
t_{PHL}	Propagation delay $\overline{MR}$ to Q_n	2	1.5	8.2	10.7	1.5	12.1	ns
t_{PHL}	Propagation delay $\overline{MR}$ to TC	2	1.5	9.9	12.2	1.5	13.8	ns
t_S	Setup time, High or Low D_n to CP	4	3.5			3.5		ns
t_H	Hold time, High or Low D_n to CP	4	1.0			1.0		ns
t_S	Setup time, High or Low $\overline{PE}$ to CP	4	6.5			6.5		ns
t_H	Hold time, High or Low $\overline{PE}$ to CP	4	1.0			1.0		ns
t_S	Setup time, High or Low CEP or CET to CP	5	4.5			4.5		ns
t_H	Hold time, High or Low CEP or CET to CP	5	1.0			1.0		ns
t_W	Clock pulse width (load) High or Low	1	4.5			4.5		ns
t_W	Clock pulse width (count) High or Low	1	4.5			4.5		ns
t_W	$\overline{MR}$ pulse width, Low	2	4.5			4.5		ns
t_{REC}	Recovery time $\overline{MR}$ to CP	2	6.0			6.0		ns

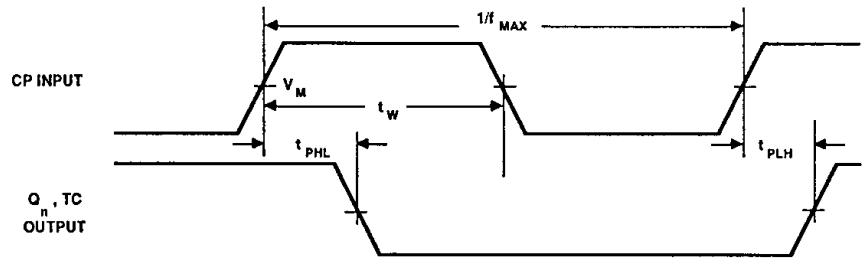
Synchronous presettable synchronous BCD decade counter, asynchronous reset

74AC/ACT11160

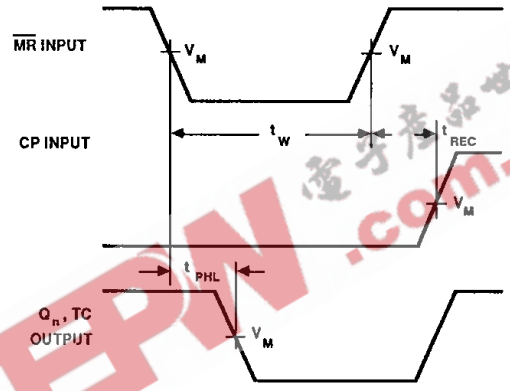
AC ELECTRICAL CHARACTERISTICS AT 5.0V ±0.5V

SYMBOL	PARAMETER	WAVEFORM	74ACT11160					UNIT
			T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	1	100	125		100		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n ($\overline{PE}$ = "H")	1	2.8 3.5	5.9 6.8	8.3 9.1	2.8 3.5	9.1 10.2	ns
t_{PLH} t_{PHL}	Propagation delay CP to Q_n ($\overline{PE}$ = "L")	1	3.0 3.7	5.8 6.7	7.9 8.8	3.0 3.7	8.6 9.8	ns
t_{PLH} t_{PHL}	Propagation delay CP to TC	1	3.8 4.4	6.9 8.3	9.1 10.8	3.8 4.4	10.1 12.0	ns
t_{PLH} t_{PHL}	Propagation delay CET to TC	3	2.3 3.1	4.3 6.7	5.6 9.2	2.3 3.1	6.0 10.1	ns
t_{PHL}	Propagation delay $\overline{MR}$ to Q_n	2	4.4	8.7	11.9	4.4	13.2	ns
t_{PHL}	Propagation delay $\overline{MR}$ to TC	2	5.4	10.1	13.2	5.4	14.7	ns
t_S	Setup time, High or Low D_n to CP	4	5.5			5.5		ns
t_H	Hold time, High or Low D_n to CP	4	1.0			1.0		ns
t_S	Setup time, High or Low $\overline{PE}$ to CP	4	7.0			7.0		ns
t_H	Hold time, High or Low $\overline{PE}$ to CP	4	1.0			1.0		ns
t_S	Setup time, High or Low CEP or CET to CP	5	7.0			7.0		ns
t_H	Hold time, High or Low CEP or CET to CP	5	1.0			1.0		ns
t_W	Clock pulse width (load) High or Low	1	5.0			5.0		ns
t_W	Clock pulse width (count) High or Low	1	5.0			5.0		ns
t_W	$\overline{MR}$ pulse width, Low	2	5.0			5.0		ns
t_{REC}	Recovery time $\overline{MR}$ to CP	2	5.0			5.0		ns

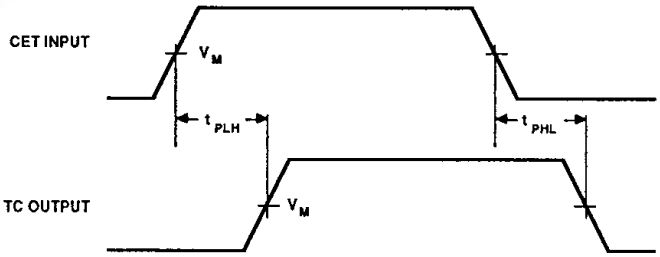
AC WAVEFORMS



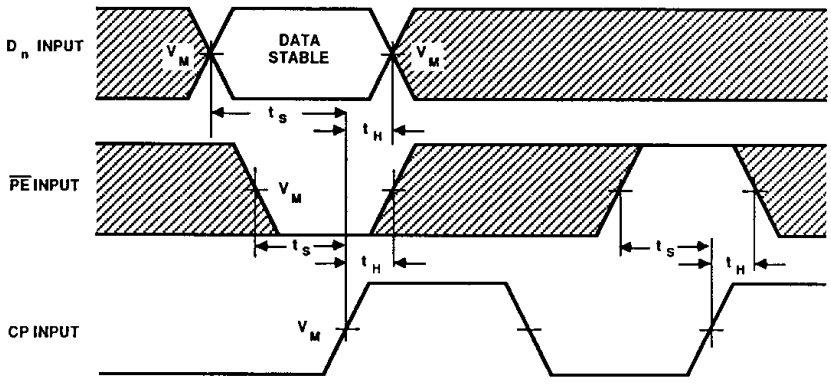
Waveform 1. Waveforms Showing Clock to Outputs Propagation Delays and Clock Pulse Width



Waveform 2. Waveforms Showing the Master Reset ($\overline{MR}$) Pulse Width, the Master Reset to Output (Qn, TC) Propagation Delays, and the Master Reset to Clock (CP) Recovery Time

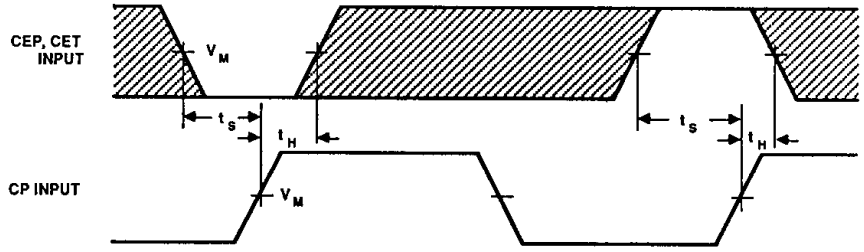


Waveform 3. Waveforms Showing the Input (CET) to Output (TC) Propagation Delays



Waveform 4. Waveforms Showing the Data Set-up and Hold Times for the Input (D_n) and Parallel Enable Input $\overline{PE}$

AC WAVEFORMS (Continued)

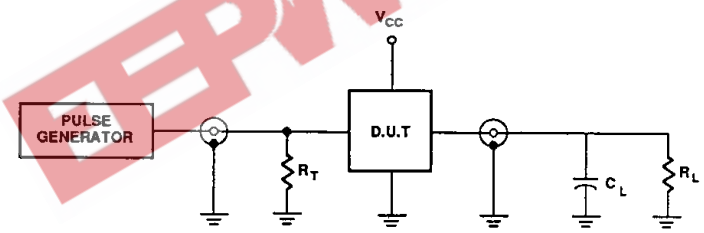


Waveform 5. Waveforms Showing CEP and CET Set-up and Hold Times

WAVEFORM CONDITIONS

	INPUTS	OUTPUTS
AC	V_{IN} = GND to V_{CC}, V_M = 50% V_{CC}	V_{OUT} = V_{OL} to V_{OH} V_M = 50% V_{CC}
ACT	V_{IN} = GND to 3.0V, V_M = 1.5V	

TEST CIRCUIT



Test Circuit

DEFINITIONS

C_L = Load capacitance, 50pF; includes jig and probe capacitance

R_L = Load resistor, 500Ω

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators

Input pulses: PRR ≤ 10MHz

$t_r = t_f$ = 3ns