



Integrated Device Technology, Inc.

FAST CMOS OCTAL REGISTERED TRANSCEIVERS

IDT29FCT52AT/BT/CT/DT
IDT29FCT2052AT/BT/CT
IDT29FCT53AT/BT/CT

FEATURES:

• Common features:

- Low input and output leakage $\leq 1\mu\text{A}$ (max.)
- CMOS power levels
- True TTL input and output compatibility
 - $V_{OH} = 3.3\text{V}$ (typ.)
 - $V_{OL} = 0.3\text{V}$ (typ.)
- Meets or exceeds JEDEC standard 18 specifications
- Product available in Radiation Tolerant and Radiation Enhanced versions
- Military product compliant to MIL-STD-883, Class B and DESC listed (dual marked)
- Available in DIP, SOIC, SSOP, QSOP, CERPACK and LCC packages

• Features for 29FCT52/29FCT53T:

- A, B, C and D speed grades
- High drive outputs (-15mA IOH, 64mA IOL)
- Power off disable outputs permit "live insertion"

• Features for 29FCT2052T:

- A, B and C speed grades
- Resistor outputs (-15mA IOH, 12mA IOL Com.)
(-12mA IOH, 12mA IOL Mil.)
- Reduced system switching noise

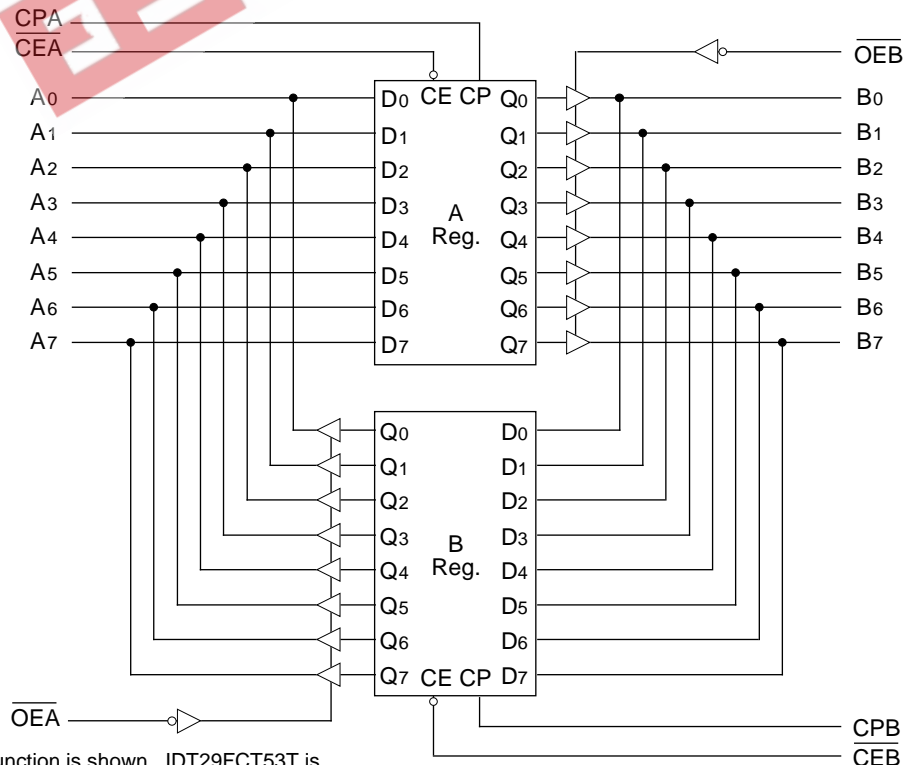
DESCRIPTION:

The IDT29FCT52AT/BT/CT/DT and IDT29FCT53AT/BT/CT are 8-bit registered transceivers built using an advanced dual metal CMOS technology. Two 8-bit back-to-back registers store data flowing in both directions between two bidirectional buses. Separate clock, clock enable and 3-state output enable signals are provided for each register. Both A outputs and B outputs are guaranteed to sink 64mA.

The IDT29FCT52AT/BT/CT/DT and IDT29FCT2052AT/BT/CT are non-inverting options of the IDT29FCT53AT/BT/CT.

The IDT29FCT2052AT/BT/CT has balanced drive outputs with current limiting resistors. This offers low ground bounce, minimal undershoot and controlled output fall times-reducing the need for external series terminating resistors. The IDT29FCT2052T part is a plug-in replacement for IDT29FCT52T part.

FUNCTIONAL BLOCK DIAGRAM⁽¹⁾



NOTE:

1. IDT29FCT52T/IDT29FCT2052T function is shown. IDT29FCT53T is the inverting option.

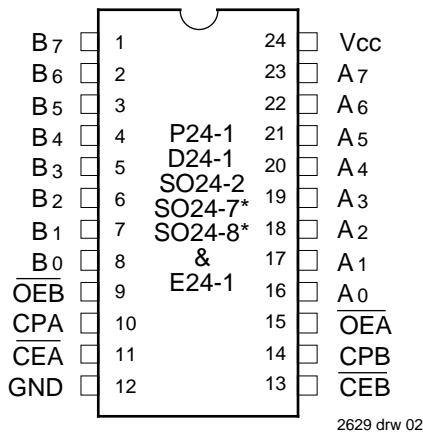
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2629 drw 01

MILITARY AND COMMERCIAL TEMPERATURE RANGES

JUNE 1995

PIN CONFIGURATIONS



**DIP/SOIC/SSOP/QSOP/CERPACK
 TOP VIEW**

* For 29FCT52/29FCT2052AT/BT/CT only



**LCC
 TOP VIEW**

PIN DESCRIPTION

| Name | I/O | Description |
|-------------------------|-----|---|
| A0-7 | I/O | Eight bidirectional lines carrying the A Register inputs or B Register outputs. |
| B0-7 | I/O | Eight bidirectional lines carrying the B Register inputs or A Register outputs. |
| CPA | I | Clock for the A Register. When CEA is LOW, data is entered into the A Register on the LOW-to-HIGH transition of the CPA signal. |
| $\overline{\text{CEA}}$ | I | Clock Enable for the A Register. When $\overline{\text{CEA}}$ is LOW, data is entered into the A Register on the LOW-to-HIGH transition of the CPA signal. When $\overline{\text{CEA}}$ is HIGH, the A Register holds its contents, regardless of CPA signal transitions. |
| $\overline{\text{OEB}}$ | I | Output Enable for the A Register. When $\overline{\text{OEB}}$ is LOW, the A Register outputs are enabled onto the B0-7 lines. When $\overline{\text{OEB}}$ is HIGH, the B0-7 outputs are in the high-impedance state. |
| CPB | I | Clock for the B Register. When CEB is LOW, data is entered into the B Register on the LOW-to-HIGH transition of the CPB signal. |
| $\overline{\text{CEB}}$ | I | Clock Enable for the B Register. When $\overline{\text{CEB}}$ is LOW, data is entered into the B Register on the LOW-to-HIGH transition of the CPB signal. When $\overline{\text{CEB}}$ is HIGH, the B Register holds its contents, regardless of CPB signal transitions. |
| $\overline{\text{OEA}}$ | I | Output Enable for the B Register. When $\overline{\text{OEA}}$ is LOW, the B Register outputs are enabled onto the A0-7 lines. When $\overline{\text{OEA}}$ is HIGH, the A0-7 outputs are in the high-impedance state. |

2629 tbl 01

REGISTER FUNCTION TABLE⁽¹⁾ (Applies to A or B Register)

| Inputs | | | Internal Q | Function |
|--------|----|-----------------|---------------|-----------|
| D | CP | \overline{CE} | | |
| X | X | H | NC | Hold Data |
| L | ↑ | L | L | Load Data |
| H | ↑ | L | H | |

NOTE:

- H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
NC = No Change
↑ = LOW-to-HIGH Transition

2629 tbl 02

OUTPUT CONTROL⁽¹⁾

| \overline{OE} | Internal Q | Y-Outputs | | Function |
|-----------------|---------------|-----------|----|-----------------|
| | | 52/2052 | 53 | |
| H | X | Z | Z | Disable Outputs |
| L | L | L | H | Enable Outputs |
| L | H | H | L | |

NOTE:

- H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
Z = High Impedance

2629 tbl 03

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

| Symbol | Rating | Commercial | Military | Unit |
|----------------------|--------------------------------------|------------------------------|------------------------------|------|
| VTERM ⁽²⁾ | Terminal Voltage with Respect to GND | -0.5 to +7.0 | -0.5 to +7.0 | V |
| VTERM ⁽³⁾ | Terminal Voltage with Respect to GND | -0.5 to V _{CC} +0.5 | -0.5 to V _{CC} +0.5 | V |
| TA | Operating Temperature | 0 to +70 | -55 to +125 | °C |
| TBIAS | Temperature Under Bias | -55 to +125 | -65 to +135 | °C |
| TSTG | Storage Temperature | -55 to +125 | -65 to +150 | °C |
| PT | Power Dissipation | 0.5 | 0.5 | W |
| IOUT | DC Output Current | -60 to +120 | -60 to +120 | mA |

NOTES:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed V_{CC} by +0.5V unless otherwise noted.
- Input and V_{CC} terminals only.
- Outputs and I/O terminals only.

2529 lmk 04

CAPACITANCE (TA = +25°C, f = 1.0MHz)

| Symbol | Parameter ⁽¹⁾ | Conditions | Typ. | Max. | Unit |
|--------|--------------------------|-----------------------|------|------|------|
| CIN | Input Capacitance | V _{IN} = 0V | 6 | 10 | pF |
| COUT | Output Capacitance | V _{OUT} = 0V | 8 | 12 | pF |

NOTE:

- This parameter is measured at characterization but not tested.

2640 lmk 05

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Commercial: $T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$, $V_{CC} = 5.0\text{V} \pm 5\%$; Military: $T_A = -55^\circ\text{C}$ to $+125^\circ\text{C}$, $V_{CC} = 5.0\text{V} \pm 10\%$

| Symbol | Parameter | Test Conditions ⁽¹⁾ | | Min. | Typ. ⁽²⁾ | Max. | Unit |
|-----------|---|--|---------------------|------|---------------------|---------|---------------|
| V_{IH} | Input HIGH Level | Guaranteed Logic HIGH Level | | 2.0 | — | — | V |
| V_{IL} | Input LOW Level | Guaranteed Logic LOW Level | | — | — | 0.8 | V |
| I_{IH} | Input HIGH Current ⁽⁴⁾ | $V_{CC} = \text{Max.}$ | $V_I = 2.7\text{V}$ | — | — | ± 1 | μA |
| I_{IL} | Input LOW Current ⁽⁴⁾ | | $V_I = 0.5\text{V}$ | — | — | ± 1 | |
| I_{OZH} | High Impedance Output Current (3-State Output pins) ⁽⁴⁾ | $V_{CC} = \text{Max.}$ | $V_O = 2.7\text{V}$ | — | — | ± 1 | μA |
| I_{OZL} | | | $V_O = 0.5\text{V}$ | — | — | ± 1 | |
| I_I | Input HIGH Current ⁽⁴⁾ | $V_{CC} = \text{Max.}, V_I = V_{CC} (\text{Max.})$ | | — | — | ± 1 | μA |
| V_{IK} | Clamp Diode Voltage | $V_{CC} = \text{Min.}, I_{IN} = -18\text{mA}$ | | — | -0.7 | -1.2 | V |
| V_H | Input Hysteresis | — | | — | 200 | — | mV |
| I_{CC} | Quiescent Power Supply Current | $V_{CC} = \text{Max.}, V_{IN} = \text{GND or } V_{CC}$ | | — | 0.01 | 1 | mA |

2629tbl06

OUTPUT DRIVE CHARACTERISTICS FOR 29FCT52T/29FCT53T

| Symbol | Parameter | Test Conditions ⁽¹⁾ | | Min. | Typ. ⁽²⁾ | Max. | Unit |
|-----------|---|--|--|------|---------------------|---------|---------------|
| V_{OH} | Output HIGH Voltage | $V_{CC} = \text{Min.}$ $V_{IN} = V_{IH} \text{ or } V_{IL}$ | $I_{OH} = -6\text{mA MIL.}$ | 2.4 | 3.3 | — | V |
| | | | $I_{OH} = -8\text{mA COM'L.}$ | — | — | — | — |
| | | | $I_{OH} = -12\text{mA MIL.}$ $I_{OH} = -15\text{mA COM'L.}$ | 2.0 | 3.0 | — | V |
| V_{OL} | Output LOW Voltage | $V_{CC} = \text{Min.}$ $V_{IN} = V_{IH} \text{ or } V_{IL}$ | $I_{OL} = 48\text{mA MIL.}$ | — | 0.3 | 0.55 | V |
| | | | $I_{OL} = 64\text{mA COM'L.}$ | — | — | — | — |
| I_{OS} | Short Circuit Current | $V_{CC} = \text{Max.}, V_O = \text{GND}^{(3)}$ | | -60 | -120 | -225 | mA |
| I_{OFF} | Input/Output Power Off Leakage ⁽⁵⁾ | $V_{CC} = 0\text{V}, V_{IN} \text{ or } V_O \leq 4.5\text{V}$ | | — | — | ± 1 | μA |

2629tbl07

OUTPUT DRIVE CHARACTERISTICS FOR 29FCT2052T

| Symbol | Parameter | Test Conditions ⁽¹⁾ | | Min. | Typ. ⁽²⁾ | Max. | Unit |
|-----------|---------------------|---|--------------------------------|------|---------------------|------|------|
| I_{ODL} | Output LOW Current | $V_{CC} = 5\text{V}, V_{IN} = V_{IH} \text{ or } V_{IL}, V_{OUT} = 1.5\text{V}^{(3)}$ | | 16 | 48 | — | mA |
| I_{ODH} | Output HIGH Current | $V_{CC} = 5\text{V}, V_{IN} = V_{IH} \text{ or } V_{IL}, V_{OUT} = 1.5\text{V}^{(3)}$ | | -16 | -48 | — | mA |
| V_{OH} | Output HIGH Voltage | $V_{CC} = \text{Min.}$ $V_{IN} = V_{IH} \text{ or } V_{IL}$ | $I_{OH} = -12\text{mA MIL.}$ | 2.4 | 3.3 | — | V |
| | | | $I_{OH} = -15\text{mA COM'L.}$ | — | — | — | — |
| V_{OL} | Output LOW Voltage | $V_{CC} = \text{Min.}$ $V_{IN} = V_{IH} \text{ or } V_{IL}$ | $I_{OL} = 12\text{mA}$ | — | 0.3 | 0.50 | V |

NOTES:

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at $V_{CC} = 5.0\text{V}$, $+25^\circ\text{C}$ ambient.
- Not more than one output should be shorted at one time. Duration of the short circuit test should not exceed one second.
- The test limit for this parameter is $\pm 5\mu\text{A}$ at $T_A = -55^\circ\text{C}$.
- This parameter is guaranteed but not tested.

2629tbl08

POWER SUPPLY CHARACTERISTICS

| Symbol | Parameter | Test Conditions ⁽¹⁾ | | Min. | Typ. ⁽²⁾ | Max. | Unit | |
|-----------------|---|--|--|----------|---------------------|--------------------|------|------------|
| ΔI_{CC} | Quiescent Power Supply Current TTL Inputs HIGH | $V_{CC} = \text{Max.}$ $V_{IN} = 3.4V^{(3)}$ | | — | 0.5 | 2.0 | mA | |
| I_{CCD} | Dynamic Power Supply Current ⁽⁴⁾ | $V_{CC} = \text{Max.}$ Outputs Open $\overline{OE}A$ or $\overline{OE}B = \text{GND}$ One Input Toggling 50% Duty Cycle | $V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$ | FCTxxxT | — | 0.15 | 0.25 | mA/ MHz |
| | | | | FCT2xxxT | — | 0.06 | 0.12 | |
| I_C | Total Power Supply Current ⁽⁶⁾ | $V_{CC} = \text{Max.}$ Outputs Open $f_{CP} = 10\text{MHz}$ 50% Duty Cycle $\overline{OE}A$ or $\overline{OE}B = \text{GND}$ One Bit Toggling at $f_i = 5\text{MHz}$ 50% Duty Cycle | $V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$ | FCTxxxT | — | 1.5 | 3.5 | mA |
| | | | | FCT2xxxT | — | 0.6 | 2.2 | |
| | | $V_{IN} = 3.4V$ | FCTxxxT | — | 2.0 | 5.5 | | |
| | | $V_{IN} = \text{GND}$ | FCT2xxxT | | 1.1 | 4.2 | | |
| | | $V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$ | FCTxxxT | — | 3.8 | 7.3 ⁽⁵⁾ | | |
| | | | FCT2xxxT | — | 1.5 | 4.0 ⁽⁵⁾ | | |
| | $V_{IN} = 3.4V$ | FCTxxxT | — | 6.0 | 16.3 ⁽⁵⁾ | | | |
| | $V_{IN} = \text{GND}$ | FCT2xxxT | — | 3.8 | 13.0 ⁽⁵⁾ | | | |

NOTES:

2629tbl09

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at $V_{CC} = 5.0V$, $+25^\circ\text{C}$ ambient.
- Per TTL driven input ($V_{IN} = 3.4V$). All other inputs at V_{CC} or GND .
- This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
- Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
- $I_C = I_{\text{QUIESCENT}} + I_{\text{INPUTS}} + I_{\text{DYNAMIC}}$
 $I_C = I_{CC} + \Delta I_{CC} \text{DHNT} + I_{CCD} (f_{CP}/2 + f_i N_i)$
 $I_{CC} = \text{Quiescent Current}$
 $\Delta I_{CC} = \text{Power Supply Current for a TTL High Input } (V_{IN} = 3.4V)$
 $DH = \text{Duty Cycle for TTL Inputs High}$
 $N_T = \text{Number of TTL Inputs at } DH$
 $I_{CCD} = \text{Dynamic Current Caused by an Input Transition Pair (HLH or LHL)}$
 $f_{CP} = \text{Clock Frequency for Register Devices (Zero for Non-Register Devices)}$
 $f_i = \text{Input Frequency}$
 $N_i = \text{Number of Inputs at } f_i$
 All currents are in milliamps and all frequencies are in megahertz.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

| Symbol | Parameter | Condition ⁽¹⁾ | 29FCT52AT/53AT 29FCT2052AT | | | | 29FCT52BT/53BT 29FCT2052BT | | | | Unit |
|--------------|--|--------------------------|-------------------------------|------|---------------------|------|-------------------------------|------|---------------------|------|------|
| | | | Com'l. | | Mil. | | Com'l. | | Mil. | | |
| | | | Min. ⁽²⁾ | Max. | Min. ⁽²⁾ | Max. | Min. ⁽²⁾ | Max. | Min. ⁽²⁾ | Max. | |
| tPLH tPHL | Propagation Delay CPA, CPB to An, Bn | CL = 50pF RL = 500Ω | 2.0 | 10.0 | 2.0 | 11.0 | 2.0 | 7.5 | 2.0 | 8.0 | ns |
| tPZH tPZL | Output Enable Time OEA or OEB to An, Bn | | 1.5 | 10.5 | 1.5 | 13.0 | 1.5 | 8.0 | 1.5 | 8.5 | ns |
| tPHZ tPLZ | Output Disable Time OEA or OEB to An, Bn | | 1.5 | 10.0 | 1.5 | 10.0 | 1.5 | 7.5 | 1.5 | 8.0 | ns |
| tsU | Set-up Time, HIGH or LOW An, Bn to CPA, CPB | | 2.5 | — | 2.5 | — | 2.5 | — | 2.5 | — | ns |
| th | Hold Time, HIGH or LOW An, Bn to CPA, CPB | | 2.0 | — | 2.0 | — | 1.5 | — | 1.5 | — | ns |
| tsU | Set-up Time, HIGH or LOW CEA, CEB to CPA, CPB | | 3.0 | — | 3.0 | — | 3.0 | — | 3.0 | — | ns |
| th | Hold Time, HIGH or LOW CEA, CEB to CPA, CPB | | 2.0 | — | 2.0 | — | 2.0 | — | 2.0 | — | ns |
| tw | Clock Pulse Width HIGH or LOW ⁽³⁾ | | 3.0 | — | 3.0 | — | 3.0 | — | 3.0 | — | ns |

2629 tbl 10

| Symbol | Parameter | Condition ⁽¹⁾ | 29FCT52CT/53CT 29FCT2052CT | | | | 29FCT52DT | | | | Unit |
|--------------|--|--------------------------|-------------------------------|------|---------------------|------|---------------------|------|---------------------|------|------|
| | | | Com'l. | | Mil. | | Com'l. | | Mil. | | |
| | | | Min. ⁽²⁾ | Max. | Min. ⁽²⁾ | Max. | Min. ⁽²⁾ | Max. | Min. ⁽²⁾ | Max. | |
| tPLH tPHL | Propagation Delay CPA, CPB to An, Bn | CL = 50pF RL = 500Ω | 2.0 | 6.3 | 2.0 | 7.3 | 2.0 | 4.5 | — | — | ns |
| tPZH tPZL | Output Enable Time OEA or OEB to An, Bn | | 1.5 | 7.0 | 1.5 | 8.0 | 1.5 | 5.6 | — | — | ns |
| tPHZ tPLZ | Output Disable Time OEA or OEB to An, Bn | | 1.5 | 6.5 | 1.5 | 7.5 | 1.5 | 4.3 | — | — | ns |
| tsU | Set-up Time, HIGH or LOW An, Bn to CPA, CPB | | 2.5 | — | 2.5 | — | 1.5 | — | — | — | ns |
| th | Hold Time, HIGH or LOW An, Bn to CPA, CPB | | 1.5 | — | 1.5 | — | 1.0 | — | — | — | ns |
| tsU | Set-up Time, HIGH or LOW CEA, CEB to CPA, CPB | | 3.0 | — | 3.0 | — | 2.0 | — | — | — | ns |
| th | Hold Time, HIGH or LOW CEA, CEB to CPA, CPB | | 2.0 | — | 2.0 | — | 1.0 | — | — | — | ns |
| tw | Clock Pulse Width HIGH or LOW ⁽³⁾ | | 3.0 | — | 3.0 | — | 3.0 | — | — | — | ns |

NOTES:

1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. This parameter is guaranteed but not tested.

2629 tbl 11

TEST CIRCUITS AND WAVEFORMS

TEST CIRCUITS FOR ALL OUTPUTS



2629 drw 03

SWITCH POSITION

| Test | Switch |
|---|--------|
| Open Drain Disable Low Enable Low | Closed |
| All Other Tests | Open |

DEFINITIONS:

CL= Load capacitance: includes jig and probe capacitance.

RT= Termination resistance: should be equal to ZOUT of the Pulse Generator.

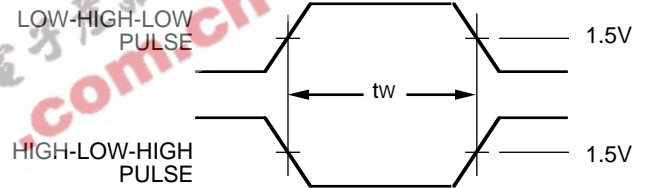
2629 Ink 12

SET-UP, HOLD AND RELEASE TIMES



2629 drw 04

PULSE WIDTH



2629 drw 05

PROPAGATION DELAY



2629 drw 06



2629 drw 07

NOTES:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH
2. Pulse Generator for All Pulses: Rate $\leq 1.0\text{MHz}$; $t_f \leq 2.5\text{ns}$; $t_r \leq 2.5\text{ns}$

ORDERING INFORMATION



2629 drw 08