DATA SHEET

For a complete data sheet, please also download:

- The IC06 74HC/HCT/HCU/HCMOS Logic Family Specifications
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Information
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Outlines

74HC/HCT7731
Quad 64-bit static shift register

Product specification
File under Integrated Circuits, IC06

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Philips Semiconductors

PHILIPS

Quad 64-bit static shift register 74HC/HCT7731

FEATURES

- Frequency range DC to 100 MHz.
- Separate serial data inputs
- Cascadable
- Functionally compatible with HEF 4731
- Includes recycling mode
- Direct shift out
- Output capability: Standard
- I_{CC} category: LSI.

APPLICATIONS

- Data storage
- Delay line.

GENERAL DESCRIPTION

The HC/HCT7731 are high-speed Si-gate CMOS devices. They are specified in compliance with JEDEC standard no. 7A.

The HC/HCT7731 are quad 64-bit static shift registers with a recycling mode. Each register has separate data inputs D_a to D_d, clock inputs CP_a to CP_d and data outputs Q_a to Q_d. Data shifts one place towards the output, each LOW to HIGH transition of the clock pulse. Each recycling mode input controls two registers REC_{ab} for registers A and B and REC_{cd} for registers C and D. When the REC input is HIGH, the device is in the recycling mode and data at the output is shifted back into the input of the register, so after 64 clock pulses the contents of a register is again in its original position. This enables the user to tap off data from any position. When the REC input is LOW external data can be shifted in.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns.

SYMBOL	PARAMETER	CONDITIONS	TYP.		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay CP_{a-d} to Q_{a-d}	C_L = 15 pF; V_{CC} = 5 V	15	20	ns
f_{max}	maximum clock frequency		100	100	MHz
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per register	notes 1, 2 and 3	58	61	pF

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW):

   $P_D = (C_{PD} \times V_{CC}^2 \times f_i) + (C_L + V_{CC}^2 \times f_o) + (I_{pull\text{-}up} \times V_{CC})$

   where:

   f_i = input frequency in MHz.

   f_o = output frequency in MHz.

   V_{CC} = supply voltage in V.

   C_L = output load capacitance in pF.

   $I_{pull\text{-}up}$ = pull-up currents in µA.

2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} – 1.5 V.
3. See also power dissipation information.

ORDERING INFORMATION

EXTENDED TYPE NUMBER	PACKAGE			
	PINS	PIN POSITION	MATERIAL	CODE
74HC/HCT7731N	16	DIL	plastic	SOT38Z
74HC/HCT7731D	16	SO16	plastic	SOT109A

Quad 64-bit static shift register 74HC/HCT7731

PINNING

SYMBOL	PIN	DESCRIPTION
Q_a to Q_d	1, 7, 9, 15	data outputs
CP_a to CP_d	2, 6, 10, 14	clock inputs
D_a to D_d	3, 5, 11, 13	data inputs
REC_{ab}, REC_{cd}	4, 12	recycled enable input
GND	8	ground (0 V)
V_{CC}	16	positive supply

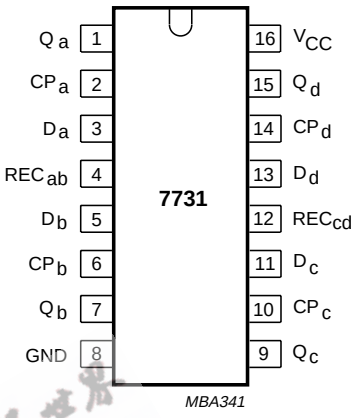


Fig.1 Pin configuration.

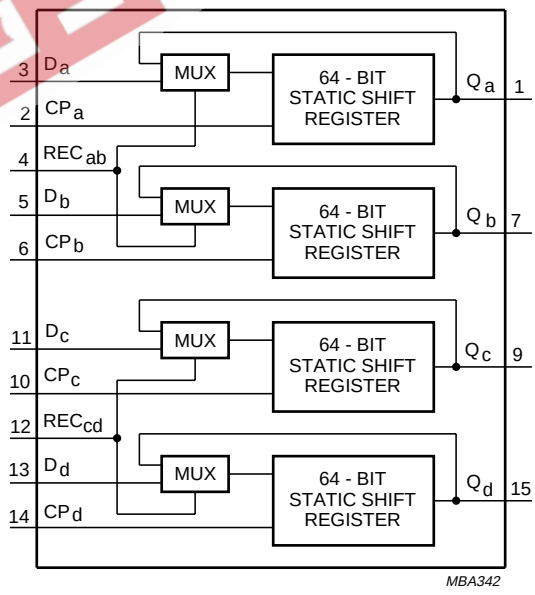


Fig.2 Functional diagram.

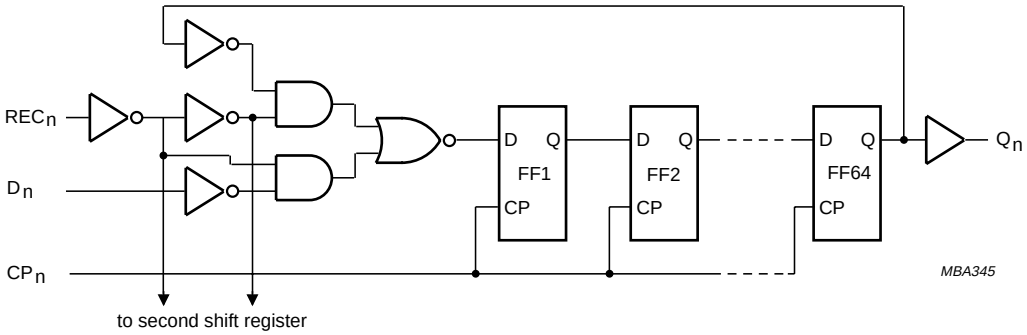


Fig.3 Logic diagram.

FUNCTION TABLE

INPUT		OUTPUT
REC	CP	MODE
L	↑	shift
H	↑	recycle

Notes

1. L = LOW voltage level
   H = HIGH voltage Level
   ↑ = LOW-to-HIGH CP transition

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: standard

I_{CC} category: LSI.

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF.

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITION	
		+25			–40 to +85		–40 to +125			V_{CC} (V)	WAVEFORMS
		MIN	TYP	MAX	MIN	MAX	MIN	MAX			
t_{PHL}/t_{PLH}	propagation delay time CP to Q_n	– – –	50 18 15	155 31 26	– – –	190 38 32	– – –	230 46 39	ns ns ns	2.0 4.5 6.0	Fig.4
t_{THL}/t_{TLH}	output transition time	– – –	19 7 6	75 15 13	– – –	90 18 15	– – –	110 22 19	ns ns ns	2.0 4.5 6.0	Fig.4
t_W	clock pulse width HIGH or LOW	80 16 14	19 7 6	– – –	100 20 17	– – –	120 24 20	– – –	ns ns ns	2.0 4.5 6.0	Fig.4
t_{su}	set-up time D_n to CP_n	60 12 10	8 3 3	– – –	75 15 13	– – –	90 18 15	– – –	ns ns ns	2.0 4.5 6.0	Fig.4
t_{su}	set-up time REC_n to CP_n	75 15 13	22 8 7	– – –	90 18 15	– – –	110 22 19	– – –	ns ns ns	2.0 4.5 6.0	Fig.5
t_h	hold time D_n to CP_n	25 5 4	–3 –1 –1	– – –	30 6 5	– – –	35 7 6	– – –	ns ns ns	2.0 4.5 6.0	Fig.4
t_h	hold time REC_n to CP_n	10 2 2	–8 –3 –3	– – –	10 2 2	– – –	15 3 3	– – –	ns ns ns	2.0 4.5 6.0	Fig.5
f_{max}	maximum clock pulse frequency	6 30 35	26 78 93	– – –	4.8 24 28	– – –	4 20 23	– – –	MHz MHZ MHz	2.0 4.5 6.0	Fig.4 (note 1)

Note

1. The maximum power dissipation has to be observed. See power dissipation information.

UNIT LOAD COEFFICIENT

INPUT	UNIT LOAD COEFFICIENT
CP_n	0.7
REC_n	0.4
D_n	0.5

Notes

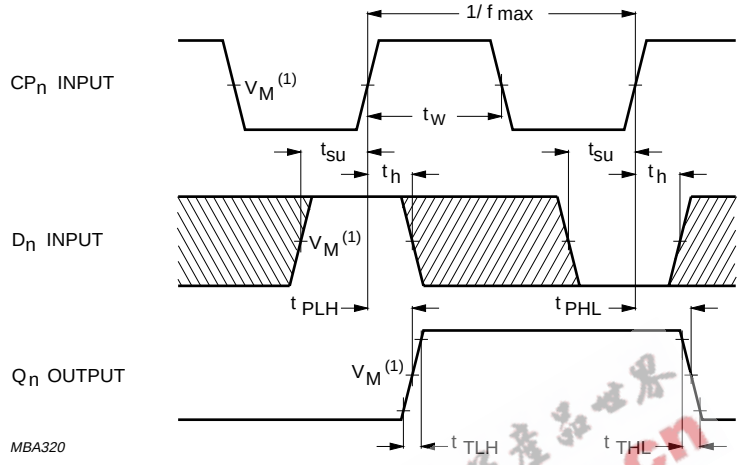
1. The RS input has CMOS input switching levels.
2. The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in Table 1.

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF.

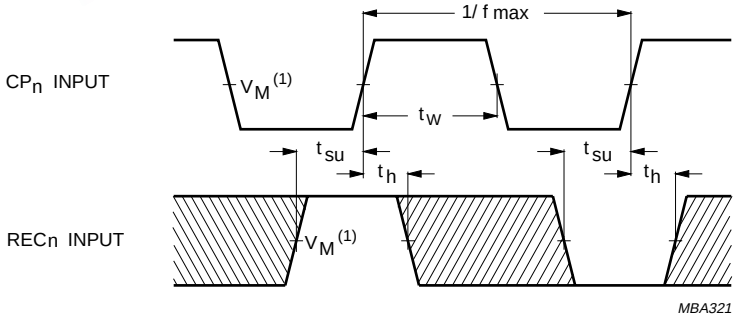
SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITION	
		+25			−40 to +85		−40 to +125			V_{CC} (V)	WAVEFORMS
		MIN	TYP	MAX	MIN	MAX	MIN	MAX			
t_{PHL}/t_{PLH}	propagation delay time CP to Q_n	–	24	42	–	52	–	63	ns	4.5	Fig.4
t_{THL}/t_{TLH}	output transmission time	–	7	15	–	18	–	22	ns	4.5	Fig.4
t_W	clock pulse width HIGH or LOW	16	7	–	20	–	24	–	ns	4.5	Fig.4
t_{su}	set-up time D_n to CP_n	12	3	–	15	–	18	–	ns	4.5	Fig.4
t_{su}	set-up time REC_n to CP_n	15	6	–	18	–	22	–	ns	2	Fig.5
t_h	hold time D_n to CP_n	5	0	–	6	–	7	–	ns	2	Fig.4
t_h	hold time REC_n to CP_n	2	−3	–	2	–	3	–	ns	4.5	Fig.5
f_{max}	maximum clock pulse frequency	30	80	–	24	–	20	–	MHz	4.5	Fig.4 (note 1)

AC WAVEFORMS



(1) HC : V_M = 50%; V_I = GND to V_{CC}
HCT : V_M = 1.3 V; V_I = GND to 3 V.

Fig.4 Waveforms showing the clock (CP) and data (D) input to output (Q) propagation delay, set-up, hold and transition times.



(1) HC : V_M = 50%; V_I = GND to V_{CC}
HCT : V_M = 1.3 V; V_I = GND to 3 V.

Fig.5 Waveforms showing the clock (CP) to recycle (REC) set-up and hold times.

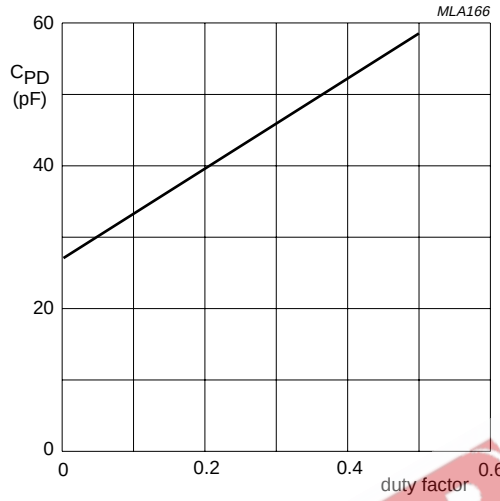


Fig.6 C_{PD} as a function of the duty factor.

POWER DISSIPATION INFORMATION

The power dissipation per register operating at the same frequency is given by:

$$P_D = (C_{PD} \times V_{CC}^2 \times f_i) + (C_L + V_{CC}^2 \times f_o) + (I_{pull\text{-}up} \times V_{CC})$$

f_i = clock input frequency
f_o = data output frequency
C_L = output load capacitance in pF
V_{CC} = power supply voltage in V.

As P_D also depends on the frequency at which the contents of the internal bits are changing, the value of C_{PD} is a function of the duty factor (d_f) being the ration between data and clock frequency, see Fig.6.

Example:

f_i = 12 MHz
f_o = 3 MHz
C_L = 25 pF
V_{CC} = 5 V
d_f = 3/12 = 0.25
C_{PD} = 42.5 pF
$P_D = (42.5 \times 5^2 \times 12) + (25 \times 5^2 \times 3) = 14625\ \mu W$

As the maximum allowable power dissipation in an SO package at T_{amb} = 125 °C is 60 mW, it is allowed to apply 4 registers at the same time under these conditions.

PACKAGE OUTLINES

See *"74HC/HCT/HCU/HCMOS Logic Package Outlines"*.