

DATA SHEET

For a complete data sheet, please also download:

- The IC06 74HC/HCT/HCU/HCMOS Logic Family Specifications
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Information
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Outlines

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74HC/HCT9015

Nine wide Schmitt trigger buffer/line driver

Product specification
Supersedes data of March 1988
File under Integrated Circuits, IC06

December 1990

Nine wide Schmitt trigger buffer/line driver

74HC/HCT9015

FEATURES

- Schmitt trigger action on all data inputs
- Output capability: standard
- I_{CC} category: MSI

The 74HC/HCT9015 are nine wide Schmitt trigger buffer/line drivers with Schmitt trigger inputs. These inputs transform slowly changing input signals into sharply defined jitter-free output signals.

The "9015" is identical to the "9014" but has non-inverting inputs.

GENERAL DESCRIPTION

The 74HC/HCT9015 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

QUICK REFERENCE DATA

GND = 0 V; $T_{amb} = 25\text{ }^{\circ}\text{C}$; $t_r = t_f = 6\text{ ns}$

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay A_n to Y_n	$C_L = 15\text{ pF}$; $V_{CC} = 5\text{ V}$	12	13	ns
C_i	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per buffer	notes 1 and 2	30	32	pF

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f_i = input frequency in MHz

f_o = output frequency in MHz

$\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs

C_L = output load capacitance in pF

V_{CC} = supply voltage in V

2. For HC the condition is $V_i = \text{GND to } V_{CC}$
For HCT the condition is $V_i = \text{GND to } V_{CC} - 1.5\text{ V}$

ORDERING INFORMATION

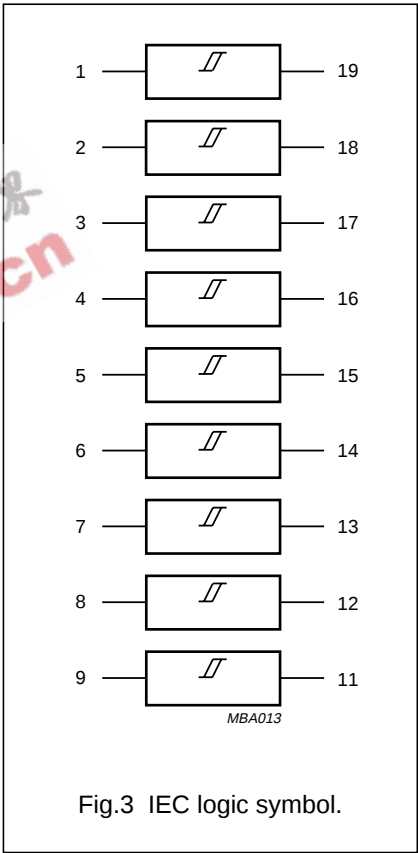
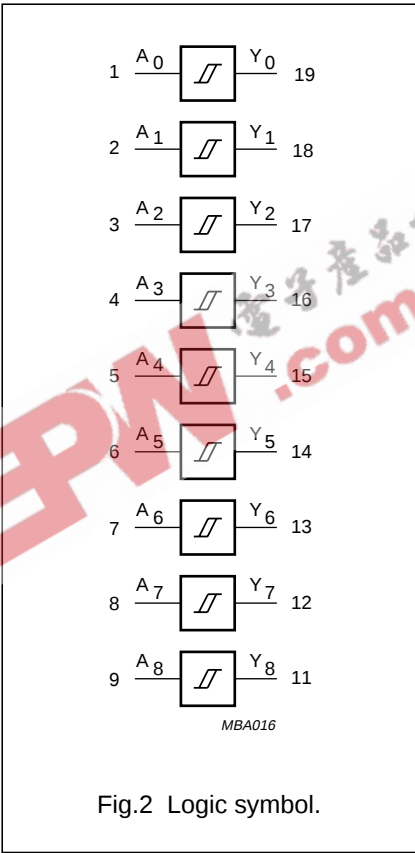
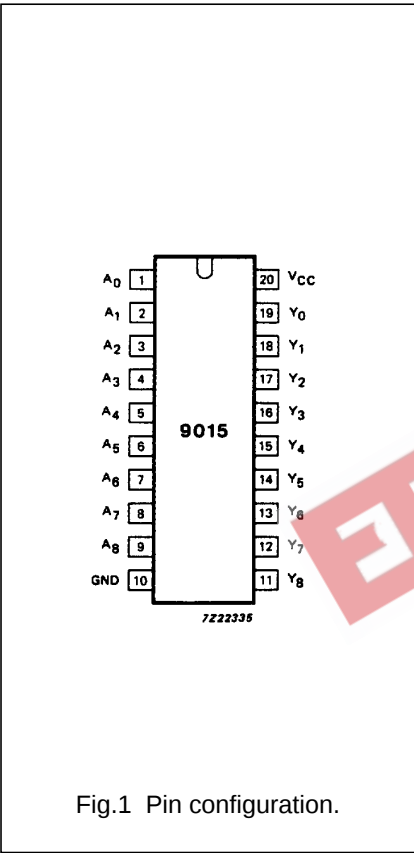
See "74HC/HCT/HCU/HCMOS Logic Package Information".

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PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 2, 3, 4, 5, 6, 7, 8, 9	A ₀ to A ₈	data inputs
10	GND	ground (0 V)
19, 18, 17, 16, 15, 14, 13, 12, 11	Y ₀ to Y ₈	data outputs
20	V _{CC}	positive supply voltage



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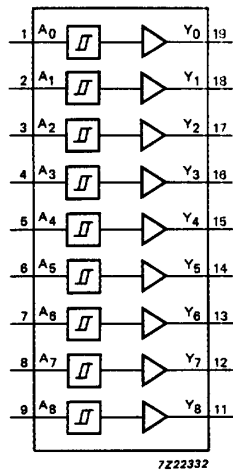


Fig.4 Functional diagram.

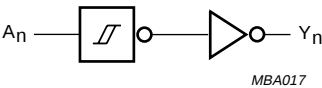


Fig.5 Logic diagram (one Schmitt trigger).

FUNCTION TABLE

INPUTS	OUTPUTS
A_n	Y_n
L	L
H	H

Notes

- 1. H = HIGH voltage level
L = LOW voltage level

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DC CHARACTERISTICS FOR 74HC

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Transfer characteristics are given below.

Output capability: standard

I_{CC} category: MSI

TRANSFER CHARACTERISTICS FOR 74HC

Voltages are referred to GND (ground = 0 V)

SYMBOL	PARAMETER	T _{amb} (°C)								UNIT	TEST CONDITIONS	
		74HC									V _{CC} (V)	WAVEFORMS
		+25			−40 to +85		−40 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
V _{T+}	positive-going threshold	0.70	1.13	1.50	0.70	1.50	0.70	1.50	V	2.0	Figs 6 and 7	
		1.75	2.37	3.15	1.75	3.15	1.75	3.15				
		2.30	3.11	4.20	2.30	4.20	2.30	4.20				
V _{T−}	negative-going threshold	0.30	0.70	1.10	0.30	1.10	0.30	1.10	V	2.0	Figs 6 and 7	
		1.35	1.80	2.40	1.35	2.40	1.35	2.40				
		1.80	2.43	3.30	1.80	3.30	1.80	3.30				
V _H	hysteresis (V _{T+} − V _{T−})	0.2	0.43	0.80	0.18	0.80	0.15	0.80	V	2.0	Fig.6	
		0.4	0.57	1.00	0.40	1.00	0.40	1.00				
		0.5	0.68	1.10	0.50	1.10	0.50	1.10				

AC CHARACTERISTICS FOR 74HC

GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T _{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V _{CC} (V)	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t _{PHL} / t _{PLH}	propagation delay A _n to Y _n		33 12 10	105 21 18		130 26 22		160 32 27	ns	2.0 4.5 6.0	Fig.8
t _{THL} / t _{TLH}	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig.8

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DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Transfer characteristics are given below.

Output capability: standard

I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications.

To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
A _n	0.3

TRANSFER CHARACTERISTICS FOR 74HCT

Voltages are referred to GND (ground = 0 V)

SYMBOL	PARAMETER	T _{amb} (°C)								UNIT	TEST CONDITIONS	
		74HCT									V _{CC} (V)	WAVEFORMS
		+25			−40 to +85		−40 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
V _{T+}	positive-going threshold	0.9 1.2	1.50 1.70	2.0 2.1	0.9 1.2	2.0 2.1	0.9 1.2	2.0 2.1	V	4.5 5.5	Figs 6 and 7	
V _{T−}	negative-going threshold	0.7 0.8	1.06 1.27	1.4 1.7	0.7 0.8	1.4 1.7	0.7 0.8	1.4 2.7	V	4.5 5.5	Figs 6 and 7	
V _H	hysteresis (V _{T+} − V _{T−})	0.2 0.2	0.44 0.44	0.8 0.8	0.2 0.2	0.8 0.8	0.2 0.2	0.8 0.8	V	4.5 5.5	Figs 6 and 7	

AC CHARACTERISTICS FOR 74HCT

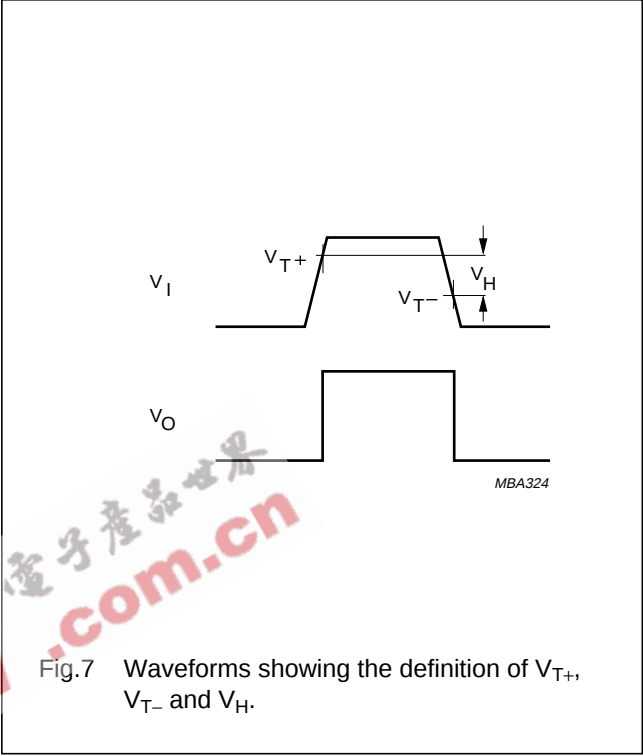
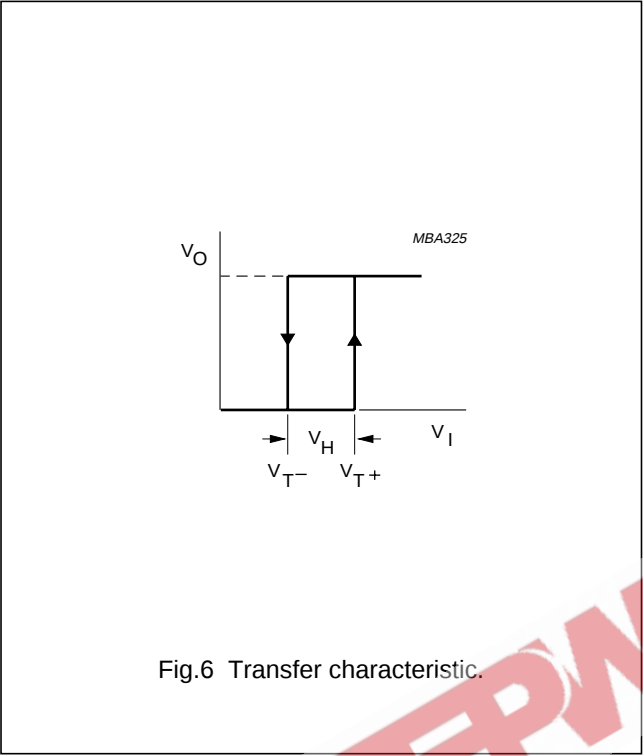
GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T _{amb} (°C)								UNIT	TEST CONDITIONS	
		74HCT									V _{CC} (V)	WAVEFORMS
		+25			−40 to +85		−40 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
t _{PHL} / t _{PLH}	propagation delay A _n to Y _n		18	32		40		48	ns	4.5	Fig.8	
t _{THL} / t _{TLH}	output transition time		7	15		19		22	ns	4.5	Fig.8	

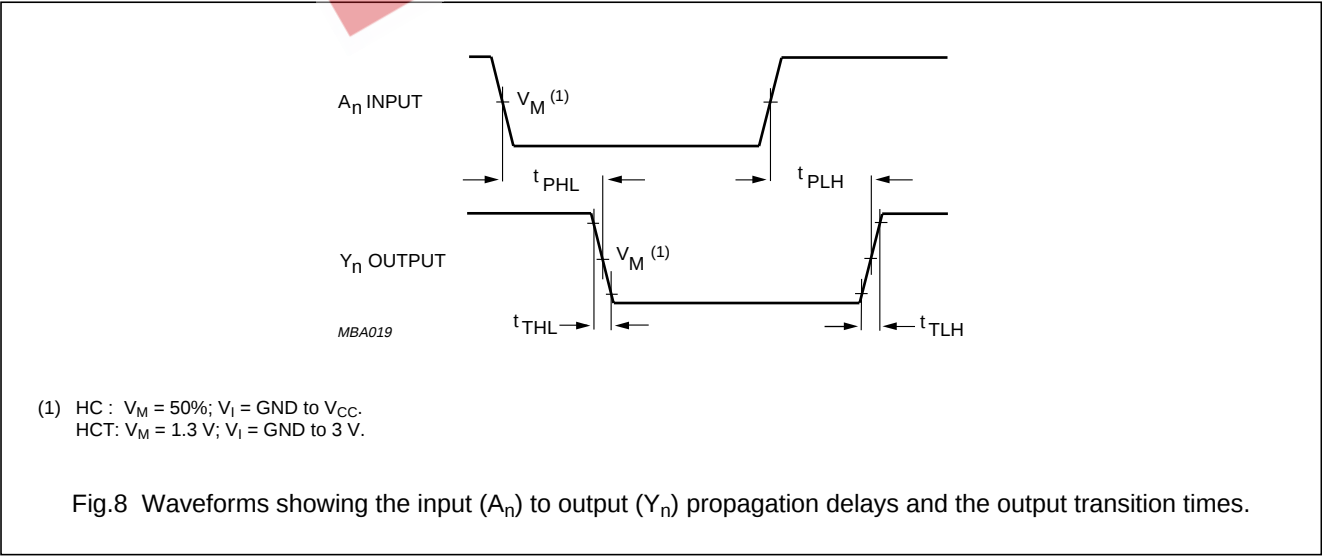
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TRANSFER CHARACTERISTIC WAVEFORMS



AC WAVEFORMS



PACKAGE OUTLINES

See "74HC/HCT/HCU/HCMOS Logic Package Outlines".