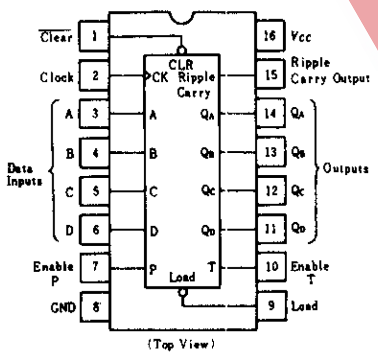
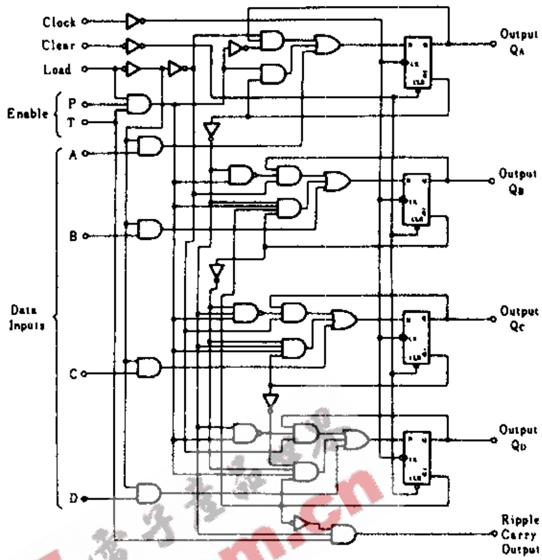
HD74LS160A ● Synchronous Decade Counters (direct clear)

This synchronous decade counter features an internal carry look-ahead for application in high-speed counting designs. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the count-enable inputs and internal gating. This mode is operation eliminates the output counting spikes that are normally associated with asynchronous (ripple clock) counters. A buffered clock input triggers the four flip-flops on the rising (positive-going) edge of the clock input waveform. This counter is fully programmable; that is, the output may be preset to either level. As presetting is synchronous, setting up a low level at the load input disables the counter and causes the outputs to agree with the setup data after the next clock pulse regardless of the levels of the enable inputs. Low-to-high transitions at the load input of this device should be avoided when the clock is low if the enable inputs are high at or before the transition. The clear function is asynchronous and a low level at the clear input sets all four of the flip-flop outputs low regardless of the levels of clock, load, or enable inputs. The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications without additional gatting. Instrumental in accomplishing this function is two count-enable inputs and a ripple carry output. Both count-enable inputs (P and T) must be high to count, and input T is fed forward to enable the ripple carry output. The ripple carry output thus enabled will produce a high-level output pulse with a duration approximately equal to the high-level portion of the Q_A output. This high-level overflow ripple carry pulse can be used to enable successive cascaded stages. High-to-low-level transitions at the enable P or T inputs should occur only when the clock input is high.

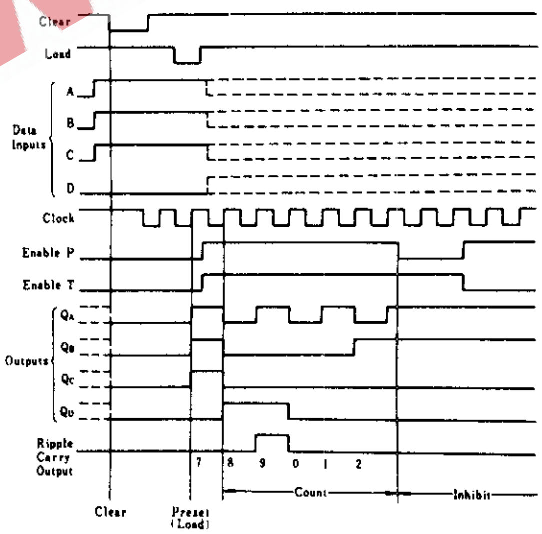
■PIN ARRANGEMENT



■BLOCK DIAGRAM



■TYPICAL CLEAR, PRESET, AND INHIBIT SEQUENCE



■RECOMMENDED OPERATIING CONDITIONS

Item		Symbol	min	typ	max	Unit
Clock frequency		f_{clock}	0	–	25	MHz
Clock pulse width		$t_{w(clock)}$	25	–	–	ns
Clear pulse width		$t_{w(clear)}$	20	–	–	ns
Setup time	A, B, C, D	t_{su}	20	–	–	ns
	Enable P, T		20	–	–	
	Load		20	–	–	
Hold time		t_h	3	–	–	ns

HD74LS160A

■ELECTRICAL CHARACTERISTICS ($Ta = -20 \sim +75°C$)

Item		Symbol	Test Conditions		min	typ*	max	Unit
Input voltage		V_{IH}			2.0	–	–	V
		V_{IL}			–	–	0.8	V
Output voltage		V_{OH}	$V_{CC}=4.75V$, $V_{IH}=2V$, $V_{IL}=0.8V$, $I_{OH}=-400\mu A$		2.7	–	–	V
		V_{OL}	$V_{CC}=4.75V$, $V_{IH}=2V$, $V_{IL}=0.8V$	$I_{OL}=4mA$	–	–	0.4	V
				$I_{OL}=8mA$	–	–	0.5	
Input current	Data, Enable P	I_{IH}	$V_{CC}=5.25V$, $V_I=2.7V$		–	–	20	μA
	Load, Clock, Enable T				–	–	40	
	Clear				–	–	20	
	Data, Enable P	I_{IL}	$V_{CC}=5.25V$, $V_I=0.4V$		–	–	−0.4	mA
	Load, Clock, Enable T				–	–	−0.8	
	Clear				–	–	−0.4	
	Data, Enable P	I_I	$V_{CC}=5.25V$, $V_I=7V$		–	–	0.1	mA
	Load, Clock, Enable T				–	–	0.2	
	Clear				–	–	0.1	
Short-circuit output current		I_{OS}	$V_{CC}=5.25V$		−20	–	−100	mA
Supply current **		I_{CCH}	$V_{CC}=5.25V$		–	18	31	mA
		I_{CCL}	$V_{CC}=5.25V$		–	19	32	mA
Input clamp voltage		V_{IK}	$V_{CC}=4.75V$, $I_{IN}=-18mA$		–	–	−1.5	V

* $V_{CC}=5V$, $Ta=25°C$

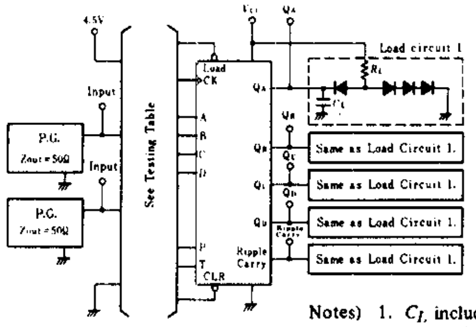
** I_{CCH} is measured with the load input high, then again with the load input low, with all other inputs high and all outputs open.
I_{CCL} is measured with the clock input high, then again with the clock input low, with all other inputs low and all outputs open.

■SWITCHING CHARACTERISTICS ($V_{CC}=5V$, $Ta=25°C$)

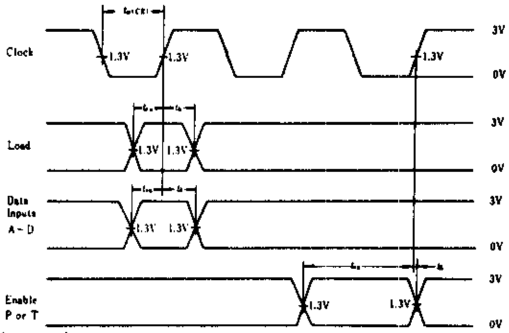
Item	Symbol	Inputs	Outputs	Test Conditions	min	typ	max	Unit
Maximum clock frequency	f_{max}	Clock	$Q_A \sim Q_D$		25	32	–	MHz
Propagation delay time	t_{PLH}	Clock	Ripple Carry	$C_L=15pF$, $R_L=2k\Omega$	–	20	35	ns
	t_{PHL}				–	18	35	ns
	t_{PLH}	Clock (Load="H")	$Q_A \sim Q_D$		–	13	24	ns
	t_{PHL}				–	18	27	ns
	t_{PLH}	Clock (Load="L")	$Q_A \sim Q_D$		–	13	24	ns
	t_{PHL}				–	18	27	ns
	t_{PLH}	Enable T	Ripple Carry		–	9	14	ns
	t_{PHL}				–	9	14	ns
	t_{PHL}	Clear	$Q_A \sim Q_D$		–	20	28	ns

■TESTING METHOD

1) Test Circuit



■TIMING METHOD



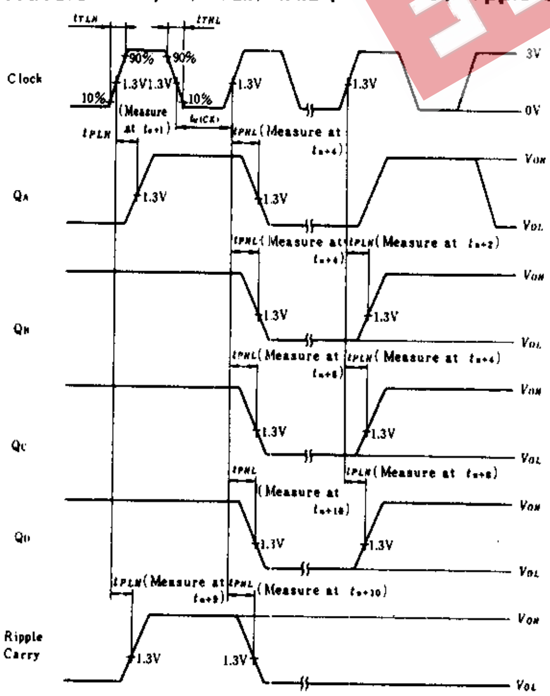
Notes) 1. C_L includes probe and jig capacitance.
2 All diodes are 1S2074 Ⓗ.

2) Testing Table

Item	From input to output	Inputs: Clear	Load	Enable P	Enable T	Clock	Data A	Data B	Data C	Data D	Outputs: Q_A	Q_B	Q_C	Q_D	Ripple Carry
f_{max}		4.5V	4.5V	4.5V	4.5V	IN	GND	GND	GND	GND	OUT	OUT	OUT	OUT	OUT
t_{PLH} t_{PHL}	CK→Ripply Carry	4.5V	4.5V	4.5V	4.5V	IN	GND	GND	GND	GND	—	—	—	—	OUT
	CK→Q	4.5V	4.5V	4.5V	4.5V	IN	GND	GND	GND	GND	OUT	OUT	OUT	OUT	—
	CK→Q	4.5V	GND	GND	GND	IN	IN*	IN*	IN*	IN*	OUT	OUT	OUT	OUT	—
	Enable T→Ripple Carry	4.5V	GND	4.5V	IN	IN**	4.5V	GND	GND	4.5V	—	—	—	—	OUT
	CLR→Q	IN	GND	GND	GND	IN**	4.5V	4.5V	4.5V	4.5V	OUT	OUT	OUT	OUT	—

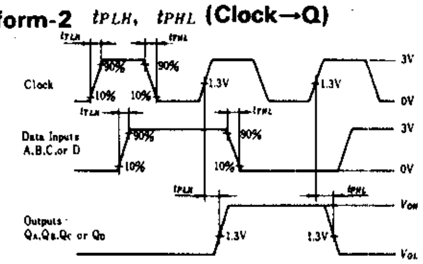
* Measuring outputs correspond to this condition, each outputs (Q_A, Q_B, Q_C, and Q_D) must not be over the following rate, "H", "L", "L", and "H".
** For initialized

Waveform-1 f_{max}, t_{PLH}, t_{PHL} (Clock→Q, Ripple Carry)



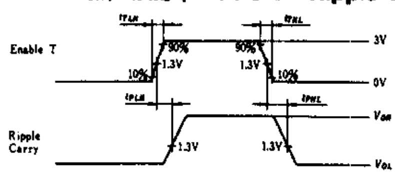
Notes) Clock input pulse; $t_{TLH} \leq 15ns$, $t_{THL} \leq 6ns$, PRR=1MHz, duty cycle=50% and: for f_{max}, $t_{TLH}=t_{THL} \leq 2.5ns$.
t_n is reference bit time when all outputs are low.

Waveform-2 t_{PLH}, t_{PHL} (Clock→Q)



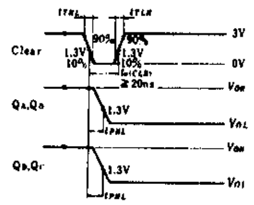
Notes) Input pulse: $t_{TLH} \leq 15ns$, $t_{THL} \leq 6ns$, Clock input: PRR= 1MHz, duty cycle 50%, Data input: PRR=500kHz, duty cycle 50%

Waveform-3 t_{PLH}, t_{PHL} (Enable T→Ripple Carry)



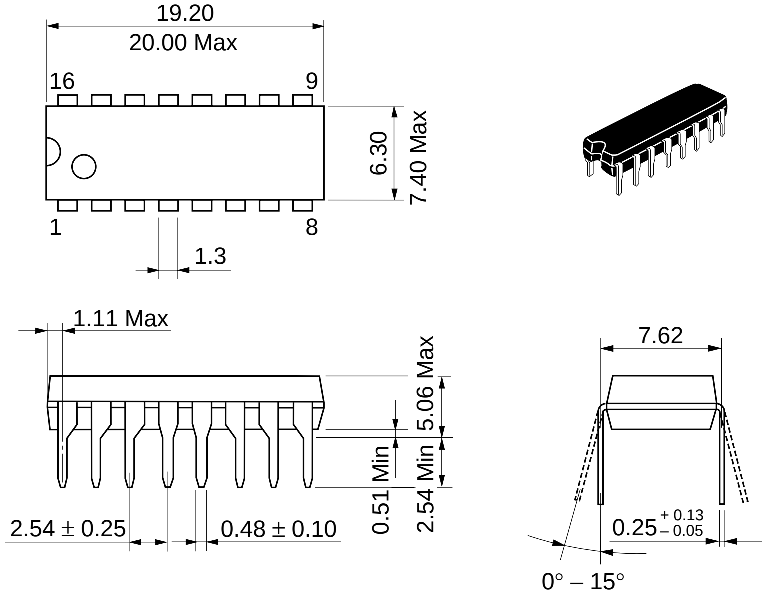
Note) Input pulse: $t_{TLH} \leq 15ns$, $t_{THL} \leq 6ns$, PRR=1MHz

Waveform-4 t_{PHL} (Clear→Q)



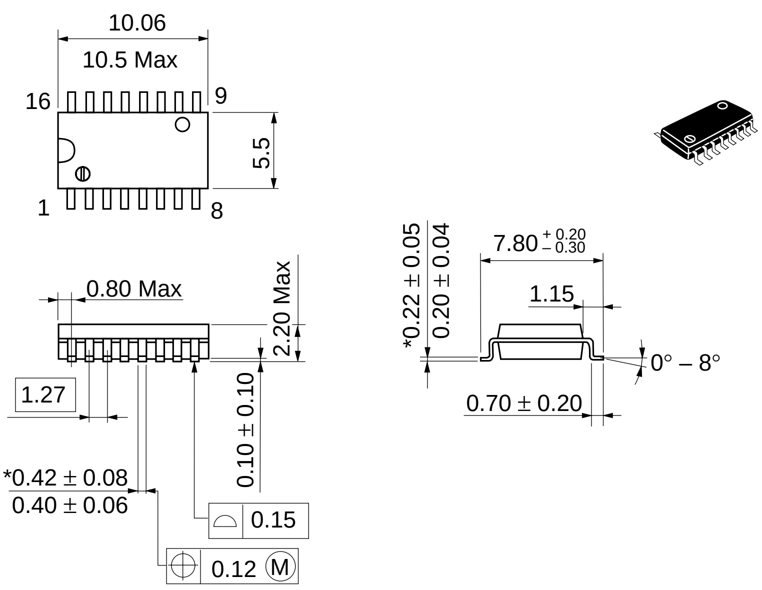
Note) Input pulse: $t_{TLH} \leq 15ns$, $t_{THL} \leq 6ns$

Unit: mm



Hitachi Code	DP-16
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	1.07 g

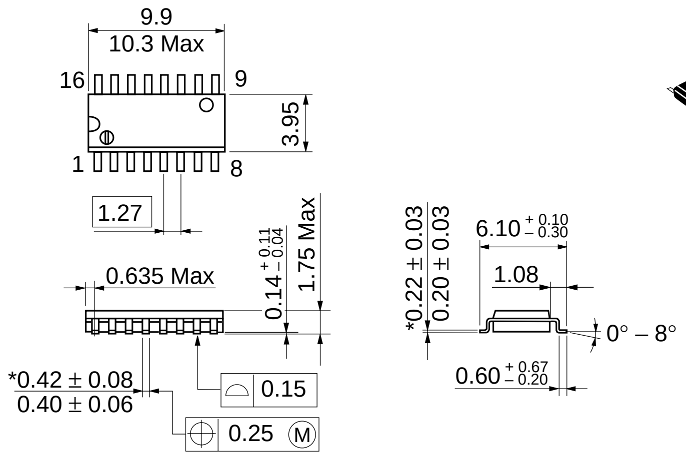
Unit: mm

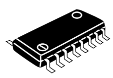


Hitachi Code	FP-16DA
JEDEC	—
EIAJ	Conforms
Weight (reference value)	0.24 g

*Dimension including the plating thickness
Base material dimension

Unit: mm





Hitachi Code	FP-16DN
JEDEC	Conforms
EIAJ	Conforms
Weight (reference value)	0.15 g

*Dimension including the plating thickness
Base material dimension

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