

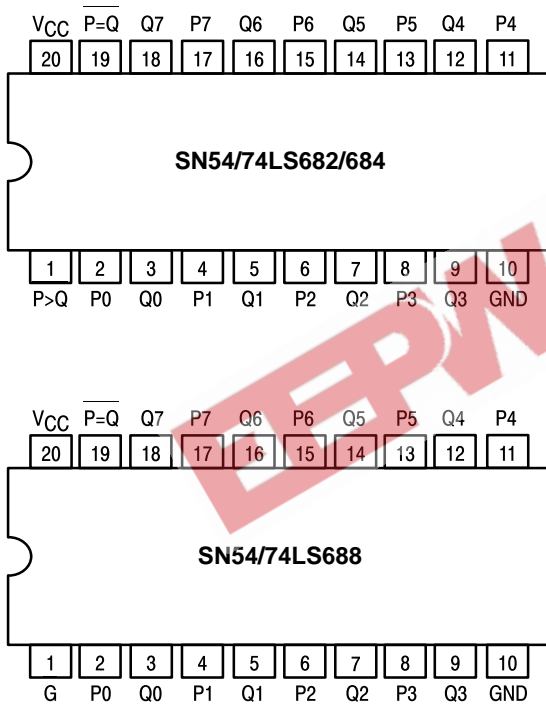


8-BIT MAGNITUDE COMPARATORS

The SN54/74LS682, 684, 688 are 8-bit magnitude comparators. These device types are designed to perform comparisons between two eight-bit binary or BCD words. All device types provide $P = Q$ outputs and the LS682 and LS684 have $P > Q$ outputs also.

The LS682, LS684 and LS688 are totem pole devices. The LS682 has a 20 k Ω pullup resistor on the Q inputs for analog or switch data.

CONNECTION DIAGRAMS (TOP VIEW)



TYPE	P = Q	P > Q	OUTPUT ENABLE	OUTPUT CONFIGURATION	PULLUP
LS682	yes	yes	no	totem-pole	yes
LS684	yes	yes	no	totem-pole	no
LS688	yes	no	yes	totem-pole	no

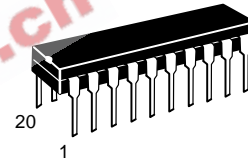
**SN54/74LS682
SN54/74LS684
SN54/74LS688**

8-BIT MAGNITUDE COMPARATORS

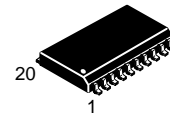
LOW POWER SCHOTTKY



**J SUFFIX
CERAMIC
CASE 732-03**



**N SUFFIX
PLASTIC
CASE 738-03**



**DW SUFFIX
SOIC
CASE 751D-03**

ORDERING INFORMATION

SN54LSXXXJ Ceramic
SN74LSXXXN Plastic
SN74LSXXXDW SOIC

FUNCTION TABLE

INPUTS			OUTPUTS	
DATA P, Q	ENABLES		$\overline{P = Q}$	$\overline{P > Q}$
	\overline{G} , GT	$\overline{G2}$		
P = Q	L	L	L	H
P > Q	L	L	H	L
P < Q	L	L	H	H
X	H	H	H	H

H = HIGH Level, L = LOW Level, X = Irrelevant

SN54/74LS682 • SN54/74LS684 • SN54/74LS688

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V _{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T _A	Operating Ambient Temperature Range	54 74	-55 0	25 25	125 70	°C
I _{OH}	Output Current — High	54, 74			-0.4	mA
I _{OL}	Output Current — Low	54 74			12 24	mA

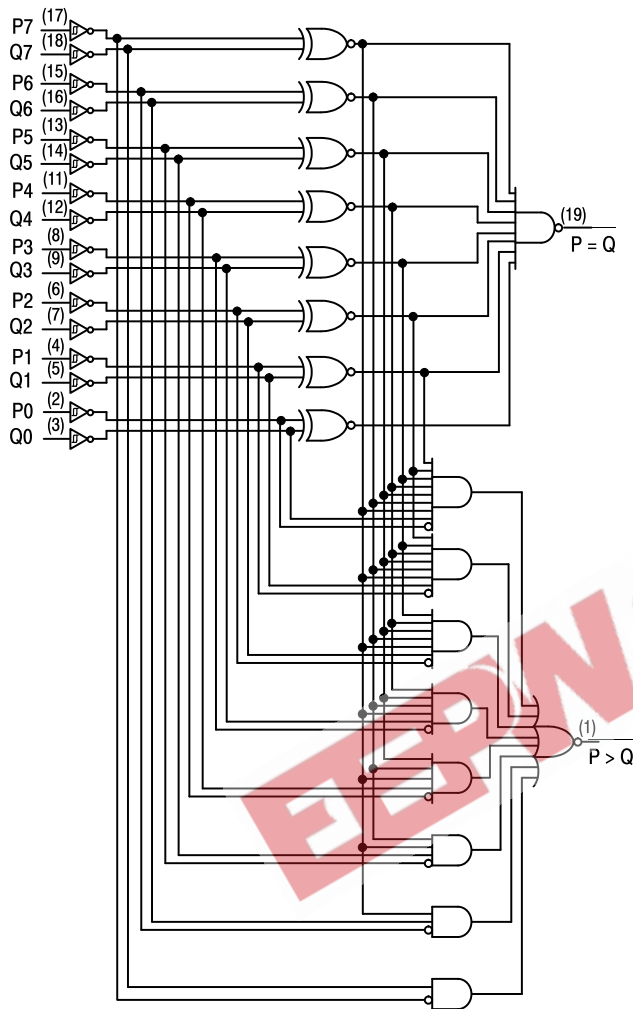
DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions	
		Min	Typ	Max			
V _{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V _{IL}	Input LOW Voltage	54		0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74		0.8			
V _{IK}	Input Clamp Diode Voltage		-0.65	-1.5	V	V _{CC} = MIN, I _{IN} = -18 mA	
V _{OH}	Output HIGH Voltage	54	2.5	3.5	V	V _{CC} = MIN, I _{OH} = MAX, V _{IN} = V _{IH} or V _{IL} per Truth Table	
		74	2.7	3.5	V		
V _{OL}	Output LOW Voltage	54, 74		0.25	0.4	I _{OL} = 12 mA	V _{CC} = V _{CC} MIN, V _{IN} = V _{IL} or V _{IH} per Truth Table
		74		0.35	0.5	I _{OL} = 24 mA	
I _{IH}	Input HIGH Current			20	μA	V _{CC} = MAX, V _{IN} = 2.7 V	
		LS628-Q Inputs		0.1	mA	V _{CC} = MAX, V _{IN} = 5.5 V	
		Others		0.1	mA	V _{CC} = MAX, V _{IN} = 7.0 V	
I _{IL}	Input LOW Current	LS682-Q Inputs		-0.4	mA	V _{CC} = MAX, V _{IN} = 0.4 V	
		Others		-0.2	mA		
I _{OS}	Short Circuit Current (Note 1)		-30	-130	mA	V _{CC} = MAX	
I _{CC}	Power Supply Current	LS682		70	mA	V _{CC} = MAX	
		LS684		65	mA		
		LS688		65	mA		

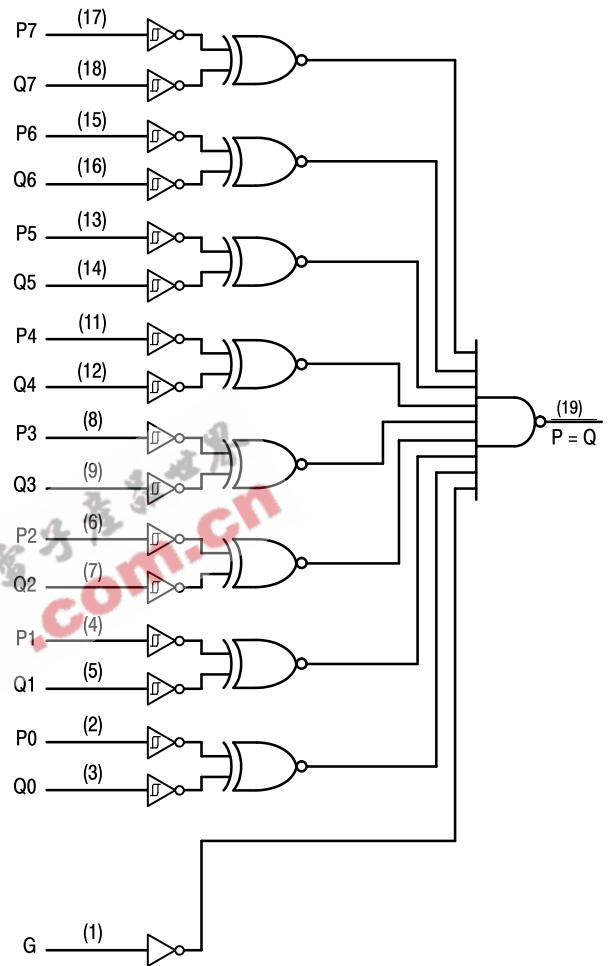
Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

SN54/74LS682 • SN54/74LS684 • SN54/74LS688

LOGIC DIAGRAMS



SN54/74LS682 thru LS684



SN54/74LS688

SN54/74LS682•SN54/74LS684•SN54/74LS688

AC CHARACTERISTICS (T_A = 25°C)

SN54/74LS682

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
t _{PLH} t _{PHL}	Propagation Delay, P to $\overline{P = Q}$		13 15	25 25	ns	V _{CC} = 5.0 V C _L = 45 pF R _L = 667 Ω
t _{PLH} t _{PHL}	Propagation Delay, Q to $\overline{P = Q}$		14 15	25 25	ns	
t _{PLH} t _{PHL}	Propagation Delay, P to $\overline{P > Q}$		20 15	30 30	ns	
t _{PLH} t _{PHL}	Propagation Delay, Q to $\overline{P > Q}$		21 19	30 30	ns	

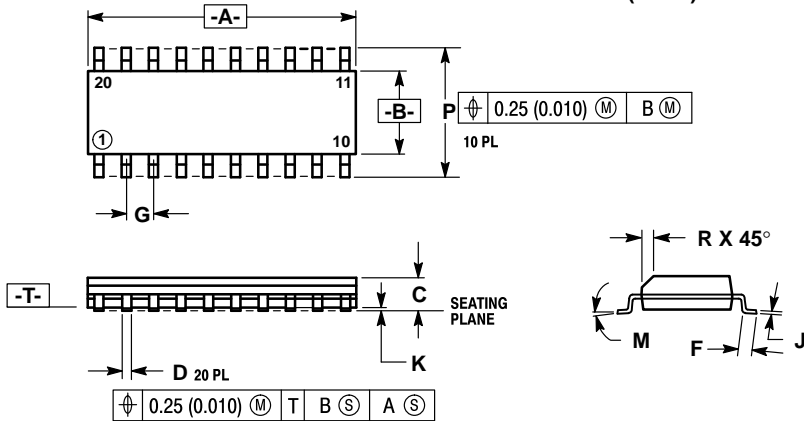
SN54/74LS684

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
t _{PLH} t _{PHL}	Propagation Delay, P to $\overline{P = Q}$		15 17	25 25	ns	V _{CC} = 5.0 V C _L = 45 pF R _L = 667 Ω
t _{PLH} t _{PHL}	Propagation Delay, Q to $\overline{P = Q}$		16 15	25 25	ns	
t _{PLH} t _{PHL}	Propagation Delay, P to $\overline{P > Q}$		22 17	30 30	ns	
t _{PLH} t _{PHL}	Propagation Delay, Q to $\overline{P > Q}$		24 20	30 30	ns	

SN54/74LS688

Symbol	Parameter	Limits			Unit	Test Conditions
		Min	Typ	Max		
t _{PLH} t _{PHL}	Propagation Delay, P to $\overline{P = Q}$		12 17	18 23	ns	V _{CC} = 5.0 V C _L = 45 pF R _L = 667 Ω
t _{PLH} t _{PHL}	Propagation Delay, Q to $\overline{P = Q}$		12 17	18 23	ns	
t _{PLH} t _{PHL}	Propagation Delay, $\overline{G}, \overline{G1}$ to $\overline{P = Q}$		12 13	18 20	ns	

**Case 751D-03 DW Suffix
20-Pin Plastic
SO-20 (WIDE)**

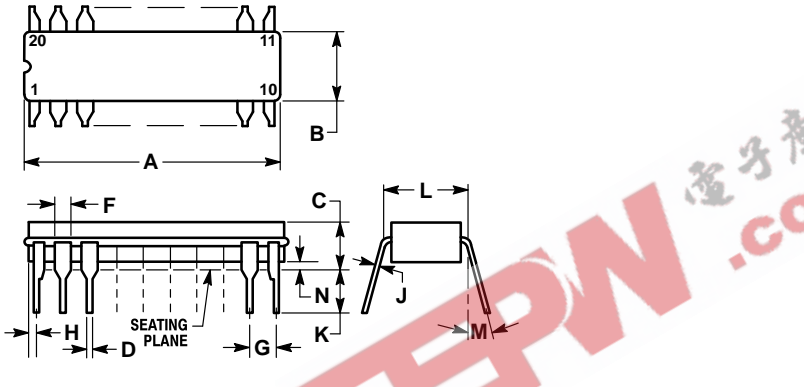


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. 751D-01, AND -02 OBSOLETE, NEW STANDARD 751D-03.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	12.65	12.95	0.499	0.510
B	7.40	7.60	0.292	0.299
C	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.50	0.90	0.020	0.035
G	1.27 BSC		0.050 BSC	
J	0.25	0.32	0.010	0.012
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	10.05	10.55	0.395	0.415
R	0.25	0.75	0.010	0.029

**Case 732-03 J Suffix
20-Pin Ceramic Dual In-Line**

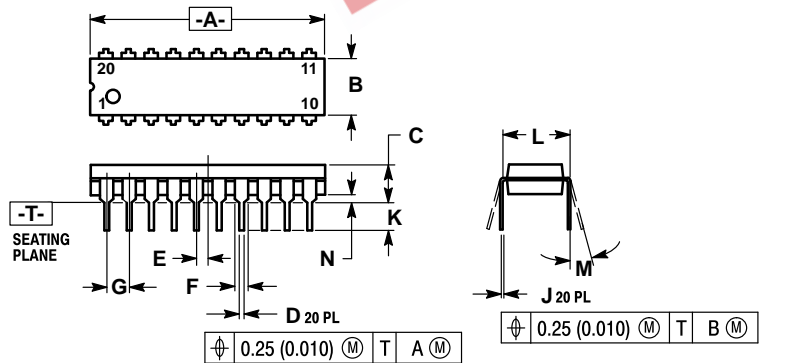


NOTES:

1. LEADS WITHIN 0.25 mm (0.010) DIA., TRUE POSITION AT SEATING PLANE, AT MAXIMUM MATERIAL CONDITION.
2. DIM L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIM A AND B INCLUDES MENISCUS.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	23.88	25.15	0.940	0.990
B	6.60	7.49	0.260	0.295
C	3.81	5.08	0.150	0.200
D	0.38	0.56	0.015	0.022
F	1.40	1.65	0.055	0.065
G	2.54 BSC		0.100 BSC	
H	0.51	1.27	0.020	0.050
J	0.20	0.30	0.008	0.012
K	3.18	4.06	0.125	0.160
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.25	1.02	0.010	0.040

**Case 738-03 N Suffix
20-Pin Plastic**




NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION "L" TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSION "B" DOES NOT INCLUDE MOLD FLASH.
5. 738-02 OBSOLETE, NEW STANDARD 738-03.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	25.66	27.17	1.010	1.070
B	6.10	6.60	0.240	0.260
C	3.81	4.57	0.150	0.180
D	0.39	0.55	0.015	0.022
E	1.27 BSC		0.050 BSC	
F	1.27	1.77	0.050	0.070
G	2.54 BSC		0.100 BSC	
J	0.21	0.38	0.008	0.015
K	2.80	3.55	0.110	0.140
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.51	1.01	0.020	0.040

EEPW 电子產品世界
www.eepw.com.cn

Motorola reserves the right to make changes without further notice to any products herein. Motorola makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does Motorola assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. "Typical" parameters can and do vary in different applications. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. Motorola does not convey any license under its patent rights nor the rights of others. Motorola products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the Motorola product could create a situation where personal injury or death may occur. Should Buyer purchase or use Motorola products for any such unintended or unauthorized application, Buyer shall indemnify and hold Motorola and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that Motorola was negligent regarding the design or manufacture of the part. Motorola and  are registered trademarks of Motorola, Inc. Motorola, Inc. is an Equal Opportunity/Affirmative Action Employer.

Literature Distribution Centers:

USA: Motorola Literature Distribution; P.O. Box 20912; Phoenix, Arizona 85036.

EUROPE: Motorola Ltd.; European Literature Centre; 88 Tanners Drive, Blakelands, Milton Keynes, MK14 5BP, England.

JAPAN: Nippon Motorola Ltd.; 4-32-1, Nishi-Gotanda, Shinagawa-ku, Tokyo 141, Japan.

ASIA PACIFIC: Motorola Semiconductors H.K. Ltd.; Silicon Harbour Center, No. 2 Dai King Street, Tai Po Industrial Estate, Tai Po, N.T., Hong Kong.

SYMBOL	SW1	SW2
tPZH	Open	Closed
tPZL	Closed	Open
tPLZ	Closed	Closed

