

## 74VHC273 Octal D-Type Flip-Flop

### General Description

The VHC273 is an advanced high speed CMOS Octal D-type flip-flop fabricated with silicon gate CMOS technology. It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

The register has a common buffered Clock (CP) which is fully edge-triggered. The state of each D input, one setup time before the LOW-to-HIGH clock transition, is transferred to the corresponding flip-flop's Q output. The Master Reset ( $\overline{\text{MR}}$ ) input will clear all flip-flops simultaneously. All outputs will be forced LOW independently of Clock or Data inputs by a LOW voltage level on the  $\overline{\text{MR}}$  input.

An input protection circuit insures that 0V to 7V can be applied to the inputs pins without regard to the supply voltage. This device can be used to interface 5V to 3V systems and two supply systems such as battery backup. This circuit prevents device destruction due to mismatched supply and input voltages.

### Features

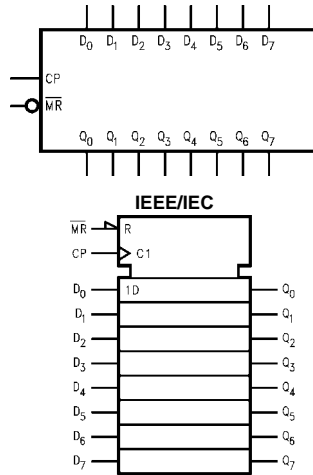
- High Speed:  $f_{\text{MAX}} = 165 \text{ MHz}$  (typ) at  $V_{\text{CC}} = 5\text{V}$
- Low power dissipation:  $I_{\text{CC}} = 4 \mu\text{A}$  (max) at  $T_{\text{A}} = 25^\circ\text{C}$
- High noise immunity:  $V_{\text{NIH}} = V_{\text{NIL}} = 28\% V_{\text{CC}}$  (min)
- Power down protection is provided on all inputs
- Low noise:  $V_{\text{OLP}} = 0.9\text{V}$  (max)
- Pin and function compatible with 74HC273
- Leadless DQFN Package

### Ordering Code:

Order Number	Package Number	Package Description
74VHC273M	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
74VHC273SJ	M20D	Pb-Free 20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74VHC273BQ (Preliminary)	MLP020B (Preliminary)	Pb-Free 20-Terminal Depopulated Quad Very-Thin Flat Pack No Leads (DQFN), JEDEC MO-241, 2.5 x 4.5mm
74VHC273MTC	MTC20	20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
74VHC273N	N20A	20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

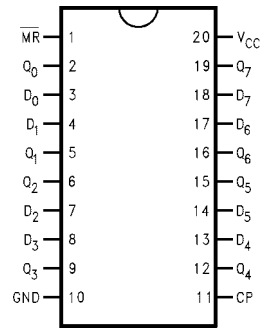
Surface mount packages are also available on Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.  
Pb-Free package per JEDEC J-STD-020B.

### Logic Symbols

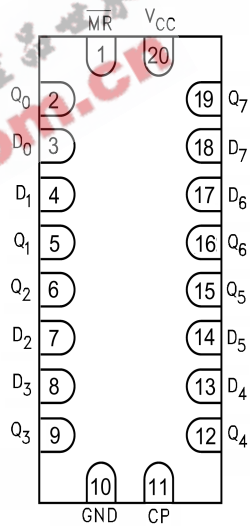


### Connection Diagrams

Pin Assignments for PDIP, SOIC, SOP, and TSSOP



Pad Assignments for DQFN



(Top Through View)

### Pin Descriptions

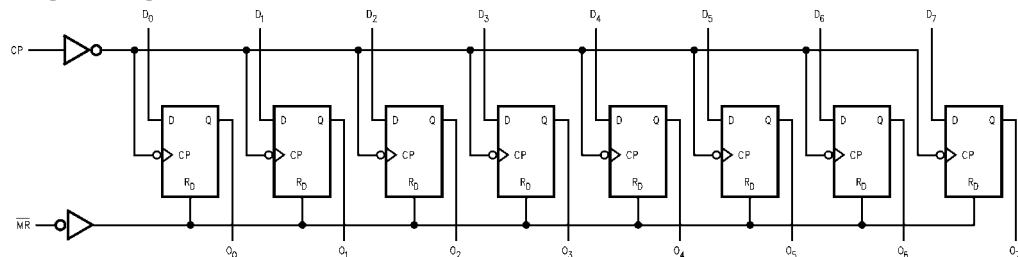
Pin Names	Description
D <sub>0</sub> -D <sub>7</sub>	Data Inputs
$\overline{\text{MR}}$	Master Reset
CP	Clock Pulse Input
Q <sub>0</sub> -Q <sub>7</sub>	Data Outputs

### Function Table

Operating Mode	Inputs			Outputs
	$\overline{\text{MR}}$	CP	D <sub>n</sub>	Q <sub>n</sub>
Reset (Clear)	L	X	X	L
Load '1'	H	↗	H	H
Load '0'	H	↘	L	L

H = HIGH Voltage Level  
 L = LOW Voltage Level  
 X = Immaterial  
 ↗ = LOW-to-HIGH Transition

### Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

**Absolute Maximum Ratings** (Note 1)

Supply Voltage ( $V_{CC}$ )	-0.5V to +7.0V
DC Input Voltage ( $V_{IN}$ )	-0.5V to +7.0V
DC Output Voltage ( $V_{OUT}$ )	-0.5V to $V_{CC} + 0.5V$
Input Diode Current ( $I_{IK}$ )	-20 mA
Output Diode Current ( $I_{OK}$ )	$\pm 20$ mA
DC Output Current ( $I_{OUT}$ )	$\pm 25$ mA
DC $V_{CC}$ /GND Current ( $I_{CC}$ )	$\pm 75$ mA
Storage Temperature ( $T_{STG}$ )	-65°C to +150°C
Lead Temperature ( $T_L$ ) (Soldering, 10 seconds)	260°C

**Recommended Operating Conditions** (Note 2)

Supply Voltage ( $V_{CC}$ )	2.0V to +5.5V
Input Voltage ( $V_{IN}$ )	0V to +5.5V
Output Voltage ( $V_{OUT}$ )	0V to $V_{CC}$
Operating Temperature ( $T_{OPR}$ )	-40°C to +85°C
Input Rise and Fall Time ( $t_r, t_f$ )	
$V_{CC} = 3.3V \pm 0.3V$	0 ns/V ~ 100 ns/V
$V_{CC} = 5.0V \pm 0.5V$	0 ns/V ~ 20 ns/V

**Note 1:** Absolute Maximum Ratings are values beyond which the device may be damaged or have its useful life impaired. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. Fairchild does not recommend operation outside databook specifications.

**Note 2:** Unused inputs must be held HIGH or LOW. They may not float.

**DC Electrical Characteristics**

Symbol	Parameter	$V_{CC}$ (V)	$T_A = 25^\circ\text{C}$			$T_A = -40^\circ\text{C to } +85^\circ\text{C}$		Units	Conditions	
			Min	Typ	Max	Min	Max			
$V_{IH}$	HIGH Level Input Voltage	2.0 3.0 – 5.5	1.50 0.7 $V_{CC}$			1.50 0.7 $V_{CC}$		V		
$V_{IL}$	LOW Level Input Voltage	2.0 3.0 – 5.5			0.50 0.3 $V_{CC}$	0.50 0.3 $V_{CC}$		V		
$V_{OH}$	HIGH Level Output Voltage	2.0	1.9	2.0		1.9		V	$V_{IN} = V_{IH}$ or $V_{IL}$	$I_{OH} = -50 \mu\text{A}$
		3.0	2.9	3.0		2.9				
		4.5	4.4	4.5		4.4		V	$I_{OH} = -4 \text{ mA}$ $I_{OH} = -8 \text{ mA}$	
		3.0	2.58			2.48				
4.5	3.94			3.80						
$V_{OL}$	LOW Level Output Voltage	2.0		0.0	0.1		0.1	V	$V_{IN} = V_{IH}$ or $V_{IL}$	$I_{OL} = 50 \mu\text{A}$
		3.0		0.0	0.1		0.1			
		4.5		0.0	0.1		0.1	V	$I_{OL} = 4 \text{ mA}$ $I_{OL} = 8 \text{ mA}$	
		3.0			0.36		0.44			
4.5			0.36		0.44					
$I_{IN}$	Input Leakage Current	0 – 5.5			$\pm 0.1$		$\pm 1.0$	$\mu\text{A}$	$V_{IN} = 5.5V$ or GND	
$I_{CC}$	Quiescent Supply Current	5.5			4.0		40.0	$\mu\text{A}$	$V_{IN} = V_{CC}$ or GND	

**Noise Characteristics**

Symbol	Parameter	$V_{CC}$ (V)	$T_A = 25^\circ\text{C}$		Units	Conditions
			Typ	Limits		
$V_{OLP}$ (Note 3)	Quiet Output Maximum Dynamic $V_{OL}$	5.0	0.6	0.9	V	$C_L = 50 \text{ pF}$
$V_{OLV}$ (Note 3)	Quiet Output Minimum Dynamic $V_{OL}$	5.0	-0.6	-0.9	V	$C_L = 50 \text{ pF}$
$V_{IHD}$ (Note 3)	Minimum HIGH Level Dynamic Input Voltage	5.0		3.5	V	$C_L = 50 \text{ pF}$
$V_{ILD}$ (Note 3)	Maximum LOW Level Dynamic Input Voltage	5.0		1.5	V	$C_L = 50 \text{ pF}$

**Note 3:** Parameter guaranteed by design.

AC Electrical Characteristics									
Symbol	Parameter	V <sub>CC</sub> (V)	T <sub>A</sub> = 25°C			T <sub>A</sub> = -40°C to +85°C		Units	Conditions
			Min	Typ	Max	Min	Max		
f <sub>MAX</sub>	Maximum Clock Frequency	3.3 ± 0.3	75	120		65		MHz	C <sub>L</sub> = 15 pF
			50	75		45			C <sub>L</sub> = 50 pF
		5.0 ± 0.5	120	165		100		MHz	C <sub>L</sub> = 15 pF
			80	110		70			C <sub>L</sub> = 50 pF
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay Time (CK - Q)	3.3 ± 0.3	8.7	13.6		1.0	16.0	ns	C <sub>L</sub> = 15 pF
			11.2	17.1		1.0	19.5		C <sub>L</sub> = 50 pF
		5.0 ± 0.5	5.8	9.0		1.0	10.5	ns	C <sub>L</sub> = 15 pF
			7.3	11.0		1.0	12.5		C <sub>L</sub> = 50 pF
t <sub>PHL</sub>	Propagation Delay Time (MR - Q)	3.3 ± 0.3	8.9	13.6		1.0	16.0	ns	C <sub>L</sub> = 15 pF
			11.4	17.1		1.0	19.5		C <sub>L</sub> = 50 pF
		5.0 ± 0.5	5.2	8.5		1.0	10.0	ns	C <sub>L</sub> = 15 pF
			6.7	10.5		1.0	12.0		C <sub>L</sub> = 50 pF
t <sub>OSLH</sub> t <sub>OSHL</sub>	Output to Output Skew	3.3 ± 0.3		1.5		1.5	ns	(Note 4)	C <sub>L</sub> = 50 pF
5.0 ± 0.5			1.0		1.0	C <sub>L</sub> = 50 pF			
C <sub>IN</sub>	Input Capacitance		4.0	10.0		10.0	pF	V <sub>CC</sub> = Open	
C <sub>PD</sub>	Power Dissipation Capacitance		31				pF	(Note 5)	

**Note 4:** Parameter guaranteed by design t<sub>OSLH</sub> = |t<sub>PLHmax</sub> - t<sub>PLHmin</sub>|; t<sub>OSHL</sub> = |t<sub>PHLmax</sub> - t<sub>PHLmin</sub>|.

**Note 5:** C<sub>PD</sub> is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained from the equation: I<sub>CC (opr.)</sub> = C<sub>PD</sub> \* V<sub>CC</sub> \* f<sub>IN</sub> + I<sub>CC</sub>/8 (per F/F). The total C<sub>PD</sub> when n pieces of the Flip-Flop operates can be calculated by the equation: C<sub>PD (total)</sub> = 22 + 9n.

### AC Operating Requirements

Symbol	Parameter	V <sub>CC</sub> (V) (Note 6)	T <sub>A</sub> = 25°C		T <sub>A</sub> = -40°C to +85°C		Units
			Typ	Guaranteed Minimum			
t <sub>W(L)</sub>	Minimum Pulse Width (CK)	3.3		5.5	6.5	ns	
t <sub>W(H)</sub>		5.0		5.0	5.0		
t <sub>W(L)</sub>	Minimum Pulse Width (MR)	3.3		5.0	6.0	ns	
		5.0		5.0	5.0		
t <sub>S</sub>	Minimum Setup Time	3.3		5.5	6.5	ns	
		5.0		4.5	4.5		
t <sub>H</sub>	Minimum Hold Time	3.3		1.0	1.0	ns	
		5.0		1.0	1.0		
t <sub>REC</sub>	Minimum Removal Time (MR)	3.3		2.5	2.5	ns	
		5.0		2.0	2.0		

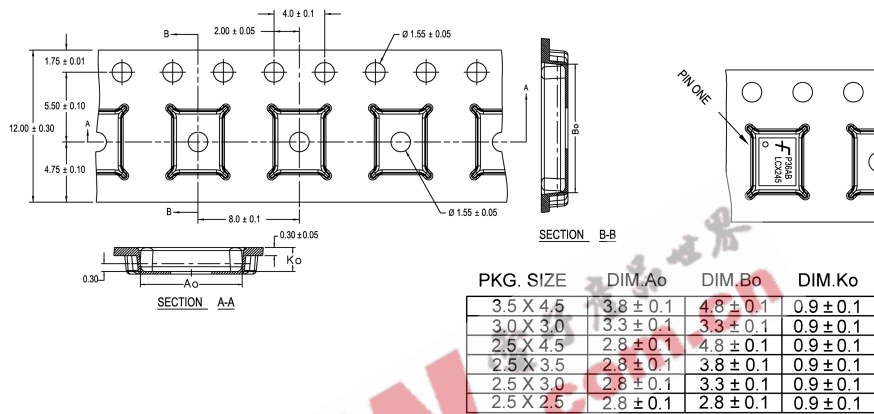
**Note 6:** V<sub>CC</sub> is 3.3 ± 0.3V or 5.0 ± 0.5V

### Tape and Reel Specification

Tape Format for DQFN

Package Designator	Tape Section	Number Cavities	Cavity Status	Cover Tape Status
BQ	Leader (Start End)	125 (typ)	Empty	Sealed
	Carrier	2500/3000	Filled	Sealed
	Trailer (Hub End)	75 (typ)	Empty	Sealed

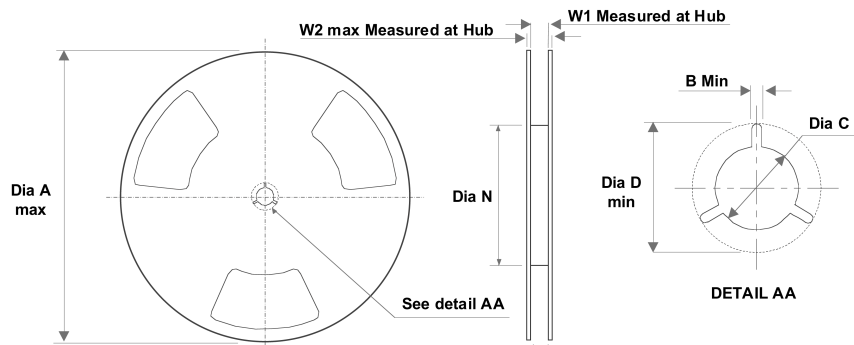
**TAPE DIMENSIONS** inches (millimeters)



NOTES: unless otherwise specified

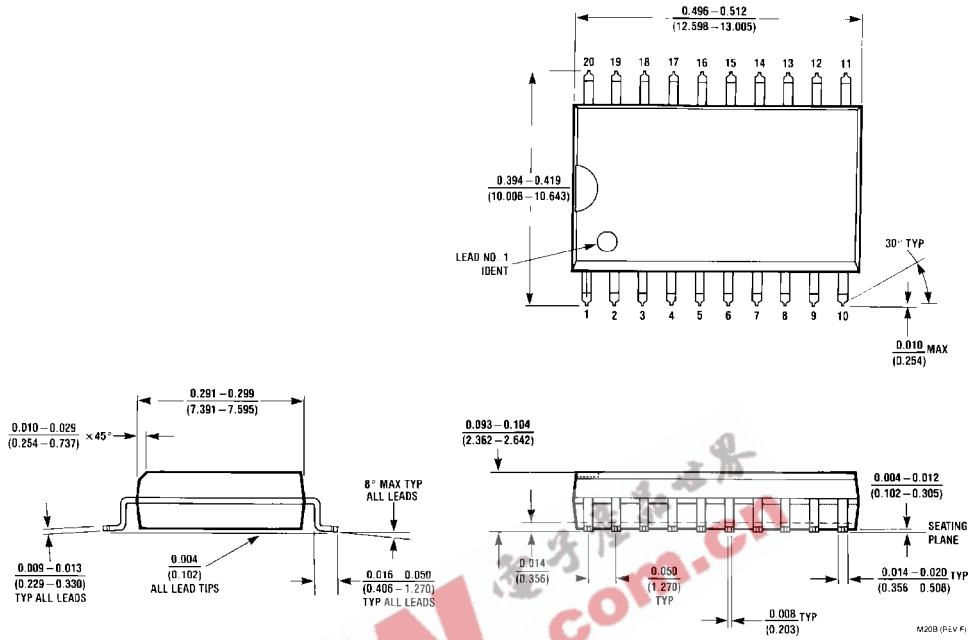
- Cumulative pitch for feeding holes and cavities (chip pockets) not to exceed 0.008[0.20] over 10 pitch span.
- Smallest allowable bending radius.
- Thru hole inside cavity is centered within cavity.
- Tolerance is ±0.002[0.05] for these dimensions on all 12mm tapes.
- Ao and Bo measured on a plane 0.120[0.30] above the bottom of the pocket.
- Ko measured from a plane on the inside bottom of the pocket to the top surface of the carrier.
- Pocket position relative to sprocket hole measured as true position of pocket. Not pocket hole.
- Controlling dimension is millimeter. Dimension in inches rounded.

**REEL DIMENSIONS** inches (millimeters)



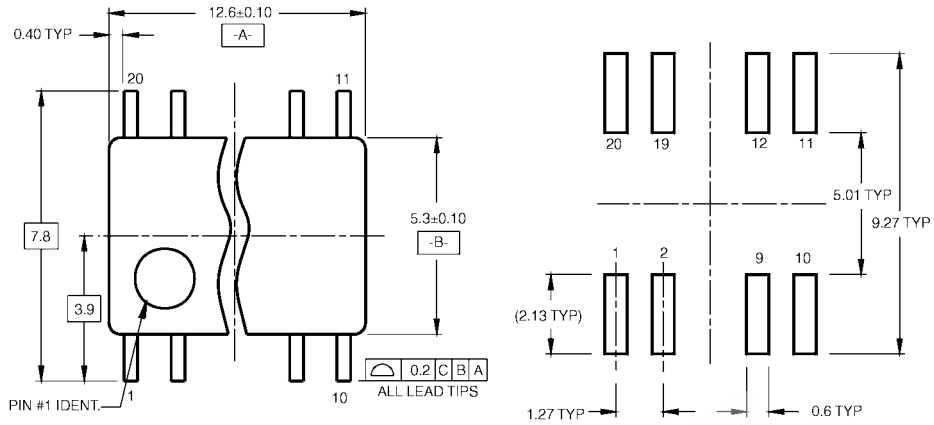
Tape Size	A	B	C	D	N	W1	W2
12 mm	13.0 (330)	0.059 (1.50)	0.512 (13.00)	0.795 (20.20)	7.008 (178)	0.488 (12.4)	0.724 (18.4)

**Physical Dimensions** inches (millimeters) unless otherwise noted



20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide  
Package Number M20B

**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



LAND PATTERN RECOMMENDATION



DIMENSIONS ARE IN MILLIMETERS

NOTES:

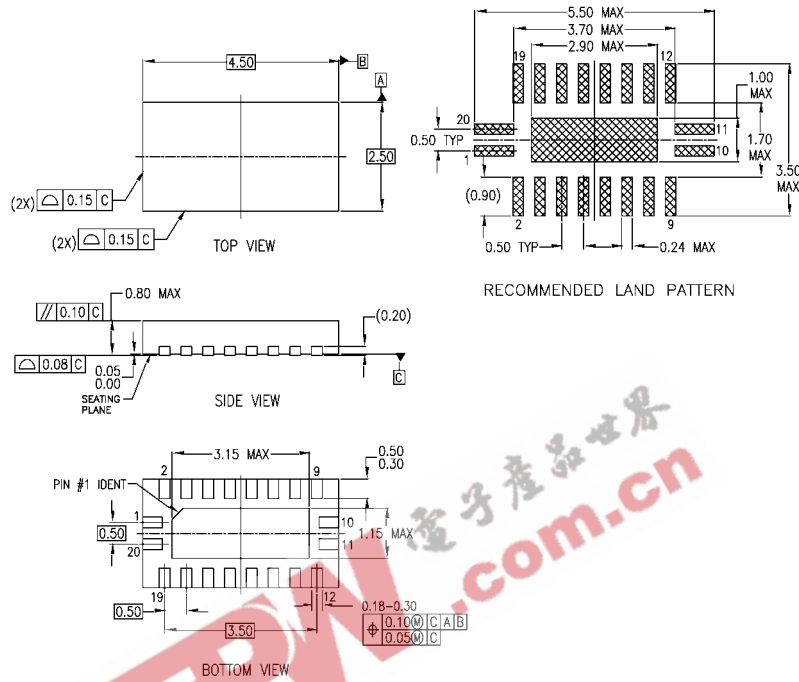
- A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

M20DRevB1

DETAIL A

**Pb-Free 20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide  
Package Number M20D**

**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



NOTES:

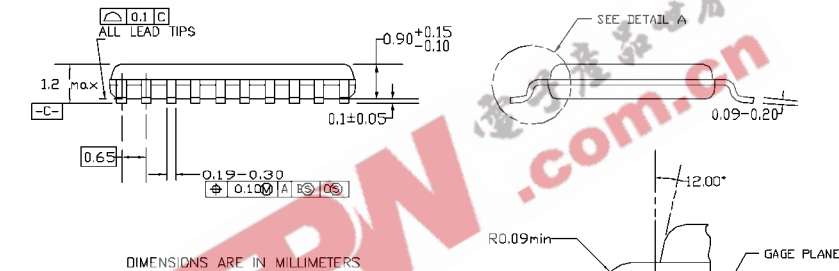
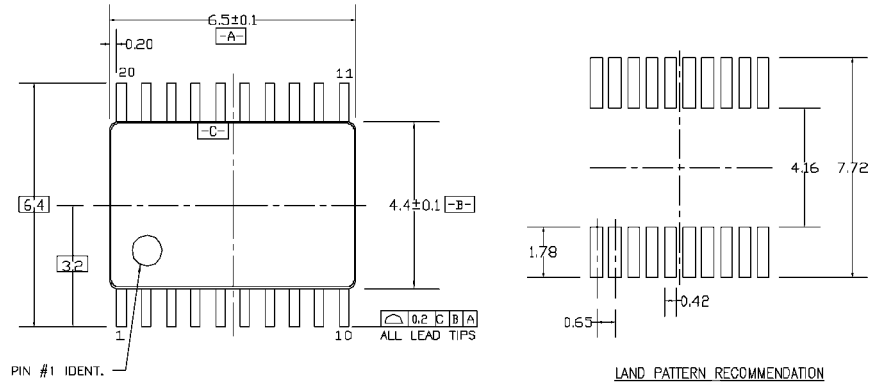
- A. CONFORMS TO JEDEC REGISTRATION MO-241, VARIATION AC
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994

MLP020BrevA

**Pb-Free 20-Terminal Depopulated Quad Very-Thin Flat Pack No Leads (DQFN), JEDEC MO-241, 2.5 x 4.5mm  
Package Number MLP020B  
(Preliminary)**



**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



DIMENSIONS ARE IN MILLIMETERS

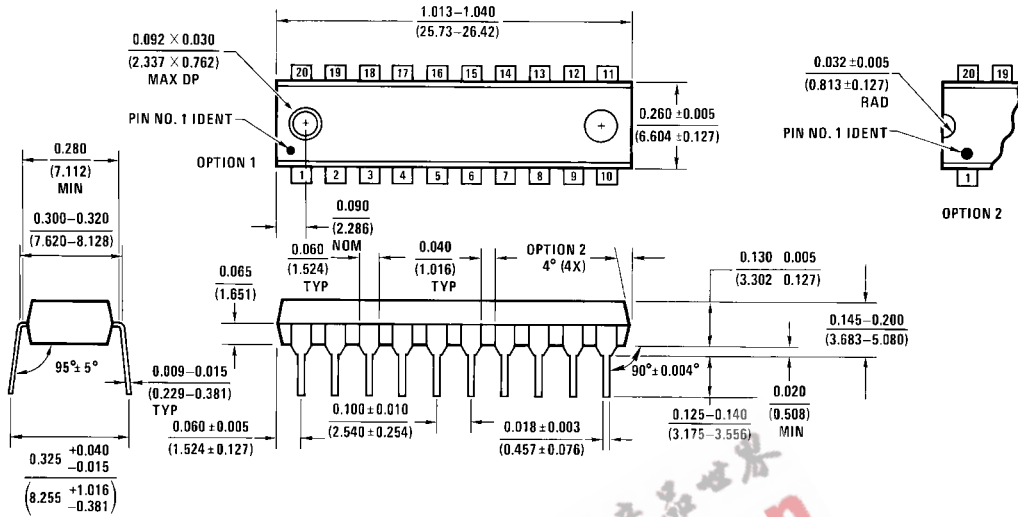
NOTES:

- A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AC, REF NOTE 6, DATE 7/93.
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLDS FLASH, AND TIE BAR EXTRUSIONS.
- D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.

MTC20REVD1

**20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide  
Package Number MTC20**

**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide  
Package Number N20A

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