DATA SHEET

74F711A, 74F711-1, 74F712A, 74F712-1
Multiplexers

Product specification

1990 Dec 13

IC15 Data Handbook

Philips
Semiconductors

PHILIPS

Multiplexers

74F711A   Quint 2-to-1 Data Selector Multiplexer (3-State)
74F711-1   Quint 2-to-1 Data Selector Multiplexer with 30Ω Equivalent Output Termination Impedance (3-State)
74F712A   Quint 3-to-1 Data Selector Multiplexer
74F712-1   Quint 3-to-1 Data Selector Multiplexer with 30Ω Equivalent Output Termination Impedance

FEATURES for 74F711A/74F711-1

- Consists of five 2-to-1 Multiplexers
- High impedance PNP base inputs for reduced loading (20μA in High and Low states)
- Designed for address multiplexing of dynamic RAM and other applications
- Output inverting/non-inverting option
- 30Ω termination impedance on each output – 74F711-1
- Outputs sink 64mA (74F711A only)

FEATURES for 74F712A/74F712-1

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- High impedance PNP base inputs for reduced loading (20μA in High and Low states)
- Designed for address multiplexing of dynamic RAM and other applications
- 30Ω termination impedance on each output – 74F712-1
- Outputs sink 64mA (74F712A only)

DESCRIPTION

The 74F711A/74F711-1 consist of five 2-to-1 multiplexers designed for address multiplexing of dynamic RAMs and other multiplexing applications. The 74F711A has a common select (S) input, an Output Enable ($\overline{OE}$) input and an Output Inverting ($\overline{INV}$) input to control the 3-State outputs. The outputs source 15mA and sink 64mA. The 74F711-1 is the same as the 74F711A except that is has a 30Ω termination impedance on each output to reduce line noise and the 3-State outputs sink 5mA.

When the inverting input ($\overline{INV}$) is Low, the input data path is inverted.

To improve speed and noise immunity, V_{CC} and GND side pins are used.

The 74F712A/74F712-1 consist of five 3-to1 multiplexers designed for address multiplexing of dynamic RAMs and other multiplexing applications. The 74F712A has two select (S0, S1) inputs to determine which set of five inputs will be propagated to the five outputs. The outputs source 15mA and sink 64mA. The 74F712-1 is the same as the 74F712A except that it has a 30Ω termination impedance on each output to reduce line noise and the outputs sink 5mA.
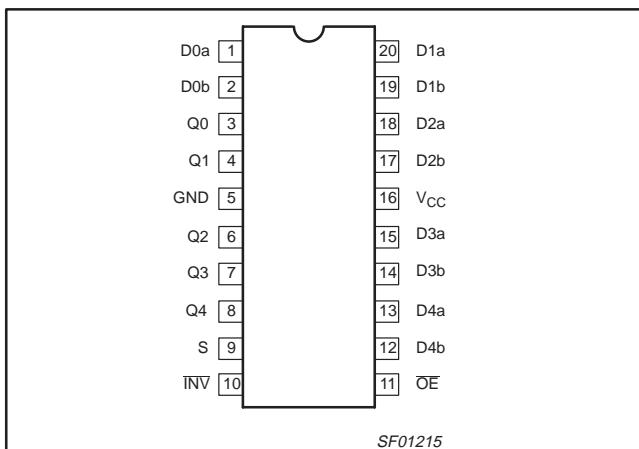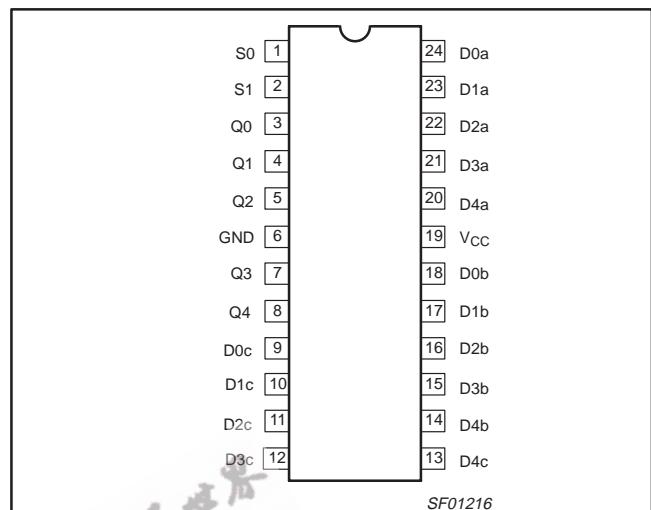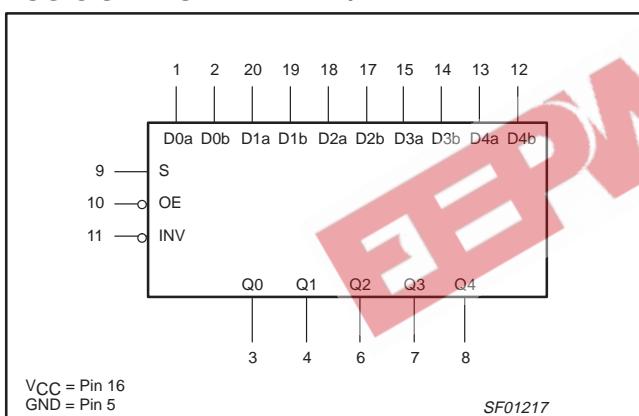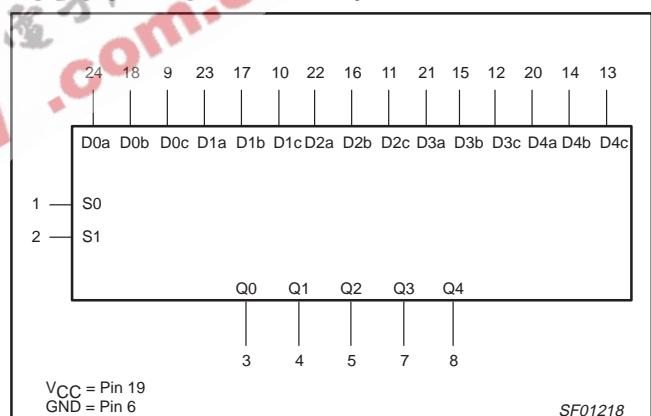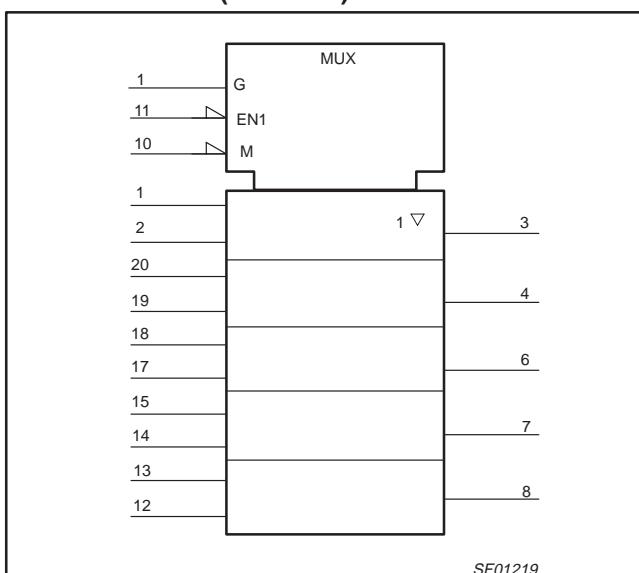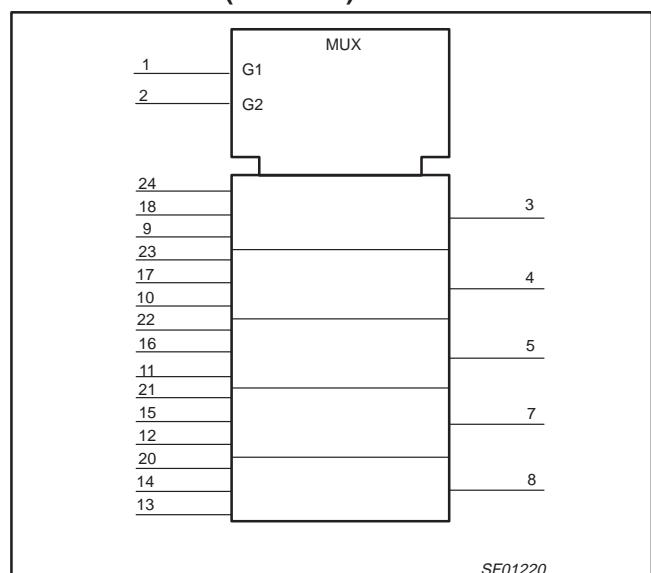
TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F711A	6.0ns	30mA
74F711-1	6.5ns	29mA
74F712A	6.5ns	25mA
74F712-1	6.5ns	25mA

ORDERING INFORMATION

| DESCRIPTION	COMMERCIAL RANGE V_{CC} = 5V ± 10% T_{amb} = 0° C to +70°C	PKG DWG #
20-Pin Plastic DIP	N74F711AN, N74F711-1N	SOT146-1
24-Pin Plastic Slim DIP (300 mil)	N74F712AN, N74F712-1N	SOT222-1
20-Pin Plastic SOL	N74F711AD, N74F711-1D	SOT163-1
24-Pin Plastic SOL	N74F712AD, N74F712-1D	SOT137-1

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS		DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
74F711A/ 74F711-1	Dna, Dnb	Data inputs	1.0/0.066	20μA/40μA
	S	Select input	1.0/0.033	20μA/20μA
	$\overline{OE}$	Output Enable input (active Low)	1.0/0.033	20μA/20μA
	$\overline{INV}$	Output inverting input (active Low)	1.0/0.033	20μA/20μA
	Q0 - Q4	Data outputs for 74F711A	750/106.7	15mA/64mA
	Q0 - Q4	Data outputs for 74F711-1	750/8.33	15mA/5mA
74F712A/ 74F712-1	Dna, Dnb, Dnc	Data inputs	1.0/0.066	20μA/40μA
	S0, S1	Select inputs	1.0/0.033	20μA/20μA
	Q0 - Q4	Data outputs for 74F712A	750/106.7	15mA/64mA
	Q0 - Q4	Data outputs for 74F712-1	750/8.33	15mA/5mA

NOTE: One (1.0) FAST Unit Load (U.L.) is defined as: 20μA in the High state and 0.6mA in the Low state.

Multiplexers

PIN CONFIGURATION – 74F711A/74F711-1

SF01215

PIN CONFIGURATION – 74F712A/74F712-1

SF01216

LOGIC SYMBOL – 74F711A/74F711-1

V_{CC} = Pin 16
GND = Pin 5

SF01217

LOGIC SYMBOL – 74F712A/74F712-1

V_{CC} = Pin 19
GND = Pin 6

SF01218

LOGIC SYMBOL (IEEE/IEC) – 74F711A/74F711-1

SF01219

LOGIC SYMBOL (IEEE/IEC) – 74F712A/74F712-1

SF01220

Multiplexers

LOGIC DIAGRAM – 74F711A/74F711-1

SF01221

V_{CC} = Pin 16
GND = Pin 5

FUNCTION TABLE – 74F711A/74F711-1

INPUTS					OUTPUT
S	$\overline{INV}$	$\overline{OE}$	Dna	Dnb	Qn
L	L	L	Data a	Data b	$\overline{Data\ a}$
H	L	L	Data a	Data b	$\overline{Data\ b}$
L	H	L	Data a	Data b	Data a
H	H	L	Data a	Data b	Data b
X	X	H	X	X	Z
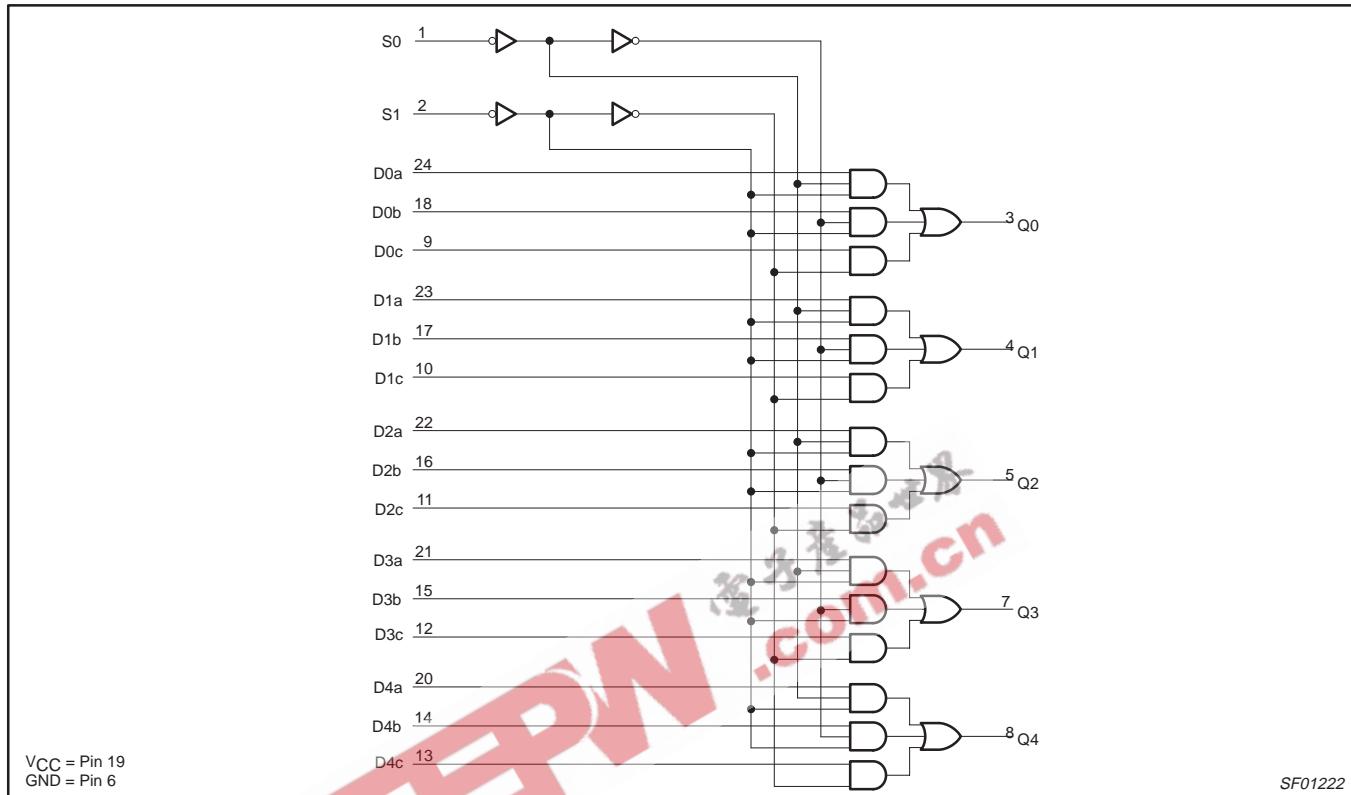
H = High voltage level
L = Low voltage level
X = Don't care
Z = High impedance "off" state

Multiplexers

LOGIC DIAGRAM – 74F712A/74F712-1

V_{CC} = Pin 19
GND = Pin 6

SF01222

FUNCTION TABLE – 74F712A/74F712-1

INPUTS					OUTPUT
S0	S1	Dna	Dnb	Dnc	Qn
L	L	Data a	Data b	Data c	Data a
H	L	Data a	Data b	Data c	Data b
X	H	Data a	Data b	Data c	Data c

H = High voltage level
L = Low voltage level
X = Don't care

ABSOLUTE MAXIMUM RATINGS

Operation beyond the limits set forth in this table may impair the useful life of the device.
Unless otherwise noted these limits are over the operating free-air temperature range.

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		−0.5 to +7.0	V
V_{IN}	Input voltage		−0.5 to +7.0	V
I_{IN}	Input current		−30 to +5	mA
V_{OUT}	Voltage applied to output in High output state		−0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	74F711A, 74F712A	96	mA
		74F711-1, 74F712-1	10	mA
T_{amb}	Operating free-air temperature range		0 to +70	°C
T_{stg}	Storage temperature		−65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
I_{IK}	Input clamp current				−18	mA
I_{OH}	High-level output current				−15	mA
I_{OL}	Low-level output current	74F711A, 74F712A			64	mA
		74F711-1, 74F712-1			5	mA
T_{amb}	Operating free-air temperature		0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			LIMITS			UNIT
						MIN	TYP[2]	MAX	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH} = –3mA	±10%V_{CC}	2.4			V
					±5%V_{CC}	2.7	3.4		V
				I_{OH} = –15mA	±10%V_{CC}	2.0			V
					±5%V_{CC}	2.0			V
V_{OL}	Low-level output voltage	74F711A/ 74F712A only	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL} = MAX	±10%V_{CC}		0.38	0.55	V
					±5%V_{CC}		0.42	0.55	V
		74F711-1/ 74F712-1		I_{OL} = 5mA	±10%V_{CC}		0.38	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				–0.73	–1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V					100	µA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	Low-level input current	Others	V_{CC} = MAX, V_I = 0.5V					–20	µA
		Dn only						–40	µA
I_{OZH}	Off-state output current High-level voltage applied	74F711A/ 74F711-1 only	V_{CC} = MAX, V_O = 2.7V					50	µA
I_{OZL}	Off-state output current Low-level voltage applied		V_{CC} = MAX, V_O = 0.5V					–50	µA
I_{OS}	Short-circuit output current[3]	74F711-1/ 74F712-1	V_{CC} = MAX			–60		–150	mA
I_O	Output current[4]	74F711A/ 74F712A	V_{CC} = MAX, V_O = 2.25 V			–60		–150	mA
I_{CC}	Supply current (total)	74F711A	I_{CCH}	V_{CC} = MAX			25	35	mA
			I_{CCL}					33	46	mA
			I_{CCZ}					27	40	mA
		74F711-1	I_{CCH}	V_{CC} = MAX				26	40	mA
			I_{CCL}					33	45	mA
			I_{CCZ}					28	45	mA
		74F712A	I_{CCH}	V_{CC} = MAX				20	27	mA
			I_{CCL}					30	40	mA
		74F712-1	I_{CCH}	V_{CC} = MAX				20	30	mA
			I_{CCL}					29	40	mA

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. I_O is tested under conditions that produce current approximity one half of the true short-circuit output current (I_{OS}).

Multiplexers
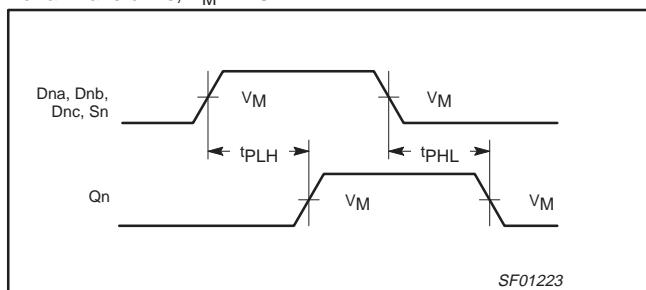
AC ELECTRICAL CHARACTERISTICS – 74F711A/74F711-1
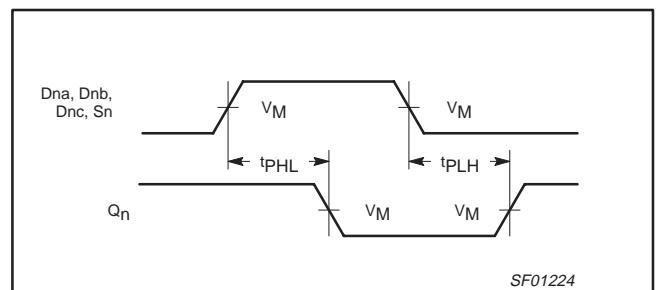
SYMBOL	PARAMETER		TEST CONDITION	LIMITS					UNIT
				$T_{amb} = +25°C$ $V_{CC} = 5V$ $C_L = 50pF, R_L = 500\Omega$			$T_{amb} = 0°C$ to $+70°C$ $V_{CC} = 5V \pm 10\%$ $C_L = 50pF,$ $R_L = 500\Omega$		
				MIN	TYP	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay Dna, Dnb to Qn	74F711A	Waveform 1, 2	2.5 2.5	5.0 4.0	7.5 7.0	2.0 2.0	8.0 7.5	ns ns
t_{PLH} t_{PHL}	Propagation delay S to Qn		Waveform 1, 3	7.0 5.0	9.0 8.0	12.0 11.0	5.5 4.5	13.5 12.0	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{INV}$ to Qn		Waveform 1, 3	6.0 4.0	9.0 8.0	12.5 11.0	5.0 3.5	14.0 11.5	ns ns
t_{PZH} t_{PZL}	Output Enable time $\overline{OE}$ to Qn		Waveform 4 Waveform 5	2.5 2.5	4.0 4.5	6.5 7.0	2.0 2.0	7.0 7.5	ns ns
t_{PHZ} t_{PLZ}	Output Disable time $\overline{OE}$ to Qn		Waveform 4 Waveform 5	2.5 3.0	4.0 5.0	7.0 8.0	2.0 2.5	8.0 8.5	ns ns
t_{PLH} t_{PHL}	Propagation delay Dna, Dnb to Qn	74F711-1	Waveform 1, 2	3.0 2.0	4.5 4.5	7.5 7.5	2.0 2.5	9.0 8.0	ns ns
t_{PLH} t_{PHL}	Propagation delay S, $\overline{INV}$ to Qn		Waveform 1, 3	6.5 4.5	10.0 8.5	13.5 11.5	5.5 4.0	14.5 12.5	ns ns
t_{PZH} t_{PZL}	Output Enable time $\overline{OE}$ to Qn		Waveform 4 Waveform 5	2.5 3.0	4.5 5.0	7.5 7.5	2.0 2.5	9.0 8.0	ns ns
t_{PHZ} t_{PLZ}	Output Disable time $\overline{OE}$ to Qn		Waveform 4 Waveform 5	2.0 3.5	4.5 5.5	7.0 8.5	2.0 3.0	8.0 9.5	ns ns

AC ELECTRICAL CHARACTERISTICS – 74F712A/74F712-1
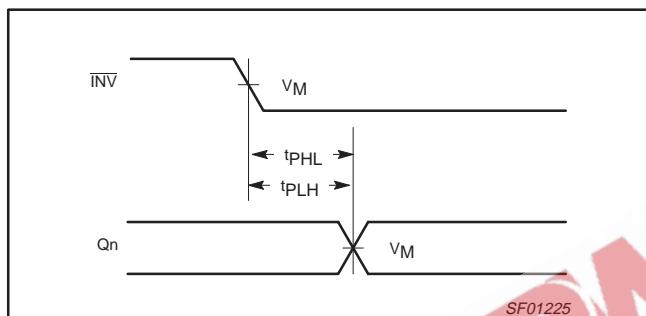
SYMBOL	PARAMETER		TEST CONDITION	LIMITS					UNIT
				$T_{amb} = +25°C$ $V_{CC} = 5V$ $C_L = 50pF, R_L = 500\Omega$			$T_{amb} = 0$ to $+70°C$ $V_{CC} = 5V \pm 10\%$ $C_L = 50pF,$ $R_L = 500\Omega$		
				MIN	TYP	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay Dna, Dnb, Dnc to Qn	74F712A	Waveform 1, 2	2.0 2.0	3.5 3.5	6.5 6.5	2.0 2.0	7.0 7.0	ns ns
t_{PLH} t_{PHL}	Propagation delay S0, S1 to Qn		Waveform 1	6.5 5.0	8.0 7.5	11.5 10.0	5.5 4.5	13.5 11.0	ns ns
t_{PLH} t_{PHL}	Propagation delay Dna, Dnb, Dnc to Qn	74F712-1	Waveform 1, 2	2.0 2.0	4.0 4.0	7.0 7.0	2.0 2.0	7.5 7.5	ns ns
t_{PLH} t_{PHL}	Propagation delay S0, S1 to Qn		Waveform 1	7.0 5.5	9.0 7.5	12.0 10.5	6.0 5.5	13.5 11.0	ns ns

AC WAVEFORMS

For all waveforms, V_M = 1.5V
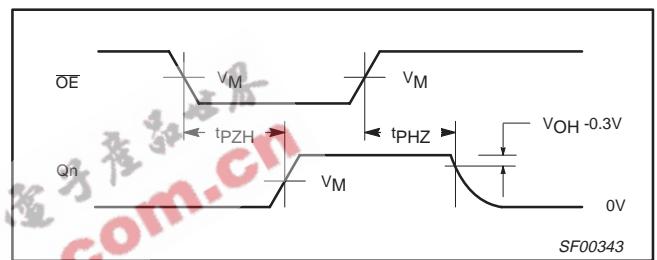
**Waveform 1. Propagation Delay for Non-Inverting Output**
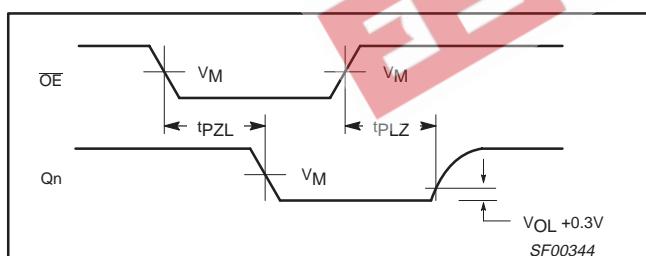
Waveform 2. Propagation Delay for Inverting Output

Waveform 3. Propagation Delay for $\overline{INV}$ to Output

**Waveform 4. 3-State Output Enable Time to High Level and
Output Disable Time from High Level**
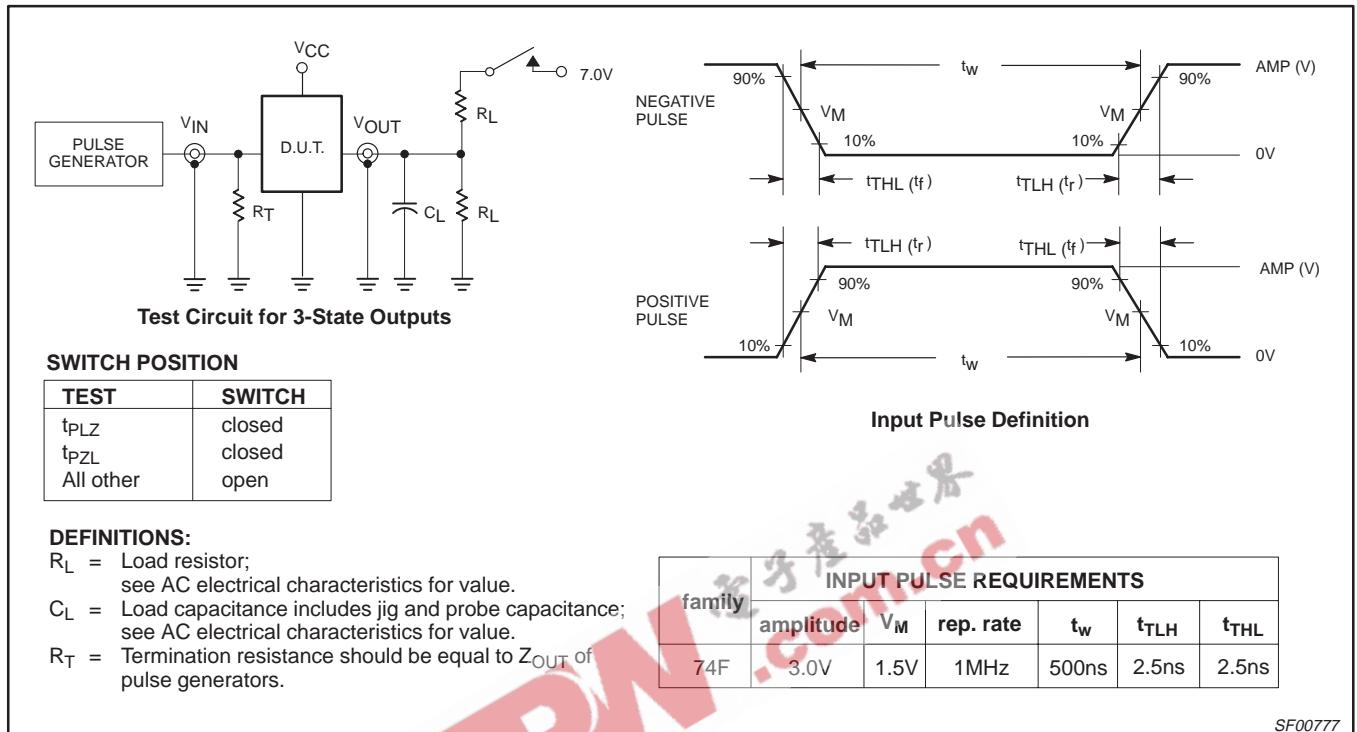
**Waveform 5. 3-State Output Enable Time to Low
Level and Output Disable Time from Low Level**

TEST CIRCUIT AND WAVEFORMS

Test Circuit for 3-State Outputs

Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS:

R_L = Load resistor;
see AC electrical characteristics for value.

C_L = Load capacitance includes jig and probe capacitance;
see AC electrical characteristics for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

| family	INPUT PULSE REQUIREMENTS					
	amplitude	V_M	rep. rate	t_w	t_{TLH}	t_{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns

SF00777

Multiplexers

74F711A/74F711-1,
74F712A/74F712-1

DIP20:   plastic dual in-line package; 20 leads (300 mil)   **SOT146-1**

DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A₁ min.	A₂ max.	b	b₁	c	D [1]	E [1]	e	e₁	L	M_E	M_H	w	Z [1] max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	0.36 0.23	26.92 26.54	6.40 6.22	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	2.0
inches	0.17	0.020	0.13	0.068 0.051	0.021 0.015	0.014 0.009	1.060 1.045	0.25 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.078

In the table header the units use subscripts: A_1, A_2, b_1, D, E, e_1, M_E, M_H, Z.

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.
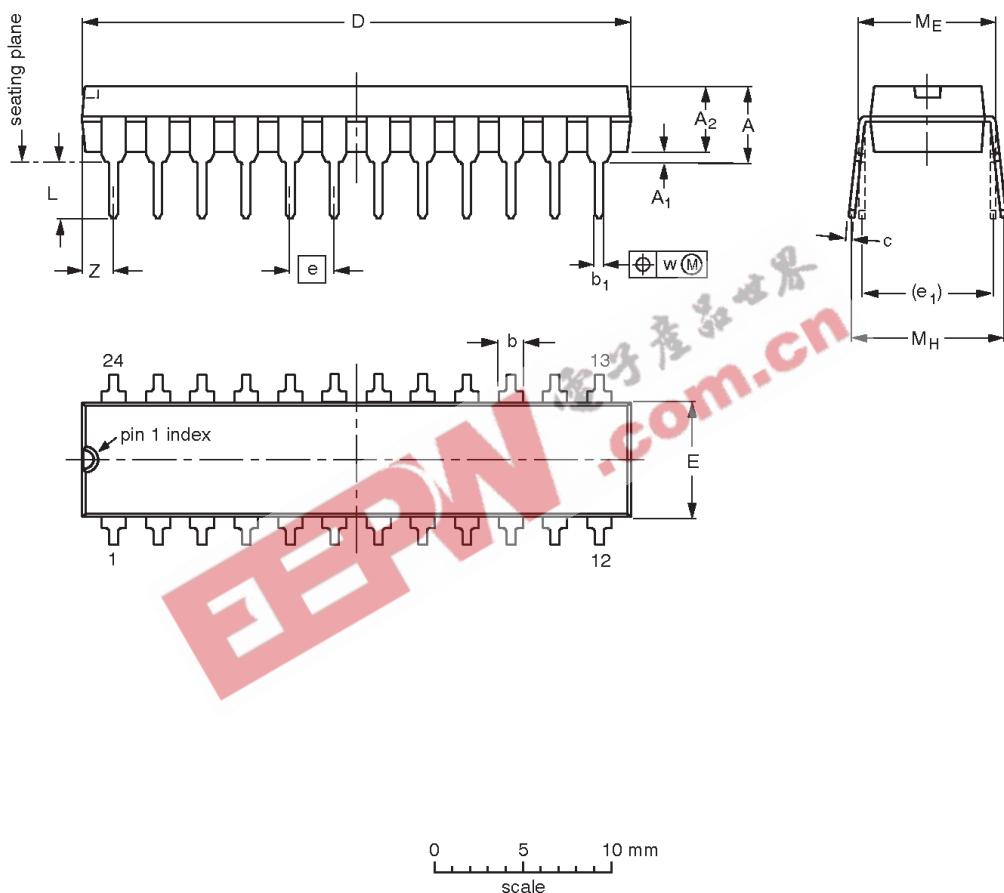
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT146-1			SC603			~~92-11-17~~ 95-05-24

Multiplexers

DIP24:   plastic dual in-line package; 24 leads (300 mil)   **SOT222-1**

DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A max.	A₁ min.	A₂ max.	b	b₁	c	D (1)	E (1)	e	e₁	L	M_E	M_H	w	Z (1) max.
mm	4.70	0.38	3.94	1.63 1.14	0.56 0.43	0.36 0.25	31.9 31.5	6.73 6.48	2.54	7.62	3.51 3.05	8.13 7.62	10.03 7.62	0.25	2.05
inches	0.185	0.015	0.155	0.064 0.045	0.022 0.017	0.014 0.010	1.256 1.240	0.265 0.255	0.100	0.300	0.138 0.120	0.32 0.30	0.395 0.300	0.01	0.081

Column headers with subscripts: A max., A_1 min., A_2 max., b, b_1, c, $D^{(1)}$, $E^{(1)}$, e, e_1, L, M_E, M_H, w, $Z^{(1)}$ max.

Note

1. Plastic or metal protrusions of 0.01 inches maximum per side are not included.
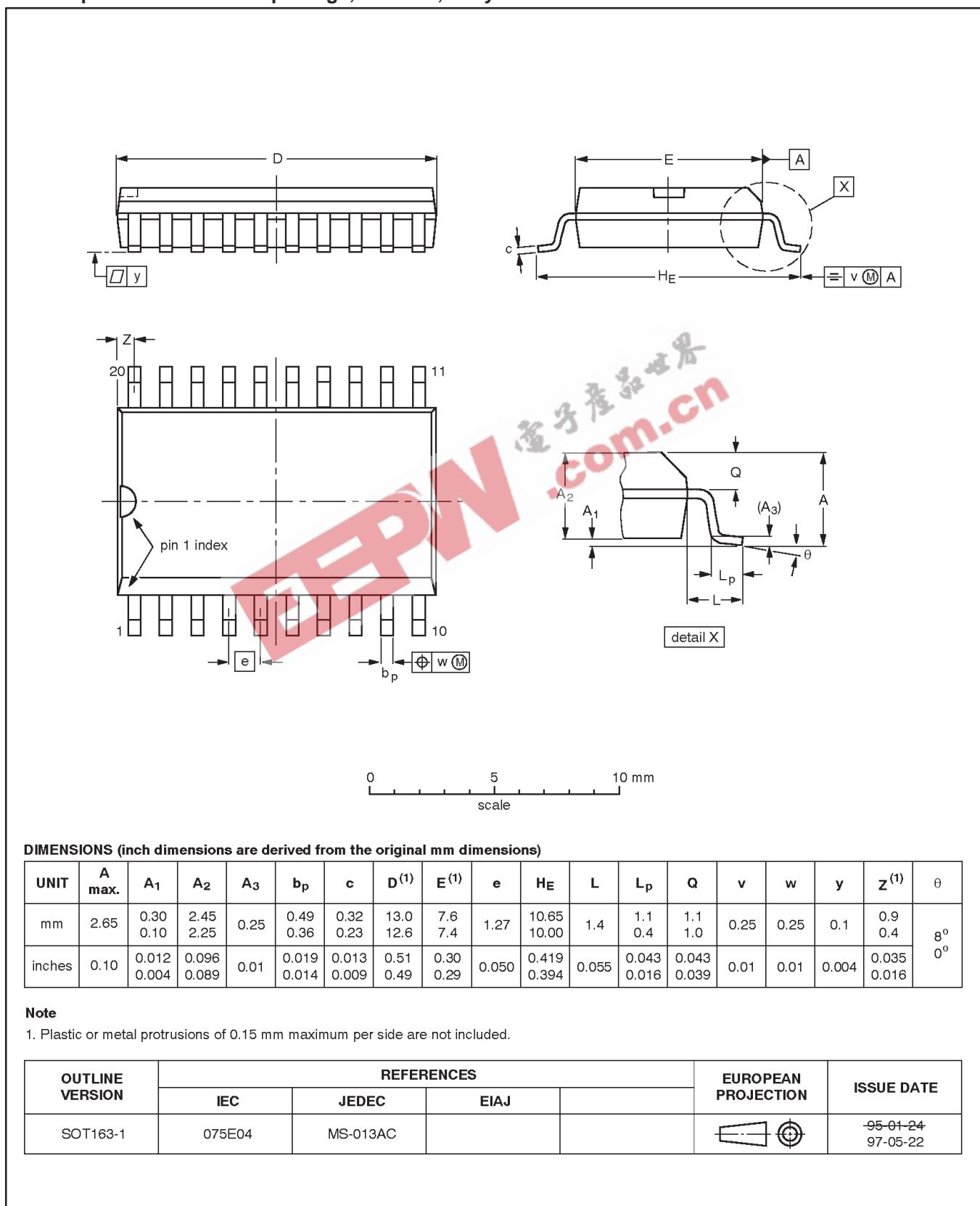
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT222-1		MS-001AF				95-03-11

Multiplexers

74F711A/74F711-1,
74F712A/74F712-1

SO20: plastic small outline package; 20 leads; body width 7.5 mm

SOT163-1

pin 1 index

detail X

scale
0   5   10 mm

DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A₁	A₂	A₃	bₚ	c	D (1)	E (1)	e	HE	L	Lₚ	Q	v	w	y	Z (1)	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	13.0 12.6	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.51 0.49	0.30 0.29	0.050	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
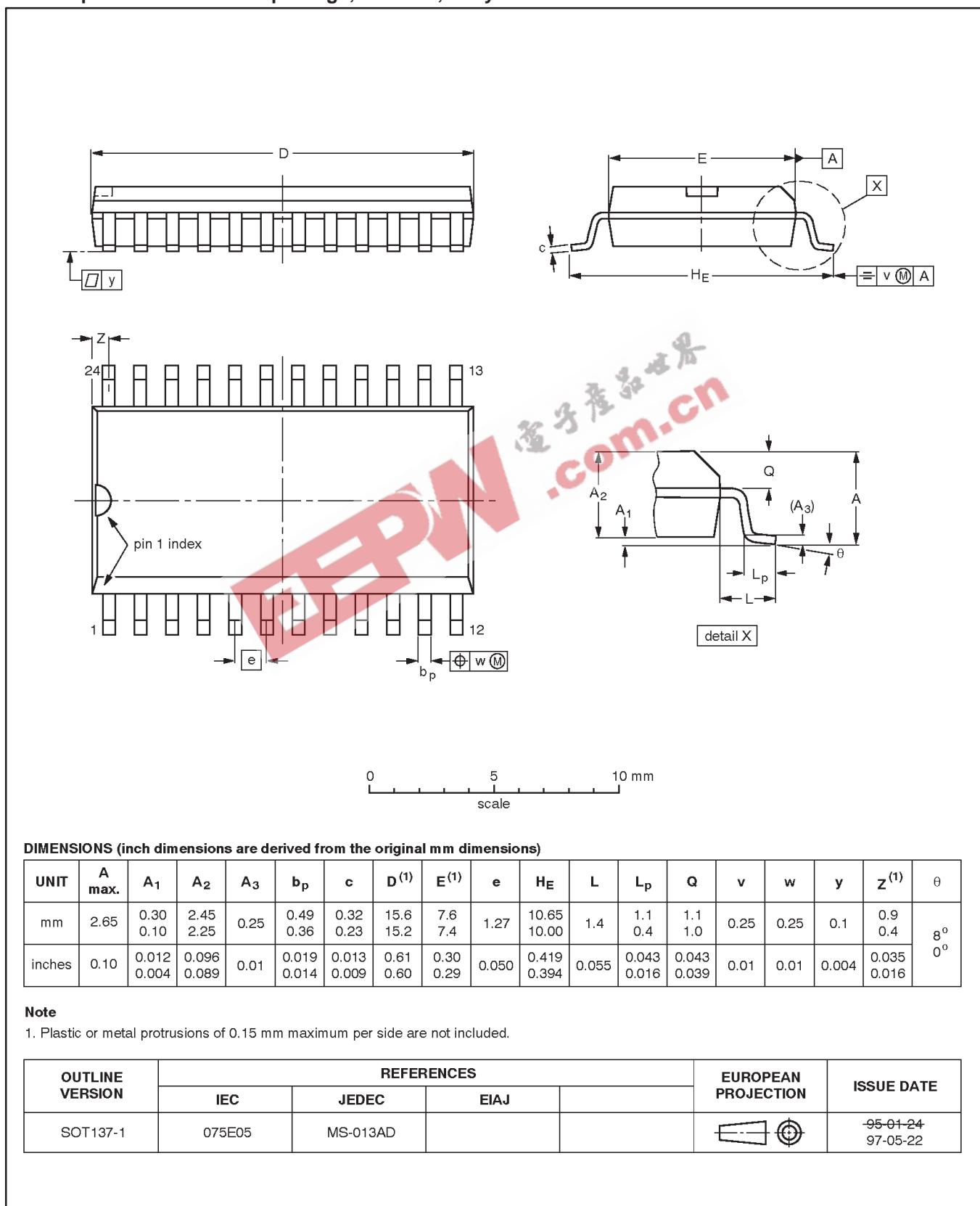
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT163-1	075E04	MS-013AC				~~95-01-24~~ 97-05-22

Multiplexers

SO24: plastic small outline package; 24 leads; body width 7.5 mm

SOT137-1

0   5   10 mm
scale

DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	15.6 15.2	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.61 0.60	0.30 0.29	0.050	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT137-1	075E05	MS-013AD				~~95-01-24~~ 97-05-22

NOTES

Data sheet status

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make chages at any time without notice in order to improve design and supply the best possible product.
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[1]   Please consult the most recently issued datasheet before initiating or completing a design.

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