

74ACT1284 IEEE 1284 Transceiver

General Description

The 74ACT1284 contains four non-inverting bidirectional buffers and three non-inverting buffers with open Drain outputs and high drive capability on the B Ports. It is intended to provide a standard signaling method for a bi-direction parallel peripheral in an Extended Capabilities Port mode (ECP).

The HD (active HIGH) input pin enables the B Ports to switch from open Drain to a high drive totem pole output, capable of sourcing 14 mA on all seven buffers. The DIR input determines the direction of data flow on the bidirectional buffers. DIR (active HIGH) enables data flow from A Ports to B Ports. DIR (active LOW) enables data flow from B Ports to A Ports.

Features

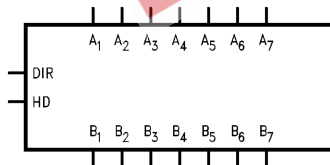
- TTL-compatible inputs
- A Ports have standard 4 mA totem pole outputs
- Typical input hysteresis of 0.5V
- B Port high drive source/sink capability of 14 mA
- Bidirectional non-inverting buffers
- Supports IEEE P1284 Level 1 and Level 2 signaling standards for bidirectional parallel communications between personal computers and printing peripherals
- B Port outputs in High Impedance mode during power down
- Guaranteed 4000V minimum ESD protection

Ordering Code:

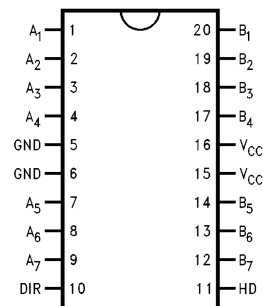
Order Number	Package Number	Package Description
74ACT1284SC	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
74ACT1284MSA	MSA20	20-Lead Shrink Small Outline Package (SSOP), EIAJ TYPE II, 5.3mm Wide
74ACT1284MTC	MTC20	20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code.

Logic Symbol



Connection Diagram



Pin Descriptions

Pin Names	Description
HD	High Drive Enable input (Active HIGH)
DIR	Direction Control Input
A ₁ - A ₄	Side A Inputs or Outputs
B ₁ - B ₄	Side B Inputs or Outputs
A ₅ - A ₇	Side A Inputs
B ₅ - B ₇	Side B Outputs

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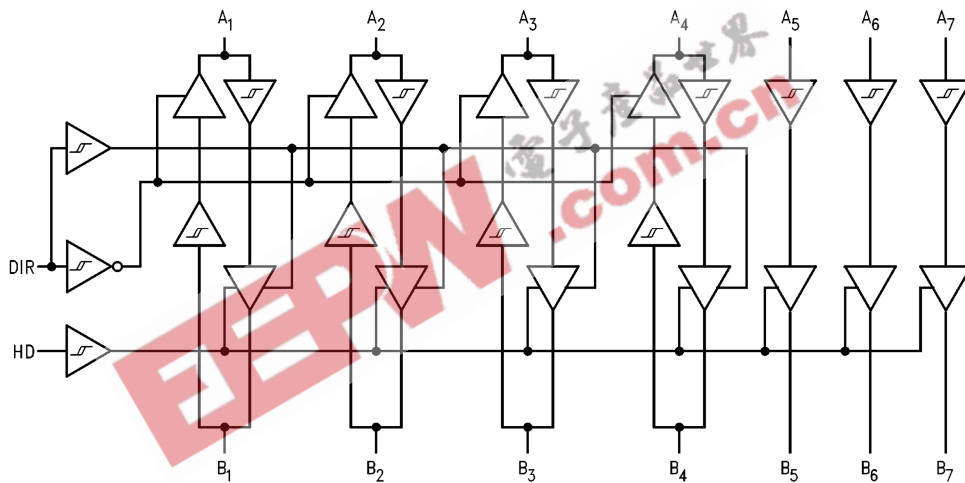
Truth Table

Inputs		Outputs
DIR	HD	
L	L	B ₁ -B ₄ Data to A ₁ -A ₄ , and A ₅ -A ₇ Data to B ₅ -B ₇ (Note 1)
L	H	B ₁ -B ₄ Data to A ₁ -A ₄ , and A ₅ -A ₇ Data to B ₅ -B ₇
H	L	A ₁ -A ₇ Data to B ₁ -B ₇ (Note 2)
H	H	A ₁ -A ₇ Data to B ₁ -B ₇

Note 1: B₅ - B₇ Open Drain Outputs

Note 2: B₁ - B₇ Open Drain Outputs

Logic Diagram



Absolute Maximum Ratings (Note 3)		Recommended Operating Conditions					
(Note 4)							
Supply Voltage (V_{CC})	-0.5V to +7.0V	Supply Voltage (V_{CC})	4.7V to 5.5V				
DC Input Diode Current (I_{IK})		Input Voltage (V_I)	0V to V_{CC}				
$V_I = -0.5V$	-20 mA	Output Voltage (V_O)	0V to V_{CC}				
$V_I = V_{CC} + 0.5V$	+20 mA	Operating Temperature (T_A)	-40°C to +85°C				
DC Input Voltage (V_I) A Side	-0.5V to $V_{CC} + 0.5V$						
DC Input Voltage (V_I) B Side	-2V to +7V						
DC Output Diode Current (I_{OK})							
$V_O = -0.5V$	-20 mA						
$V_O = V_{CC} + 0.5V$	+20 mA						
DC Output Voltage (V_O) A Side	-0.5V to $V_{CC} + 0.5V$						
DC Output Voltage (V_O) B Side	-2V to +7V						
DC Output Source							
or Sink Current (I_O)	± 50 mA						
DC V_{CC} or Ground Current							
per Output Pin (I_{CC} or I_{GND})	± 50 mA						
Storage Temperature (T_{STG})	-65°C to +150°C						
Note 3: Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. Fairchild does not recommend operation of FACT™ circuits outside databook specifications.							
Note 4: Either voltage limit or current limit is sufficient to protect inputs.							
DC Electrical Characteristics							
Symbol	Parameter	V_{CC} (V)	Guaranteed Limits			Units	Conditions
			$T_A = +25^\circ\text{C}$	$T_A = 0^\circ\text{C to } +70^\circ\text{C}$	$T_A = -40^\circ\text{C to } +85^\circ\text{C}$		
V_{IH}	Minimum HIGH Level	4.7	2.0	2.0	2.0	V	Recognized High Signal
	Input Voltage	5.5	2.0	2.0	2.0		
V_{IL}	Maximum LOW Level	4.7	0.8	0.8	0.8	V	Recognized Low Signal
	Input Voltage	5.5	0.8	0.8	0.8		
V_{OH}	Minimum HIGH Level	4.7	4.5	4.5	4.5	V	$I_{OUT} = -50 \mu\text{A}$ (A_n) $V_{IN} = V_{IL}$ or V_{IH} (Note 5) $I_{OH} = -4 \text{ mA}$ (A_n) $I_{OH} = -14 \text{ mA}$ (B_n)
	Output Voltage		3.7	3.7	3.7		
			2.4	2.4	2.4		
V_{OL}	Maximum LOW Level	4.7	0.2	0.2	0.2	V	$I_{OUT} = 50 \mu\text{A}$ (A_n) $V_{IN} = V_{IL}$ or V_{IH} (Note 5) $I_{OH} = 4 \text{ mA}$ (A_n) $I_{OH} = 14 \text{ mA}$ (B_n)
	Output Voltage		0.4	0.4	0.4		
I_{IN}	Maximum Input Leakage Current	5.5		±0.1	±1.0	μA	$V_I = V_{CC}$, GND (DIR, A5, A6, A7, HD)
I_{CCT}	Maximum I_{CC} /Input	5.5		1.5	1.5	mA	$V_I = V_{CC} - 2.1V$
I_{CC}	Maximum Quiescent Supply Current	5.5	400	400	500	μA	$V_{IN} = V_{CC}$ or GND
I_{OZ}	Maximum Output Leakage Current	5.5	±20	±20	±20	μA	$V_O = V_{CC}$, GND
I_{OFF}	Maximum B-Side Power Down Leakage Current	0.0	100	100	100	μA	$V_{OUT} = 5.25V$
ΔV_T	Input Hysteresis	5.0	0.4	0.4	0.35	V	$V_T + - V_T -$
R_D	Maximum Output Impedance	5.0	22	22	24	Ω	B_n (Note 6)
	Minimum Output Impedance	5.0	8	8	6	Ω	B_n (Note 6)
Note 5: All outputs loaded; thresholds on input associated with output under test.							
Note 6: This parameter is guaranteed but not tested, characterized only: RD is the measure of the B-Side output impedance with the output in the HIGH state.							

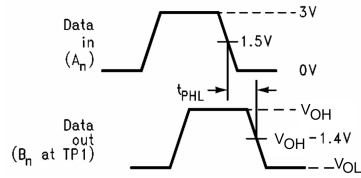
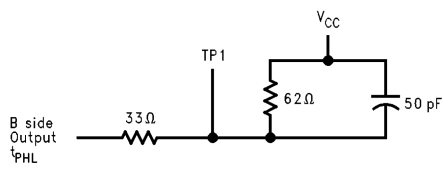
AC Electrical Characteristics									
Symbol	Parameter	T _A = +25°C V _{CC} = 4.7V – 5.5V		T _A = 0°C to +70°C V _{CC} = 4.7V – 5.5V		T _A = –40°C to +85°C V _{CC} = 4.7V – 5.5V		Units	Figure Number
		Min	Max	Min	Max	Min	Max		
t _{PHL}	A ₁ - A ₇ to B ₁ - B ₇	2.0	20.0	2.0	20.0	2.0	24.0	ns	Figure 1
t _{PLH}	A ₁ - A ₇ to B ₁ - B ₇	2.0	20.0	2.0	20.0	2.0	24.0	ns	Figure 2
t _{PHL}	B ₁ - B ₄ to A ₁ - A ₄	2.0	20.0	2.0	20.0	2.0	24.0	ns	Figure 3
t _{PLH}	B ₁ - B ₄ to A ₁ - A ₄	2.0	20.0	2.0	20.0	2.0	24.0	ns	Figure 3
t _{pEnable}	Output Enable Time HD to B ₁ - B ₇	2.0	20.0	2.0	20.0	2.0	24.0	ns	Figure 2
t _{pDisable}	Output Disable Time HD to B ₁ - B ₇	2.0	20.0	2.0	20.0	2.0	24.0	ns	Figure 2
t _{SKEW}	Output Slew Rate								
t _{PLH}	B ₁ - B ₇	0.05	0.40	0.05	0.40	0.05	0.40	V/ns	Figures 1, 2
t _{PHL}									
t _r , t _f	t _{RISE} and t _{FALL} B ₁ - B ₇ (Note 7)		120		120		120	ns	Figure 4 (Note 8)

Note 7: Open Drain
Note 8: This parameter is guaranteed but not tested, characterized only.
Note: Pulse Generator for all pulses; Rate ≤ 1.0 MHz; A_O ≤ 50Ω; t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.

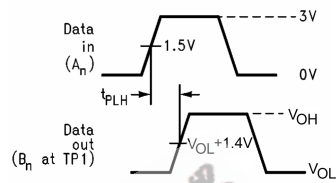
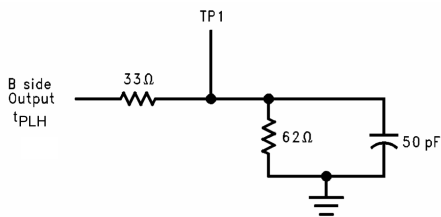
Capacitance

Symbol	Parameter	Typ	Units	Conditions
C _{IN}	Input Capacitance	4.0	pF	V _{CC} = OPEN (HD, DIR A ₅ - A ₇)
C _{I/O}	I/O Pin Capacitance	12.0	pF	V _{CC} = 5.0V

AC Loading and Waveforms



t_{SLEW} measures between 10% to 90% on the t_{PHL} Transition



t_{SLEW} measures between 10% to 90% on the t_{PLH} Transition

FIGURE 1. Port A to B Propagation Delay Waveforms

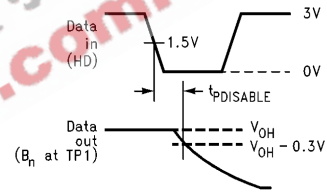
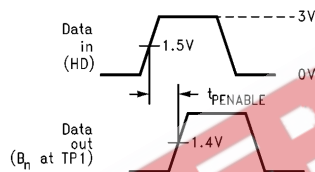


FIGURE 2. B Output Test Load and Waveforms

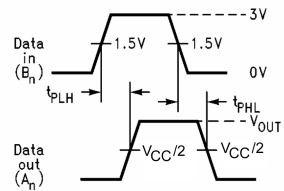
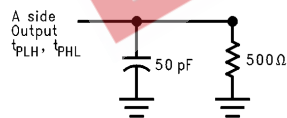


FIGURE 3. B to A Direction Test Load and Waveforms for Outputs A₁ - A₄

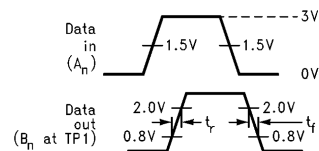
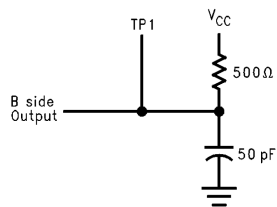
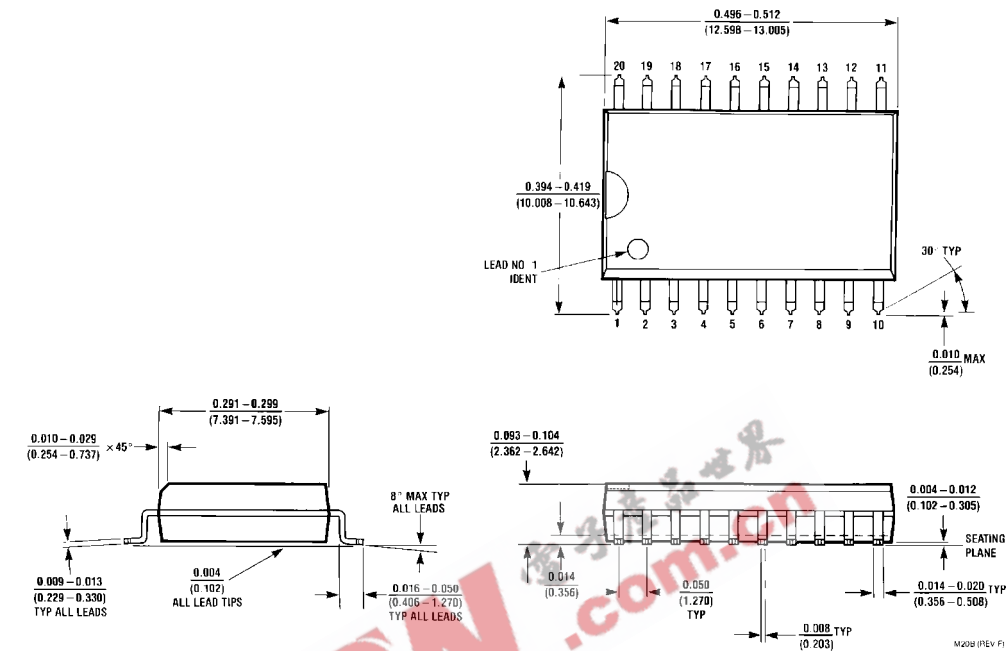
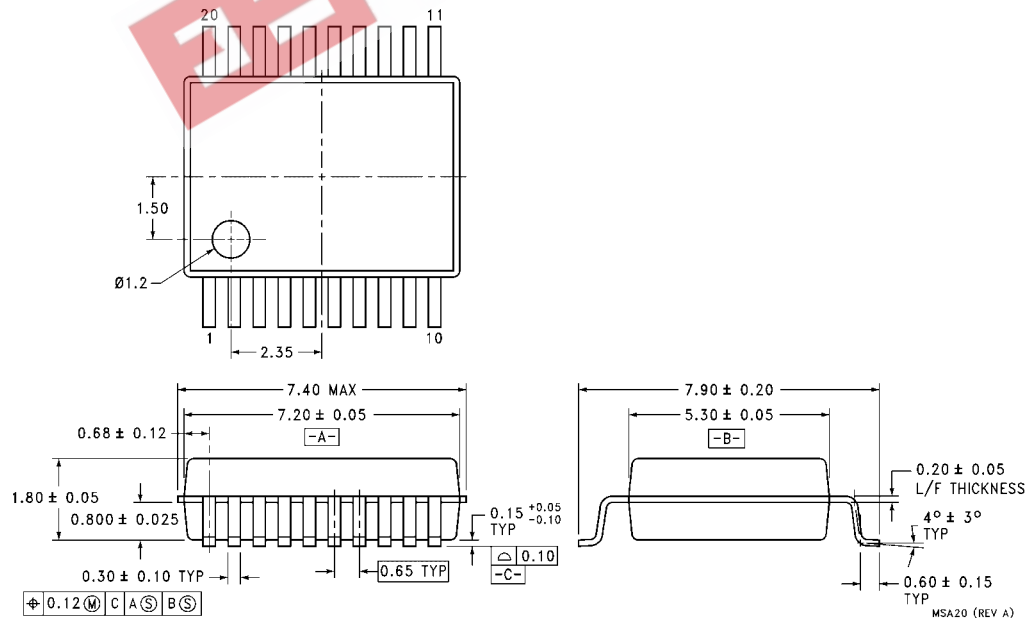


FIGURE 4. A to B Direction Test Load and Waveforms for Open Drain B₁ - B₇

Physical Dimensions inches (millimeters) unless otherwise noted

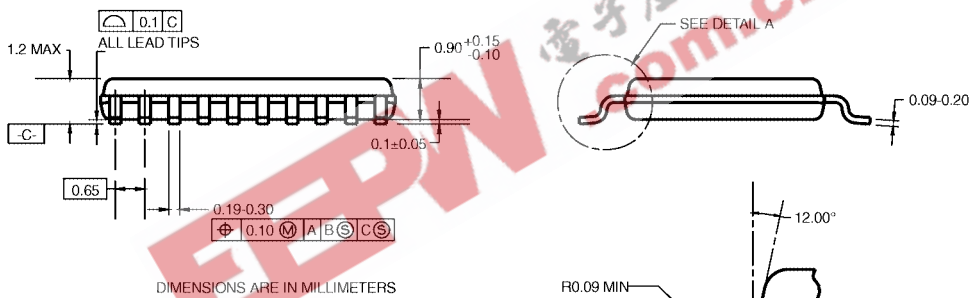
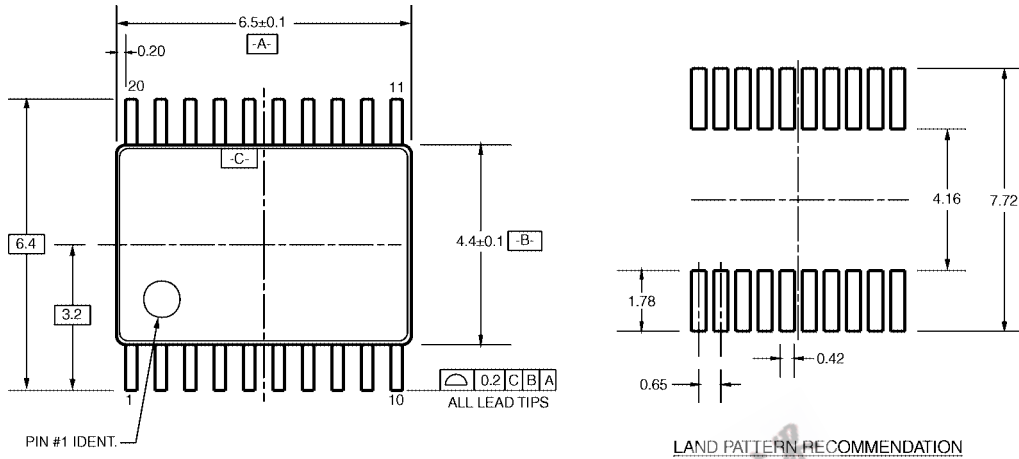


20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide Package Number M20B



20-Lead Shrink Small Outline Package (SSOP), EIAJ TYPE II, 5.3mm Wide Package Number MSA20

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



DIMENSIONS ARE IN MILLIMETERS

NOTES:

- A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AC, REF NOTE 6, DATE 7/93.
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.
- D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.

MTC20RevD1

**20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
Package Number MTC20**

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