



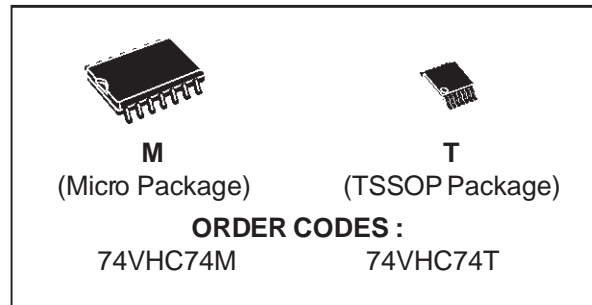
DUAL D-TYPE FLIP FLOP WITH PRESET AND CLEAR

- HIGH SPEED:
 $f_{MAX} = 170 \text{ MHz (TYP.) at } V_{CC} = 5\text{V}$
- LOW POWER DISSIPATION:
 $I_{CC} = 2 \mu\text{A (MAX.) at } T_A = 25 \text{ }^\circ\text{C}$
- HIGH NOISE IMMUNITY:
 $V_{NIH} = V_{NIL} = 28\% V_{CC} \text{ (MIN.)}$
- POWER DOWN PROTECTION ON INPUTS
- SYMMETRICAL OUTPUT IMPEDANCE:
 $|I_{OH}| = I_{OL} = 8 \text{ mA (MIN)}$
- BALANCED PROPAGATION DELAYS:
 $t_{PLH} \cong t_{PHL}$
- OPERATING VOLTAGE RANGE:
 $V_{CC} \text{ (OPR)} = 2\text{V to } 5.5\text{V}$
- PIN AND FUNCTION COMPATIBLE WITH 74 SERIES 74
- IMPROVED LATCH-UP IMMUNITY

DESCRIPTION

The 74VHC74 is an advanced high-speed CMOS DUAL D-TYPE FLIP FLOP WITH PRESET AND CLEAR fabricated with sub-micron silicon gate and double-layer metal wiring C²MOS technology.

A signal on the D INPUT is transferred to the Q OUTPUT during the positive going transition of the clock pulse.



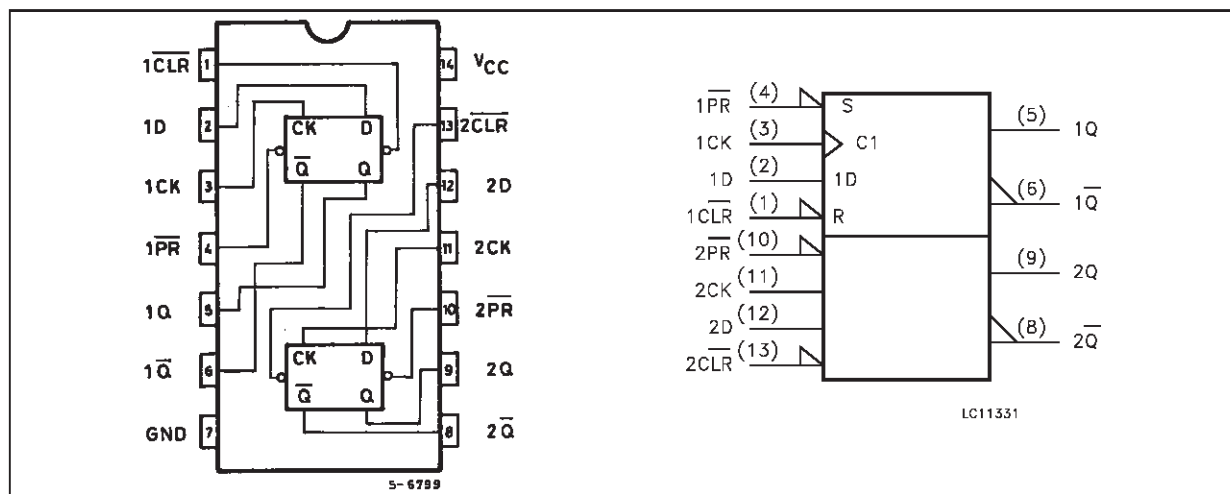
CLEAR and PRESET are independent of the clock and accomplished by a low setting on the appropriate input.

It is ideal for low power applications maintaining high speed operation similar to equivalent Bipolar Schottky TTL.

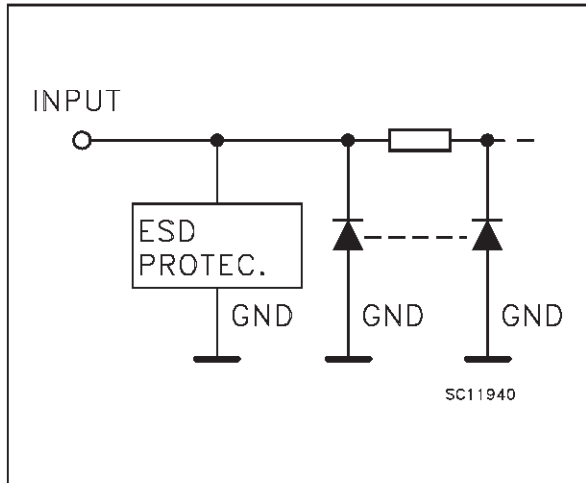
Power down protection is provided on all inputs and 0 to 7V can be accepted on inputs with no regard to the supply voltage. This device can be used to interface 5V to 3V.

All inputs and outputs are equipped with protection circuits against static discharge, giving them 2KV ESD immunity and transient excess voltage.

PIN CONNECTION AND IEC LOGIC SYMBOLS



INPUT EQUIVALENT CIRCUIT



PIN DESCRIPTION

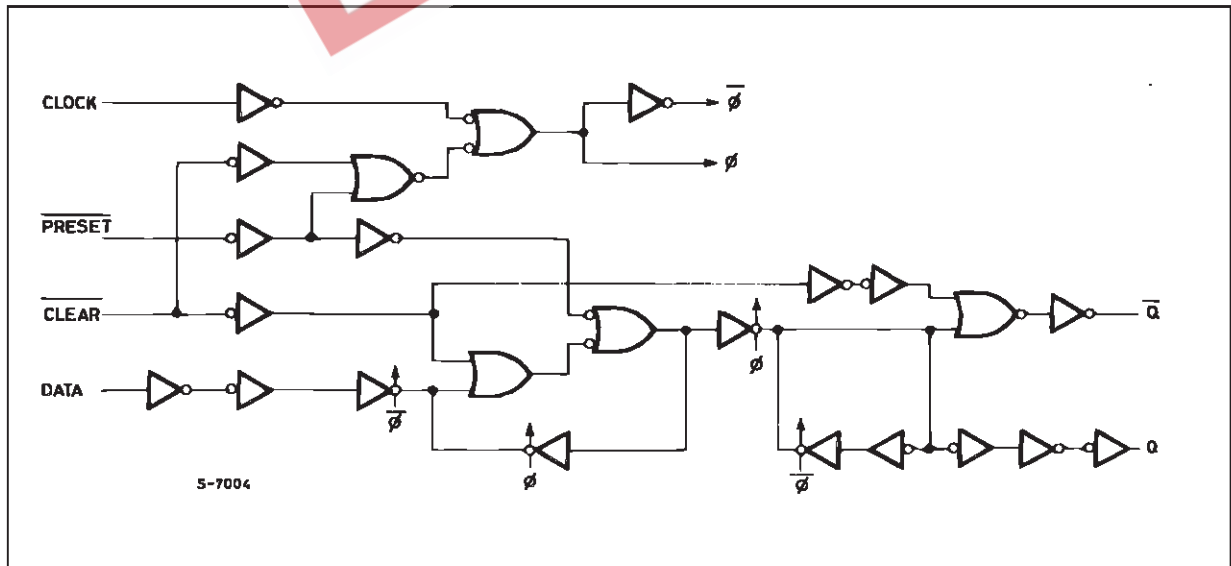
PIN No	SYMBOL	NAME AND FUNCTION
1, 13	1 $\overline{\text{CLR}}$, 2 $\overline{\text{CLR}}$	Asynchronous Reset - Direct Input
2, 12	1D, 2D	Data Input
3, 11	1CK, 2CK	Clock Input (LOW-to-HIGH, Edge-Triggered)
4, 10	1 $\overline{\text{PR}}$, 2 $\overline{\text{PR}}$	Asynchronous Set - Direct Input
5, 9	1Q, 2Q	True Flip-Flop Outputs
6, 8	1 $\overline{\text{Q}}$, 2 $\overline{\text{Q}}$	Complement Flip-Flop Outputs
7	GND	Ground (0V)
14	V _{CC}	Positive Supply Voltage

TRUTH TABLE

INPUTS				OUTPUTS		FUNCTION
$\overline{\text{CLR}}$	$\overline{\text{PR}}$	D	CK	Q	$\overline{\text{Q}}$	
L	H	X	X	L	H	CLEAR
H	L	X	X	H	L	PRESET
L	L	X	X	H	H	
H	H	L	\uparrow	L	H	
H	H	H	\uparrow	H	L	
H	H	X	\uparrow	Q _n	$\overline{\text{Q}}_n$	NO CHANGE

X: Don't Care

LOGIC DIAGRAMS



This logic diagram has not been used to estimate propagation delays

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V _{CC}	Supply Voltage	-0.5 to +7.0	V
V _I	DC Input Voltage	-0.5 to +7.0	V
V _O	DC Output Voltage	-0.5 to V _{CC} + 0.5	V
I _{IK}	DC Input Diode Current	- 20	mA
I _{OK}	DC Output Diode Current	± 20	mA
I _O	DC Output Current	± 25	mA
I _{CC} or I _{GND}	DC V _{CC} or Ground Current	± 50	mA
T _{stg}	Storage Temperature	-65 to +150	°C
T _L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V _{CC}	Supply Voltage	2.0 to 5.5	V
V _I	Input Voltage	0 to 5.5	V
V _O	Output Voltage	0 to V _{CC}	V
T _{op}	Operating Temperature	-40 to +85	°C
dt/dv	Input Rise and Fall Time (see note 1) (V _{CC} = 3.3 ± 0.3V) (V _{CC} = 5.0 ± 0.5V)	0 to 100 0 to 20	ns/V ns/V

1) V_{IN} from 30% to 70% of V_{CC}

DC SPECIFICATIONS

Symbol	Parameter	Test Conditions		Value					Unit
				T _A = 25 °C			-40 to 85 °C		
				Min.	Typ.	Max.	Min.	Max.	
V _{IH}	High Level Input Voltage	2.0		1.5			1.5		V
		3.0 to 5.5		0.7V _{CC}			0.7V _{CC}		
V _{IL}	Low Level Input Voltage	2.0				0.5		0.5	V
		3.0 to 5.5				0.3V _{CC}		0.3V _{CC}	
V _{OH}	High Level Output Voltage	2.0	I _O =-50 μA	1.9	2.0		1.9		V
		3.0	I _O =-50 μA	2.9	3.0		2.9		
		4.5	I _O =-50 μA	4.4	4.5		4.4		
		3.0	I _O =-4 mA	2.58			2.48		
		4.5	I _O =-8 mA	3.94			3.8		
V _{OL}	Low Level Output Voltage	2.0	I _O =50 μA		0.0	0.1		0.1	V
		3.0	I _O =50 μA		0.0	0.1		0.1	
		4.5	I _O =50 μA		0.0	0.1		0.1	
		3.0	I _O =4 mA			0.36		0.44	
		4.5	I _O =8 mA			0.36		0.44	
I _I	Input Leakage Current	0 to 5.5	V _I = 5.5V or GND			±0.1		±1.0	μA
I _{CC}	Quiescent Supply Current	5.5	V _I = V _{CC} or GND			2		20	μA

AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 3$ ns)

Symbol	Parameter	Test Condition			Value					Unit
		V _{CC} (V)	C _L (pF)		T _A = 25 °C			-40 to 85 °C		
					Min.	Typ.	Max.	Min.	Max.	
t _{PLH} t _{PHL}	Propagation Delay Time CK to Q or \bar{Q}	3.3 ^(*)	15			6.7	11.9	1.0	14.0	ns
		3.3 ^(*)	50			9.2	15.4	1.0	17.5	
		5.0 ^(**)	15			4.6	7.3	1.0	8.5	
		5.0 ^(**)	50			6.1	9.3	1.0	10.5	
t _{PLH} t _{PHL}	Propagation Delay Time \overline{PR} or \overline{CLR} to Q or \bar{Q}	3.3 ^(*)	15			7.6	12.3	1.0	14.5	ns
		3.3 ^(*)	50			10.1	15.8	1.0	18.0	
		5.0 ^(**)	15			4.8	7.7	1.0	9.0	
		5.0 ^(**)	50			6.3	9.7	1.0	11.0	
t _w	CK Pulse Width HIGH or LOW	3.3 ^(*)					6.0		7.0	ns
		5.0 ^(**)					5.0		5.0	
t _w	PR or CLR Pulse Width LOW	3.3 ^(*)					6.0		7.0	ns
		5.0 ^(**)					5.0		5.0	
t _s	Setup Time D to CK HIGH or LOW	3.3 ^(*)					6.0		7.0	ns
		5.0 ^(**)					5.0		5.0	
t _h	Hold Time D to CK HIGH or LOW	3.3 ^(*)					0.5		0.5	ns
		5.0 ^(**)					0.5		0.5	
t _{REM}	Removal Time \overline{CLR} or \overline{PR} to CK	3.3 ^(*)					5.0		5.0	ns
		5.0 ^(**)					3.0		3.0	
f _{MAX}	Maximum Clock Frequency	3.3 ^(*)	15		80	125		70		MHz
		3.3 ^(*)	50		50	75		45		
		5.0 ^(**)	15		130	170		110		
		5.0 ^(**)	50		90	115		75		

(*) Voltage range is 3.3V ± 0.3V

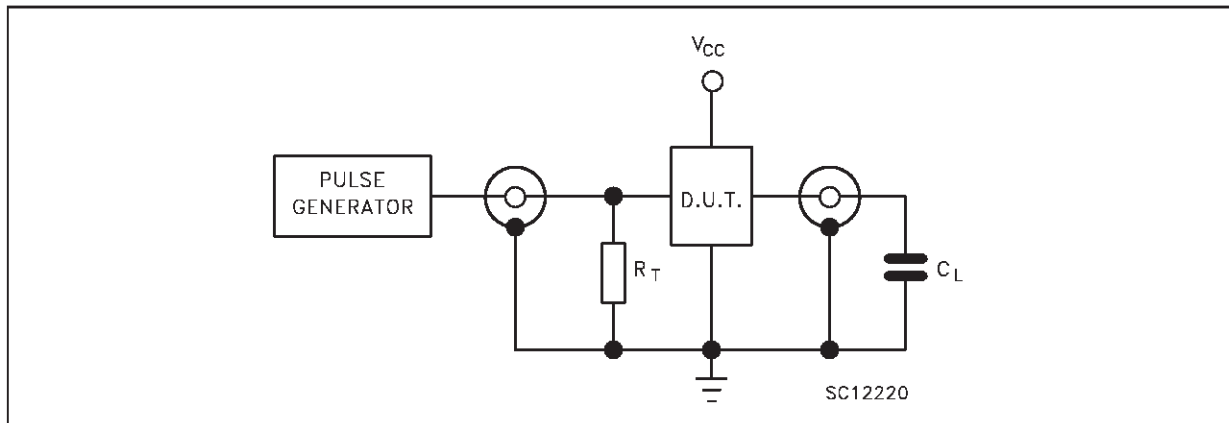
(**) Voltage range is 5V ± 0.5V

CAPACITIVE CHARACTERISTICS

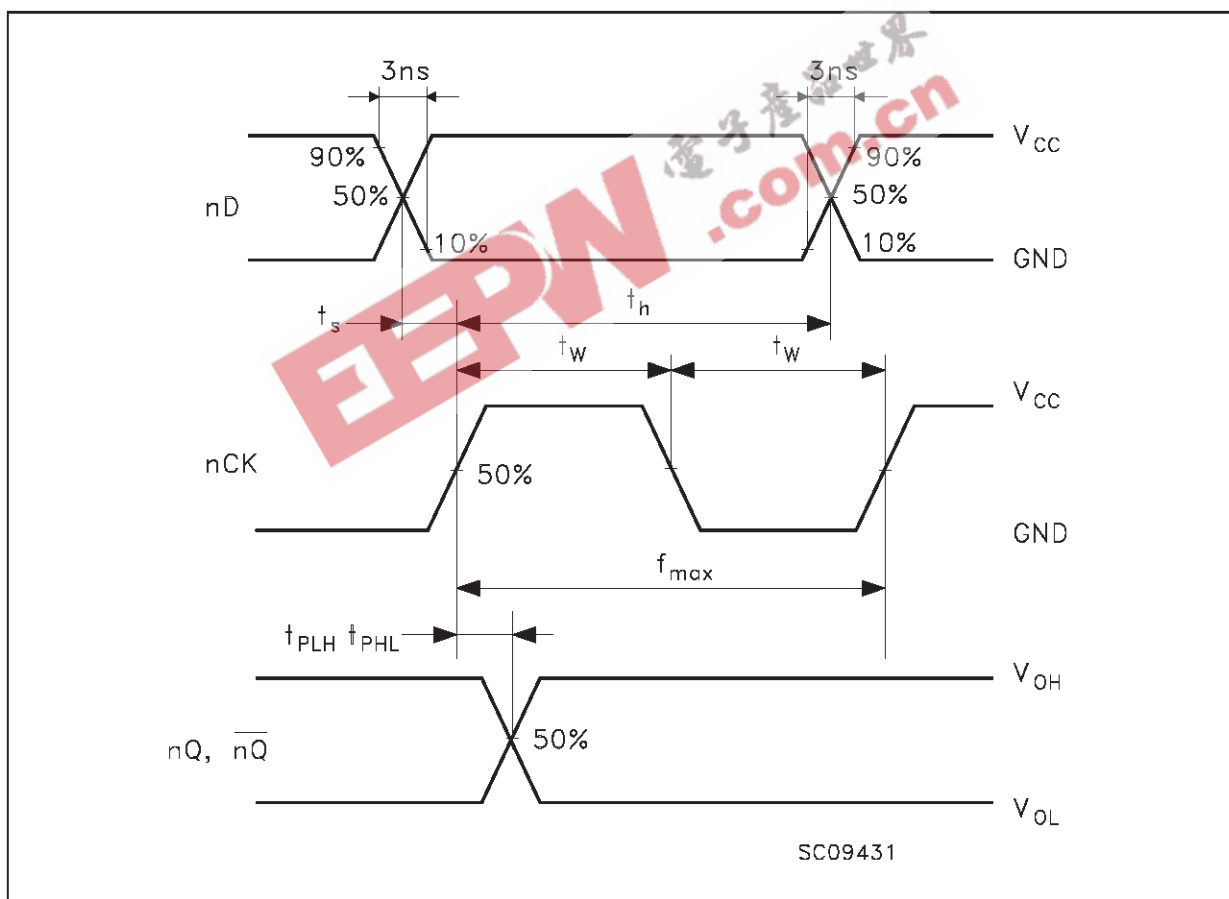
Symbol	Parameter	Test Conditions		Value					Unit
		V _{CC} (V)		T _A = 25 °C			-40 to 85 °C		
				Min.	Typ.	Max.	Min.	Max.	
C _{IN}	Input Capacitance	3.3			4	10		10	pF
C _{PD}	Power Dissipation Capacitance (note 1)	3.3	f _{IN} = 10 MHz		25				pF

1) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operating current can be obtained by the following equation. I_{CC(opr)} = C_{PD} • V_{CC} • f_{IN} + I_{CC2}/2 (per Flip-Flop)

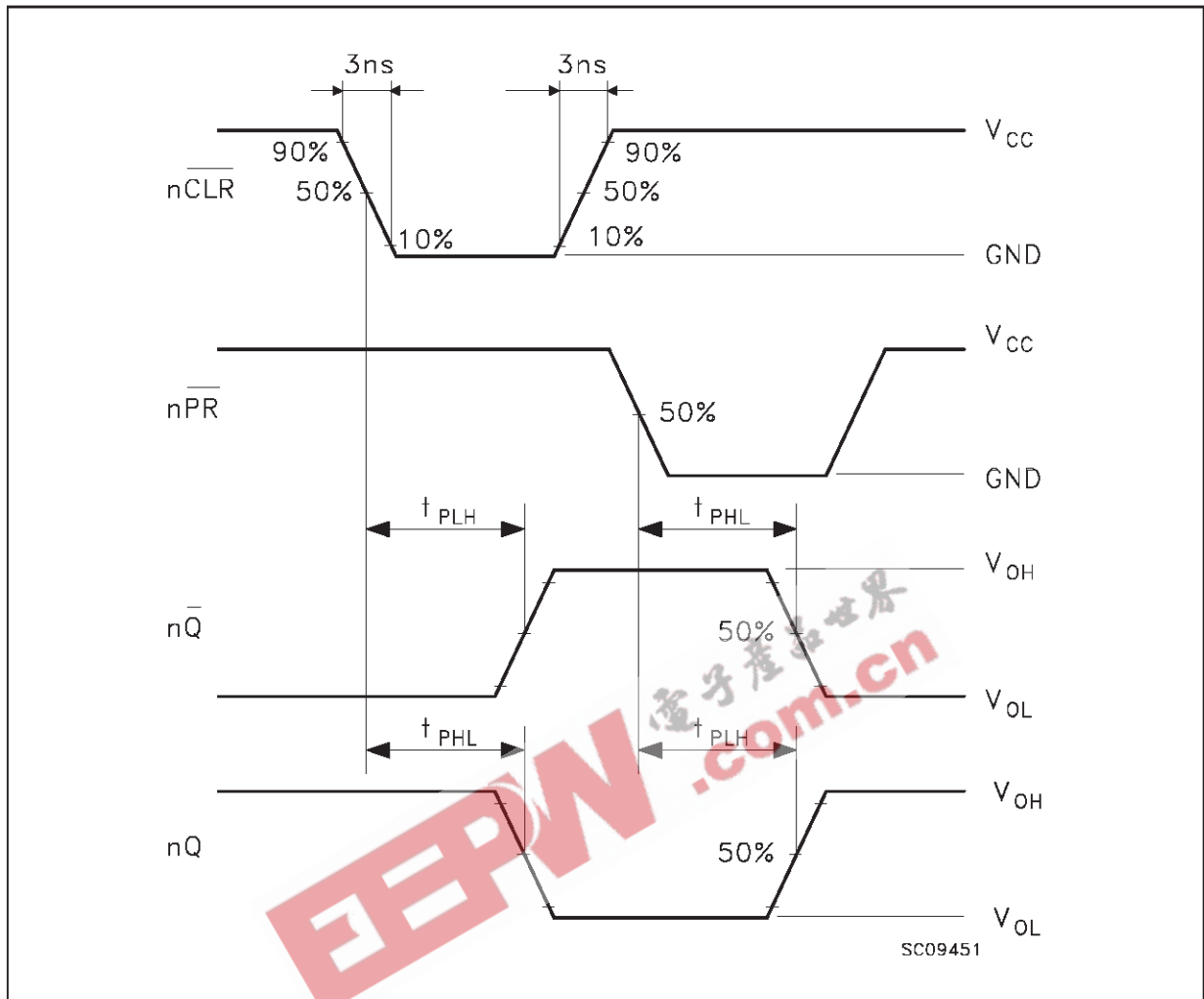
TEST CIRCUIT

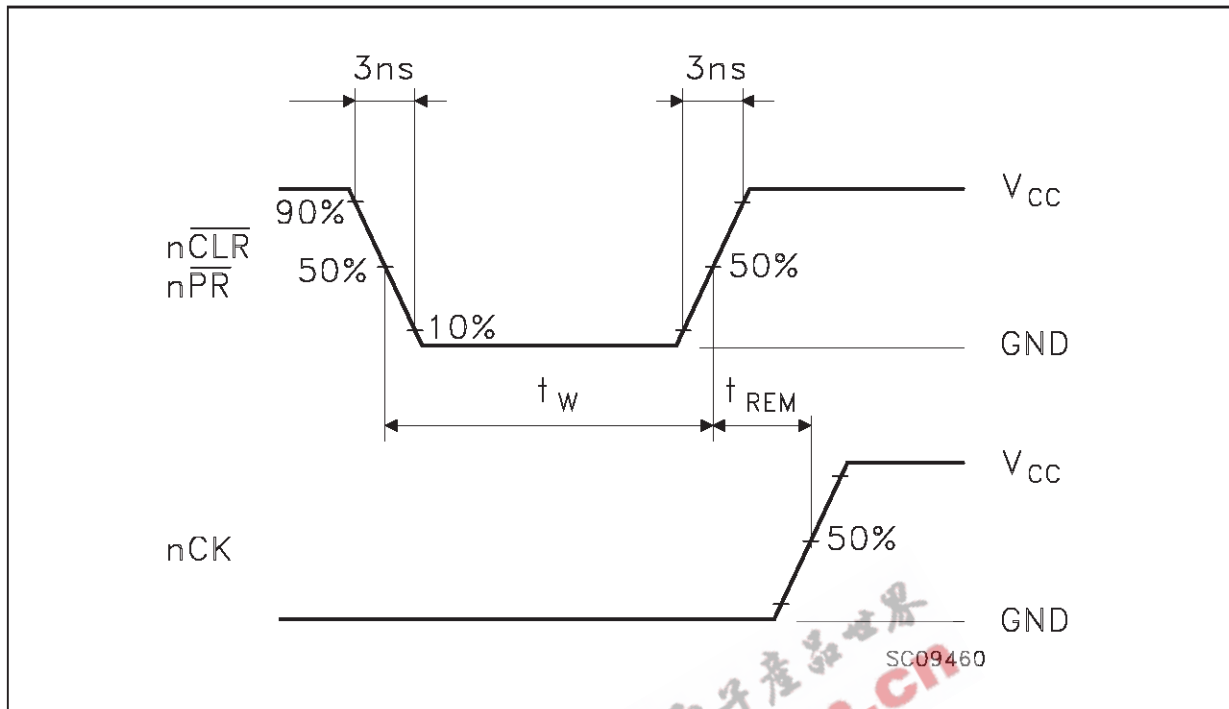
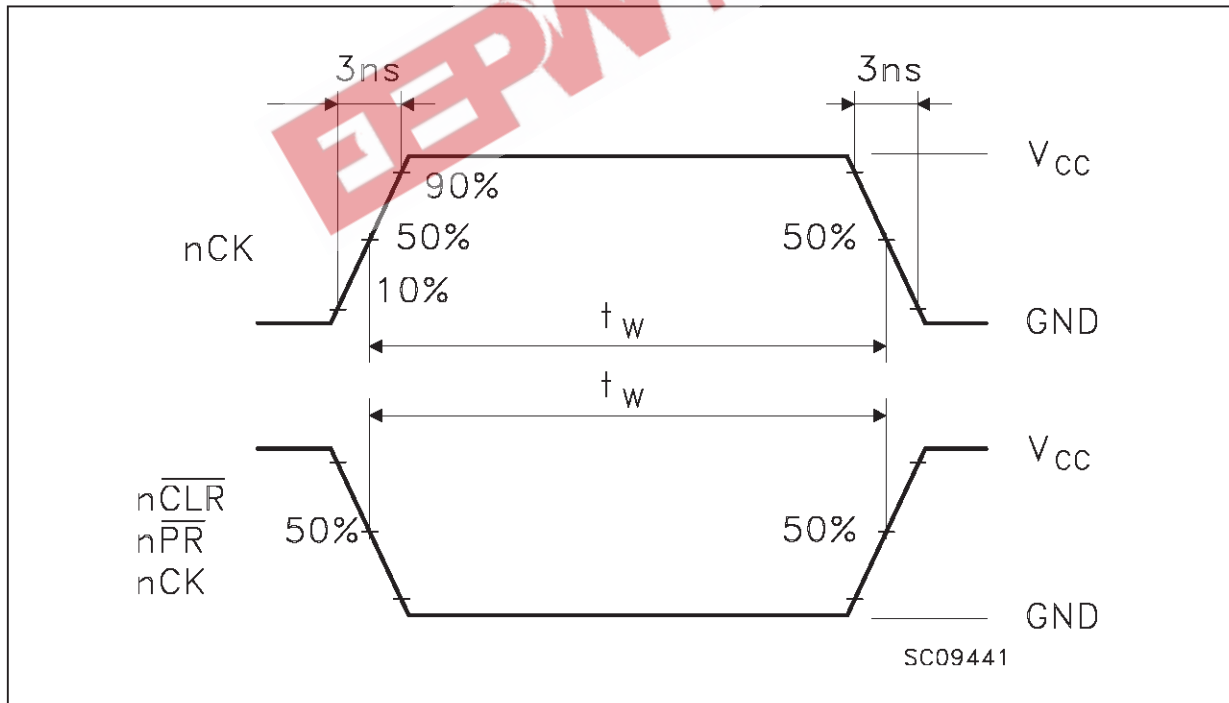


$C_L = 15/50$ pF or equivalent (includes jig and probe capacitance)
 $R_T = Z_{OUT}$ of pulse generator (typically 50Ω)

WAVEFORM 1: PROPAGATION DELAYS, SETUP AND HOLD TIMES ($f=1$ MHz; 50% duty cycle)

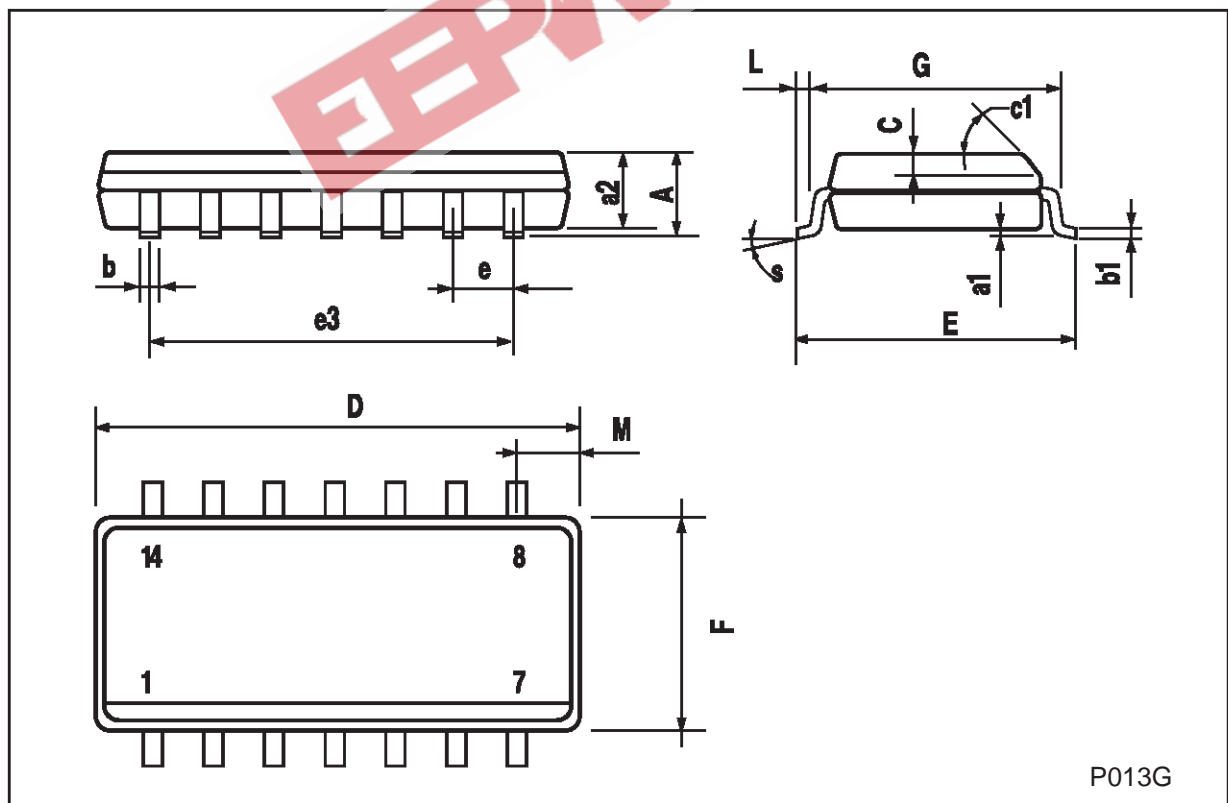
WAVEFORM 2: PROPAGATION DELAYS (f=1MHz; 50% duty cycle)



WAVEFORM 3: RECOVERY TIMES ($f=1\text{MHz}$; 50% duty cycle)

WAVEFORM 3: PULSE WIDTH


SO-14 MECHANICAL DATA

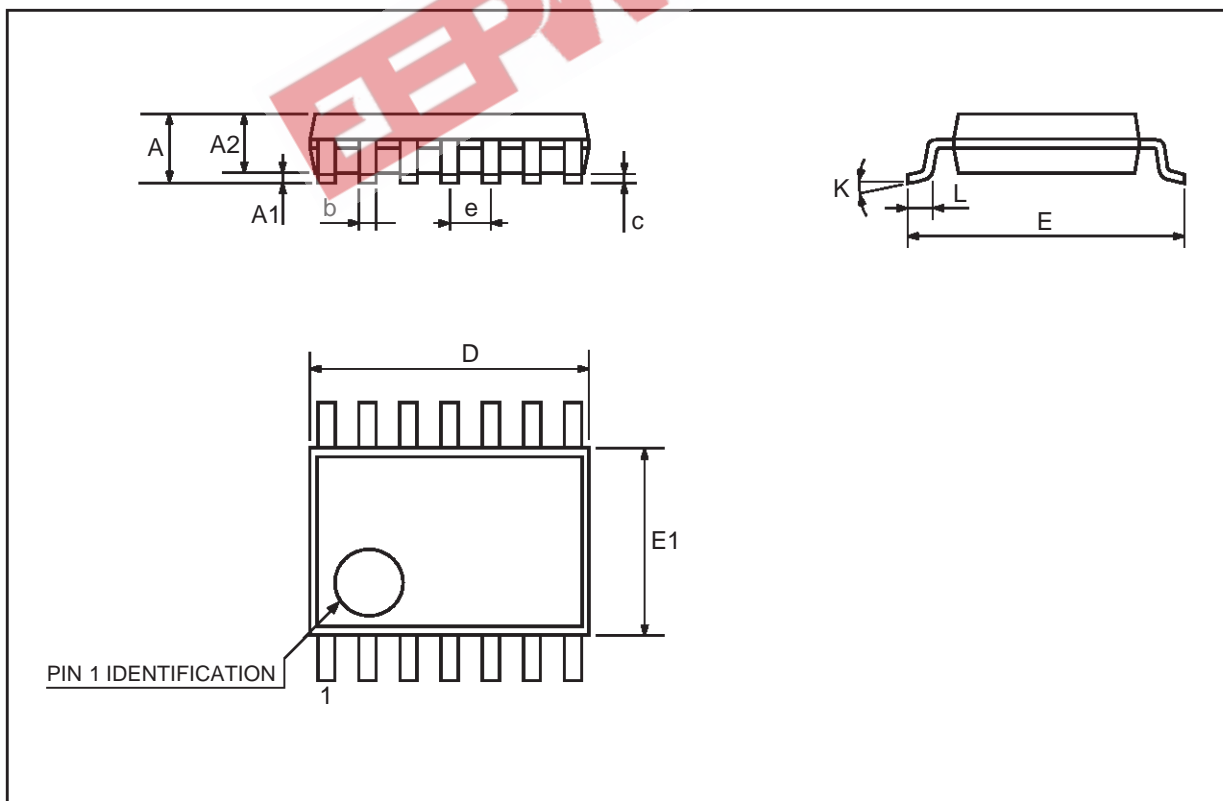
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.75			0.068
a1	0.1		0.2	0.003		0.007
a2			1.65			0.064
b	0.35		0.46	0.013		0.018
b1	0.19		0.25	0.007		0.010
C		0.5			0.019	
c1	45 (typ.)					
D	8.55		8.75	0.336		0.344
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		7.62			0.300	
F	3.8		4.0	0.149		0.157
G	4.6		5.3	0.181		0.208
L	0.5		1.27	0.019		0.050
M			0.68			0.026
S	8 (max.)					



P013G

TSSOP14 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.1			0.433
A1	0.05	0.10	0.15	0.002	0.004	0.006
A2	0.85	0.9	0.95	0.335	0.354	0.374
b	0.19		0.30	0.0075		0.0118
c	0.09		0.20	0.0035		0.0079
D	4.9	5	5.1	0.193	0.197	0.201
E	6.25	6.4	6.5	0.246	0.252	0.256
E1	4.3	4.4	4.48	0.169	0.173	0.176
e		0.65 BSC			0.0256 BSC	
K	0°	4°	8°	0°	4°	8°
L	0.50	0.60	0.70	0.020	0.024	0.028





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