

Arithmetic logic unit

74F181

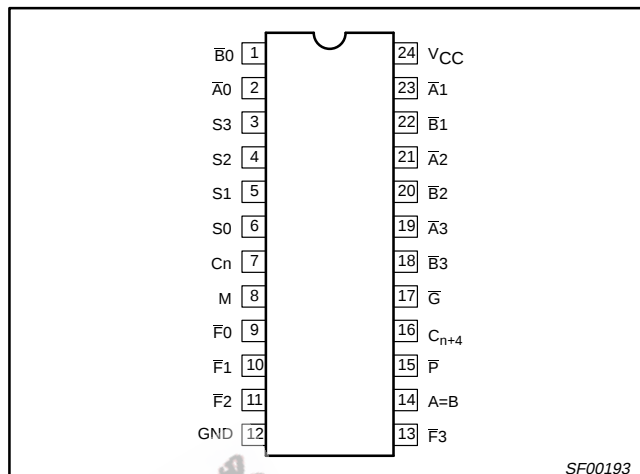
FEATURES

- Provides 16 arithmetic operation: add, subtract, compare, and double; plus 12 other arithmetic operations
- Provides all 16 logic operations of two variables: Exclusive-OR, Compare, AND, NAND, NOR, OR, plus 10 other logic operations
- Full look-ahead carry for high speed arithmetic operation on long words
- 40% faster than 'S181 with only 30% 'S181 power consumption
- Available in 300mil-wide Slim 24-pin Dual In-Line package

DESCRIPTION

The 74F181 is a 4-bit high-speed parallel Arithmetic Logic Unit (ALU). Controlled by the four Function Select inputs (S0–S3) and the Mode Control input (M), it can perform all the 16 possible logic operations or 16 different arithmetic operations on active-High or active-Low operands. The Function Table lists these operations.

PIN CONFIGURATION



SF00193

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F181	7.0ns	43mA

ORDERING INFORMATION

DESCRIPTION	COMMERCIAL RANGE $V_{CC} = 5V \pm 10\%$, $T_{amb} = 0^{\circ}C$ to $+70^{\circ}C$
24-Pin Plastic Slim DIP (300 mil)	N74F181N
24-Pin Plastic SOL	N74F181D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

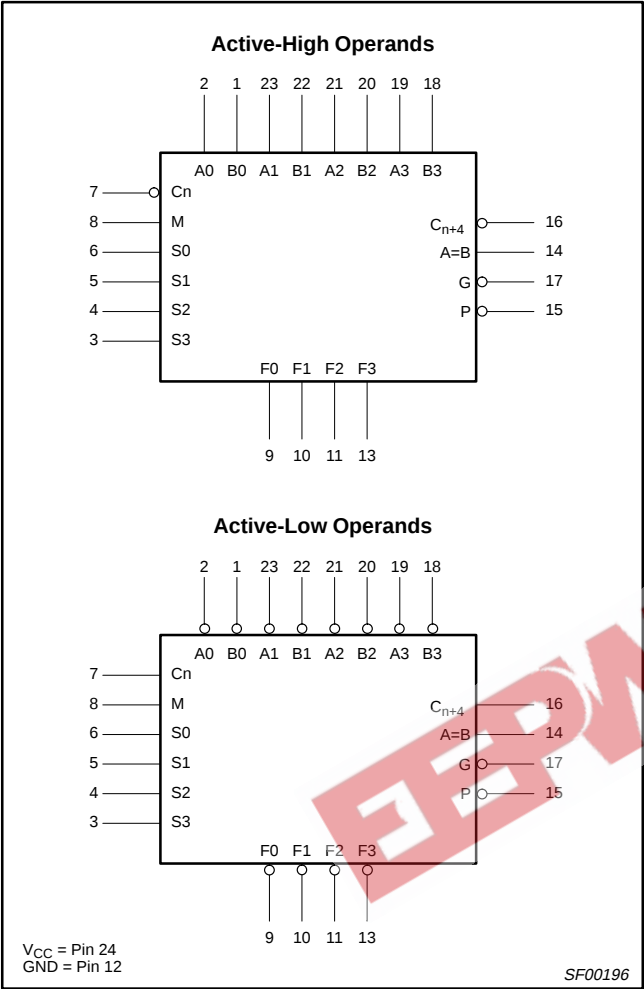
PINS	DESCRIPTION	74F (U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$\bar{A}0$ – $\bar{A}3$	A operand inputs	1.0/3.0	20 μ A/1.8mA
$\bar{B}0$ – $\bar{B}3$	B operand inputs	1.0/3.0	20 μ A/1.8mA
M	Mode control input	1.0/1.0	20 μ A/0.6mA
S0–S3	Function select input	1.0/4.0	20 μ A/2.4mA
Cn	Carry input	1.0/5.0	20 μ A/3.0mA
Cn+4	Carry output	50/33	1.0mA/20mA
$\bar{P}$	Carry Propagate output	50/33	1.0mA/20mA
$\bar{G}$	Carry Generate output	50/33	1.0mA/20mA
A=B	Compare output	OC/33	OC/20mA
$\bar{F}0$ – $\bar{F}3$	Outputs	50/33	1.0mA/20mA

NOTE: One (1.0) FAST unit load is defined as: 20 μ A in the High state and 0.6mA in the Low state.
OC = Open Collector

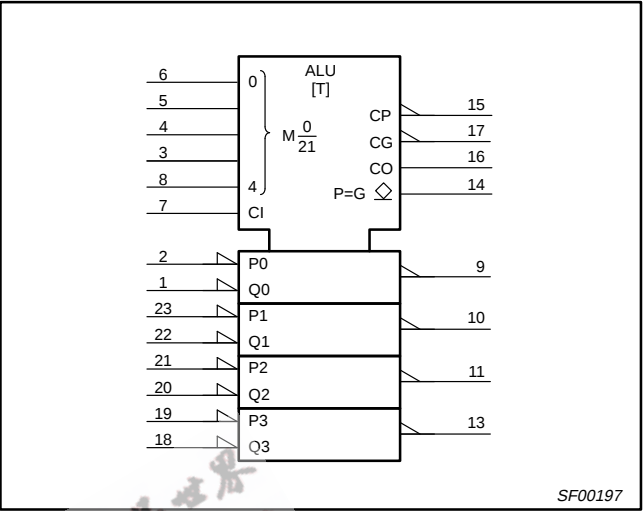
Arithmetic logic unit

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LOGIC SYMBOL



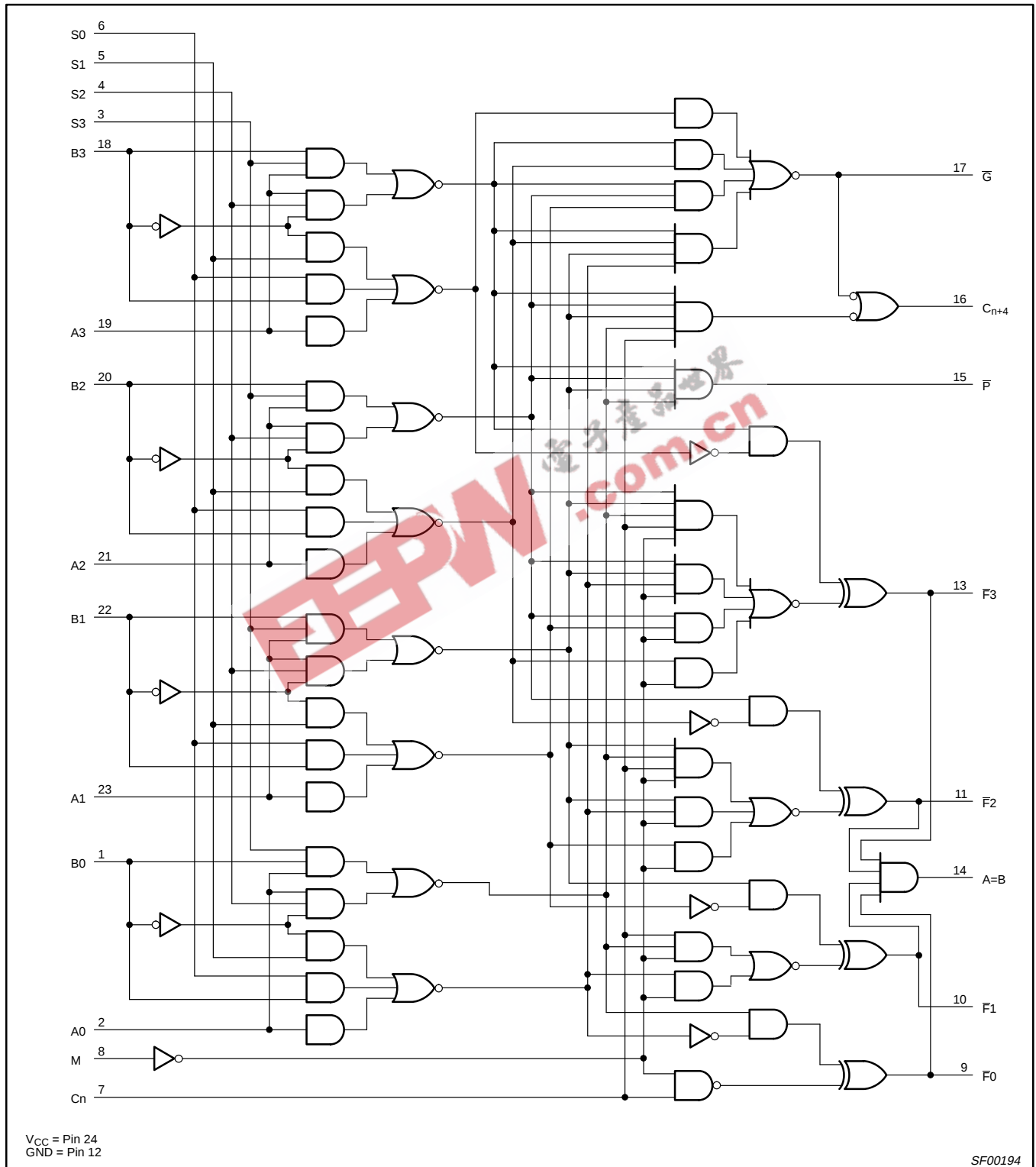
IEC/IEEE SYMBOL



Arithmetic logic unit

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LOGIC DIAGRAM



Arithmetic logic unit

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When the Mode Control input (M) is High, all internal carries are inhibited and the device performs logic operations on the individual bits as listed. When the Mode control input is Low, the carries are enabled and the device performs arithmetic operations on the two 4-bit words. The device incorporates full internal carry look-ahead and provides for either ripple carry between device using the C_{n+4} output, or for carry look-ahead between packages using the signals $\bar{P}$ (Carry Propagate) and $\bar{G}$ (Carry Generate). $\bar{P}$ and $\bar{G}$ are not affected by carry in. When speed requirements are not stringent, it can be used in a simple ripple carry mode by connecting the Carry output (C_{n+4}) signal to the Carry input (C_n) of the next unit. For high-speed operation, the device is used in conjunction with the 74F182 carry look-ahead circuit. One carry look-ahead package is required for each group of four 74F181 devices. Carry look-ahead can be provided at various levels and offers high speed capability over extremely long word lengths.

The A=B output from the device goes High when all four F outputs are High and can be used to indicate logic equivalence over 4-bits

when the unit is in the subtract mode. The A=B output is open-collector and can be wired-AND with other A=B outputs to give a comparison for more than 4 bits. The A=B signal can also be used with the C_{n+4} signal to indicate A>B and A<B. The Function Table lists the arithmetic operations that are performed without a carry in. An incoming carry adds a one to each operation. Thus select code LHHL generates A minus B minus 1 (two's complement notation) without a carry in and generates A minus B when a carry is applied. Because subtraction is actually performed by complementary addition (one's complement), a carry out means borrow; thus, a carry is generated when there is no underflow and no carry is generated when there is underflow. As indicated, this device can be used with either active-Low inputs producing active-Low outputs or with active-High inputs producing active-High outputs. For either case, the table lists the operations that are performed to the operands labeled inside the logic symbol.

MODE-SELECT FUNCTION TABLE

MODE SELECT INPUTS				ACTIVE HIGH INPUTS & OUTPUTS		ACTIVE LOW INPUTS & OUTPUTS	
S3	S2	S1	S0	Logic (M=H)	Arithmetic** (M=L) (Cn=H)	Logic (M=H)	Arithmetic** (M=L) (Cn=L)
L	L	L	L	$\bar{A}$	A	$\bar{A}$	A minus 1
L	L	L	H	$\bar{A}+\bar{B}$	A+B	$\bar{A}\bar{B}$	AB minus 1
L	L	H	L	$\bar{A}B$	$A+\bar{B}$	$\bar{A}+B$	$\bar{A}\bar{B}$ minus 1
L	L	H	H	Logical 0	minus 1	Logical 1	minus 1
L	H	L	L	$\bar{A}\bar{B}$	A plus $\bar{A}\bar{B}$	$\bar{A}+\bar{B}$	A plus (A+B)
L	H	L	H	$\bar{B}$	(A+B) plus $\bar{A}\bar{B}$	$\bar{B}$	AB plus (A+B)
L	H	H	L	$A\oplus B$	A minus B minus 1	$\bar{A}\oplus \bar{B}$	A minus B minus 1
L	H	H	H	$A\bar{B}$	AB minus 1	$A+\bar{B}$	$A+\bar{B}$
H	L	L	L	$\bar{A}+B$	A plus AB	$\bar{A}B$	A plus (A+B)
H	L	L	H	$\bar{A}\oplus \bar{B}$	A plus B	$A\oplus B$	A plus B
H	L	H	L	B	(A+B) plus AB	B	$\bar{A}\bar{B}$ plus (A+B)
H	L	H	H	AB	AB minus 1	A+B	A+B
H	H	L	L	Logical 1	A plus A*	Logical 0	A plus A*
H	H	L	H	$A+\bar{B}$	(A+B) plus A	$\bar{A}\bar{B}$	AB plus A
H	H	H	L	A+B	(A+B) plus A	AB	$\bar{A}\bar{B}$ plus A
H	H	H	H	A	A minus 1	A	A

H = High voltage level

L = Low voltage level

* = Each bit is shifted to the next more significant position.

** = Arithmetic operations expressed in two's complement notation.

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Table 1. Sum Mode TestFunction Inputs: $S_0 = S_3 = 4.5V$, $S_1 = S_2 = M = 0V$

PARAMETER	INPUT UNDER TEST	OTHER INPUT, SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST
		Apply 4.5V	Apply GND	Apply 4.5V	Apply GND	
t_{PLH}, t_{PHL}	$\bar{A}_i$	$\bar{B}_i$	None	Remaining $\bar{A}$ and $\bar{B}$	C_n	$\bar{F}_i$
t_{PLH}, t_{PHL}	$\bar{B}_i$	$\bar{A}_i$	None	Remaining $\bar{A}$ and $\bar{B}$	C_n	$\bar{F}_i$
t_{PLH}, t_{PHL}	$\bar{A}_i$	$\bar{B}_i$	None	None	Remaining $\bar{A}, \bar{B}, C_n$	$\bar{P}$
t_{PLH}, t_{PHL}	$\bar{B}_i$	$\bar{A}_i$	None	None	Remaining $\bar{A}, \bar{B}, C_n$	$\bar{P}$
t_{PLH}, t_{PHL}	$\bar{A}_i$	None	$\bar{B}_i$	Remaining $\bar{B}$	Remaining $\bar{A}, C_n$	$\bar{G}$
t_{PLH}, t_{PHL}	$\bar{B}_i$	None	$\bar{A}_i$	Remaining $\bar{B}$	Remaining $\bar{A}, C_n$	$\bar{G}$
t_{PLH}, t_{PHL}	$\bar{A}_i$	None	$\bar{B}_i$	Remaining $\bar{B}$	Remaining $\bar{A}, C_n$	C_{n+4}
t_{PLH}, t_{PHL}	$\bar{B}_i$	None	$\bar{A}_i$	Remaining $\bar{B}$	Remaining $\bar{A}, C_n$	C_{n+4}
t_{PLH}, t_{PHL}	C_n	None	None	All $\bar{A}$	All $\bar{B}$	Any $\bar{F}$ or C_{n+4}

Table 2. Diff Mode TestFunction Inputs: $S_1 = S_2 = 4.5V$, $S_0 = S_3 = M = 0V$

PARAMETER	INPUT UNDER TEST	OTHER INPUT, SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST
		Apply 4.5V	Apply GND	Apply 4.5V	Apply GND	
t_{PLH}, t_{PHL}	$\bar{A}_i$	None	$\bar{B}_i$	Remaining $\bar{A}$	Remaining $\bar{B}, C_n$	$\bar{F}_i$
t_{PLH}, t_{PHL}	$\bar{B}_i$	$\bar{A}_i$	None	Remaining $\bar{A}$	Remaining $\bar{B}, C_n$	$\bar{F}_i$
t_{PLH}, t_{PHL}	$\bar{A}_i$	None	$\bar{B}_i$	None	Remaining $\bar{A}, \bar{B}, C_n$	$\bar{P}$
t_{PLH}, t_{PHL}	$\bar{B}_i$	$\bar{A}_i$	None	None	Remaining $\bar{A}, \bar{B}, C_n$	$\bar{P}$
t_{PLH}, t_{PHL}	$\bar{A}_i$	$\bar{B}_i$	None	None	Remaining $\bar{A}, \bar{B}, C_n$	$\bar{G}$
t_{PLH}, t_{PHL}	$\bar{B}_i$	None	$\bar{A}_i$	None	Remaining $\bar{A}, \bar{B}, C_n$	$\bar{G}$
t_{PLH}, t_{PHL}	$\bar{A}_i$	None	$\bar{B}_i$	Remaining $\bar{A}$	Remaining $\bar{B}, C_n$	$A=B$
t_{PLH}, t_{PHL}	$\bar{B}_i$	$\bar{A}_i$	None	Remaining $\bar{A}$	Remaining $\bar{B}, C_n$	$A=B$
t_{PLH}, t_{PHL}	$\bar{A}_i$	$\bar{B}_i$	None	None	Remaining $\bar{A}, \bar{B}, C_n$	C_{n+4}
t_{PLH}, t_{PHL}	$\bar{B}_i$	None	$\bar{A}_i$	None	Remaining $\bar{A}, \bar{B}, C_n$	C_{n+4}
t_{PLH}, t_{PHL}	C_n	None	None	All $\bar{A}$ and $\bar{B}$	None	Any $\bar{F}$ or C_{n+4}

Table 3. Logic Mode TestFunction Inputs: $S_1 = S_2 = 4.5V$, $S_0 = S_3 = 0V$

PARAMETER	INPUT UNDER TEST	OTHER INPUT, SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST
		Apply 4.5V	Apply GND	Apply 4.5V	Apply GND	
t_{PLH}, t_{PHL}	$\bar{A}_i$	$\bar{B}_i$	None	None	Remaining $\bar{A}, \bar{B}, C_n$	$\bar{F}_i$
t_{PLH}, t_{PHL}	$\bar{B}_i$	$\bar{A}_i$	None	None	Remaining $\bar{A}, \bar{B}, C_n$	$\bar{F}_i$

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device.

Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to V_{CC}	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_{amb}	Operating free-air temperature range	0 to +70	°C
T_{stg}	Storage temperature range	-65 to +150	°C

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RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			MIN	NOM	MAX	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
I_{IK}	Input clamp current				-18	mA
V_{OH}	High level output voltage	A=B only			4.5	V
I_{OH}	High-level output current	Any output except A=B			-1	mA
I_{OL}	Low-level output current				20	mA
T_{amb}	Operating free-air temperature range		0		+70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS ¹		LIMITS			UNIT	
					MIN	TYP ²	MAX		
I _{OH}	High-level output current	A=B only	V _{CC} = MIN, V _{IL} = MAX; V _{IH} = MIN, V _{OH} = MAX				250	μA	
V _{OH}	High-level output voltage	Any output except A=B	V _{CC} = MIN, V _{IL} = MAX, V _{IH} = MIN	I _{OH} = MAX	±10%V _{CC}	2.5		V	
					±5%V _{CC}	2.7	3.4		
V _{OL}	Low-level output voltage		V _{CC} = MIN, V _{IL} = MAX, V _{IH} = MIN	I _{OL} = MAX	±10%V _{CC}		0.30	V	
					±5%V _{CC}		0.30		0.50
V _{IK}	Input clamp voltage		V _{CC} = MIN, I _I = I _{IK}				−0.73	−1.2	V
I _I	Input current at maximum input voltage		V _{CC} = MAX, V _I = 7.0V					100	μA
I _{IH}	High-level input current		V _{CC} = MAX, V _I = 2.7V					20	μA
I _{IL}	Low-level input current	M	V _{CC} = MAX, V _I = 0.5V					−0.6	mA
		Ā0–Ā3, B̄0–B̄3						−1.8	mA
		S0–S3						−2.4	mA
		Cn						−3.0	mA
I _{OS}	Short-circuit output current ³	Any output except A=B	V _{CC} = MAX			−60		−150	mA
I _{CC}	Supply current (total)	I _{CCH}	V _{CC} = MAX	S0–S3=M=Ā0–Ā3=4.5V, B̄0–B̄3=Cn=GND		43	65	mA	
		I _{CCL}		S0–S3=M=4.5V, B̄0–B̄3=Cn=Ā0–Ā3=GND		43	65	mA	

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at $V_{CC} = 5\text{V}$, $T_{amb} = 25^\circ\text{C}$.
- Not more than one output should be shorted at a time. For testing I_{OS} , the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

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AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS				LIMITS					UNIT
						$V_{CC} = +5.0V$ $T_{amb} = +25^{\circ}C$ $C_L = 50pF$ $R_L = 500\Omega$			$V_{CC} = +5.0V \pm 10\%$ $T_{amb} = 0^{\circ}C \text{ to } +70^{\circ}C$ $C_L = 50pF$ $R_L = 500\Omega$		
		Mode	Table	Waveform	Condition	MIN	TYP	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay C_n to C_{n+4}	Sum Diff	1 2	1	M=0V	3.0 2.5	5.0 5.0	8.0 8.0	3.0 2.5	8.5 8.5	ns
t_{PLH} t_{PHL}	Propagation delay $\bar{A}_n$ or B_n to C_{n+4}	Sum	1	2	M=S1=S2=0V, S0=S3=4.5V	5.0 5.0	9.0 8.0	12.0 12.0	5.0 5.0	13.0 12.5	ns
t_{PLH} t_{PHL}	Propagation delay $\bar{A}_n$ or B_n to C_{n+4}	Diff	2	2	M=S0=S3=0V, S1=S2=4.5V	5.0 5.0	9.5 8.0	13.0 12.0	5.0 5.0	14.0 12.5	ns
t_{PLH} t_{PHL}	Propagation delay C_n to F_n	Diff Sum	2 1	1	M=0V	3.0 3.0	5.0 5.0	8.0 8.0	3.0 2.5	9.0 9.0	ns
t_{PLH} t_{PHL}	Propagation delay $\bar{A}_n$ or B_n to $\bar{G}$	Sum	1	1	M=S1=S2=0V, S0=S3=4.5V	3.0 3.0	5.0 5.0	7.5 7.5	2.5 2.5	8.0 8.0	ns
t_{PLH} t_{PHL}	Propagation delay $\bar{A}_n$ or B_n to $\bar{G}$	Diff	2	2	M=S0=S3=0V, S1=S2=4.5V	3.0 3.0	4.5 5.0	8.0 8.5	2.5 2.5	9.0 9.5	ns
t_{PLH} t_{PHL}	Propagation delay $\bar{A}_n$ or B_n to $\bar{P}$	Sum	1	2	M=S1=S2=0V, S0=S3=4.5V	2.5 3.0	4.0 4.5	7.0 7.5	2.0 2.5	7.5 8.0	ns
t_{PLH} t_{PHL}	Propagation delay $\bar{A}_n$ or B_n to $\bar{P}$	Diff	2	1, 2	M=S0=S3=0V, S1=S2=4.5V	2.5 3.0	4.0 5.0	7.5 8.5	2.0 2.5	8.0 9.0	ns
t_{PLH} t_{PHL}	Propagation delay $\bar{A}_i$ or $\bar{B}_i$ to $\bar{F}_i$	Sum	1	1, 2	M=S1=S2=0V, S0=S3=4.5V	3.0 3.0	4.5 4.5	7.5 7.5	2.5 3.0	8.5 8.5	ns
t_{PLH} t_{PHL}	Propagation delay $\bar{A}_i$ or $\bar{B}_i$ to $\bar{F}_i$	Diff	2	1, 2	M=S0=S3=0V, S1=S2=4.5V	3.0 3.0	4.5 5.0	8.5 8.5	2.5 3.0	9.0 9.0	ns
t_{PLH} t_{PHL}	Propagation delay $\bar{A}_n$ or B_n to F_n	Sum		1, 2		3.5 3.5	6.0 5.5	10.0 9.5	3.0 3.0	11.0 10.0	ns
t_{PLH} t_{PHL}	Propagation delay $\bar{A}_n$ or B_n to F_n	Diff		1, 2		4.0 4.5	6.5 7.0	10.5 10.5	3.5 4.5	11.0 11.0	ns
t_{PLH} t_{PHL}	Propagation delay $\bar{A}_i$ or $\bar{B}_i$ to $\bar{F}_i$	Logic	3	1, 2	M=4.5V	3.5 3.5	5.5 5.5	9.0 10.0	3.0 3.0	9.5 10.5	ns
t_{PLH} t_{PHL}	Propagation delay $\bar{A}_n$ or B_n to A=B	Diff	2	1, 2	M=S0=S3=0V, S1=S2=4.5V	10.0 6.0	14.0 8.5	19.0 12.5	9.5 5.5	20.5 12.5	ns

NOTES:

" $\bar{A}_n$ or B_n to F_n " means any $\bar{A}$ or any B to any $\bar{F}$; " $\bar{A}_i$ or B_i to $\bar{F}_i$ " means $\bar{A}1$, $B1$ to $\bar{F}1$; $\bar{A}2$, $B2$ to $\bar{F}2$ (the identifying number must be the same).

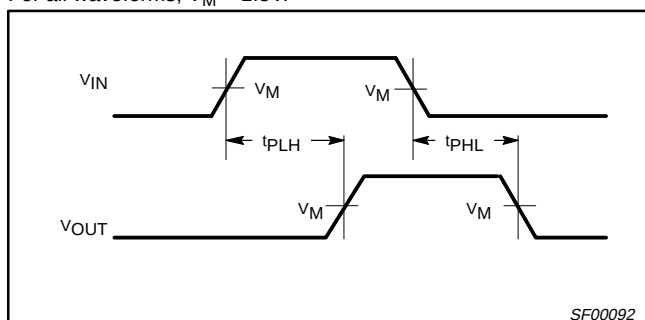
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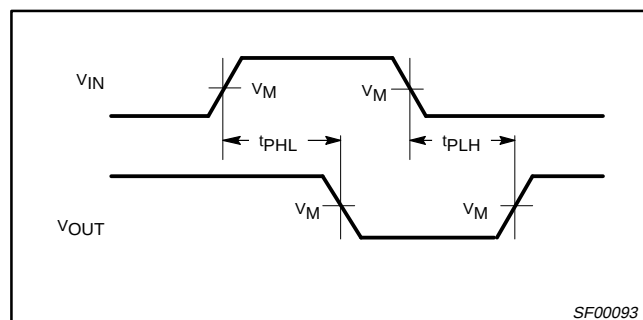
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS					UNIT
				$V_{CC} = +5.0V$ $T_{amb} = +25^{\circ}C$ $C_L = 50pF$ $R_L = 500\Omega$			$V_{CC} = +5.0V \pm 10\%$ $T_{amb} = 0^{\circ}C \text{ to } +70^{\circ}C$ $C_L = 50pF$ $R_L = 500\Omega$		
		Mode	Waveform	MIN	TYP	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation delay S_i to $\overline{F_i}$ (Inverting)		1	3.5 3.5	5.5 5.0	8.0 8.0	3.0 3.0	9.0 9.0	ns
t_{PLH} t_{PHL}	Propagation delay S_i to $\overline{F_i}$ (Non-Inverting)		2	3.0 3.0	5.5 5.5	8.5 8.5	3.0 3.0	9.5 9.5	ns
t_{PLH} t_{PHL}	Propagation delay S_i to A=B (Inverting)		1	10.5 6.0	16.5 8.0	22.5 11.0	10.5 6.0	24.0 11.5	ns
t_{PLH} t_{PHL}	Propagation delay S_i to A=B (Non-Inverting)		2	10.0 5.5	15.0 8.5	19.0 12.5	10.0 5.0	21.0 13.5	ns
t_{PLH} t_{PHL}	Propagation delay S_i to C_{n+4} (Inverting)		1	3.5 3.0	7.0 5.5	11.0 10.0	3.0 2.5	12.5 10.0	ns
t_{PLH} t_{PHL}	Propagation delay S_i to $\overline{G}$ (Non-Inverting)		2	2.5 2.5	5.0 4.0	7.5 7.5	2.5 2.5	8.0 8.0	ns
t_{PLH} t_{PHL}	Propagation delay S_i to $\overline{P}$ (Non-Inverting)		2	2.5 2.5	4.0 4.5	6.5 7.0	2.5 2.5	7.0 8.0	ns
t_{PLH} t_{PHL}	Propagation delay M to $\overline{F_i}$ (Inverting)	Sum	1	3.5 3.5	6.0 6.0	8.5 8.5	3.5 3.5	9.5 9.5	ns
t_{PLH} t_{PHL}	Propagation delay M to $\overline{F_i}$ (Non-Inverting)	Sum	2	4.5 4.0	7.0 6.0	10.0 9.5	4.5 4.0	11.0 10.0	ns
t_{PLH} t_{PHL}	Propagation delay M to $\overline{F_i}$ (Inverting)	Diff	1	3.5 3.5	6.0 6.0	8.5 8.5	3.5 3.5	9.5 9.5	ns
t_{PLH} t_{PHL}	Propagation delay M to $\overline{F_i}$ (Non-Inverting)	Diff	2	4.0 4.0	7.0 6.0	10.0 9.5	4.0 4.0	11.5 10.0	ns
t_{PLH} t_{PHL}	Propagation delay M to A=B (Inverting)	Sum	1	12.0 6.5	16.0 8.0	20.0 11.0	11.0 6.0	22.0 11.0	ns
t_{PLH} t_{PHL}	Propagation delay M to A=B (Non-Inverting)	Sum	2	13.0 6.5	17.0 8.0	21.0 10.5	12.0 6.0	24.0 11.5	ns
t_{PLH} t_{PHL}	Propagation delay M to A=B (Inverting)	Diff	1	11.5 6.0	16.0 8.0	20.0 10.5	10.5 6.0	22.0 11.0	ns
t_{PLH} t_{PHL}	Propagation delay M to A=B (Non-Inverting)	Diff	2	13.0 6.0	17.0 8.0	21.5 11.0	12.5 6.0	24.0 11.5	ns

AC WAVEFORMS

For all waveforms, $V_M = 1.5V$.

Waveform 1. Propagation Delay for Non-Inverting Paths

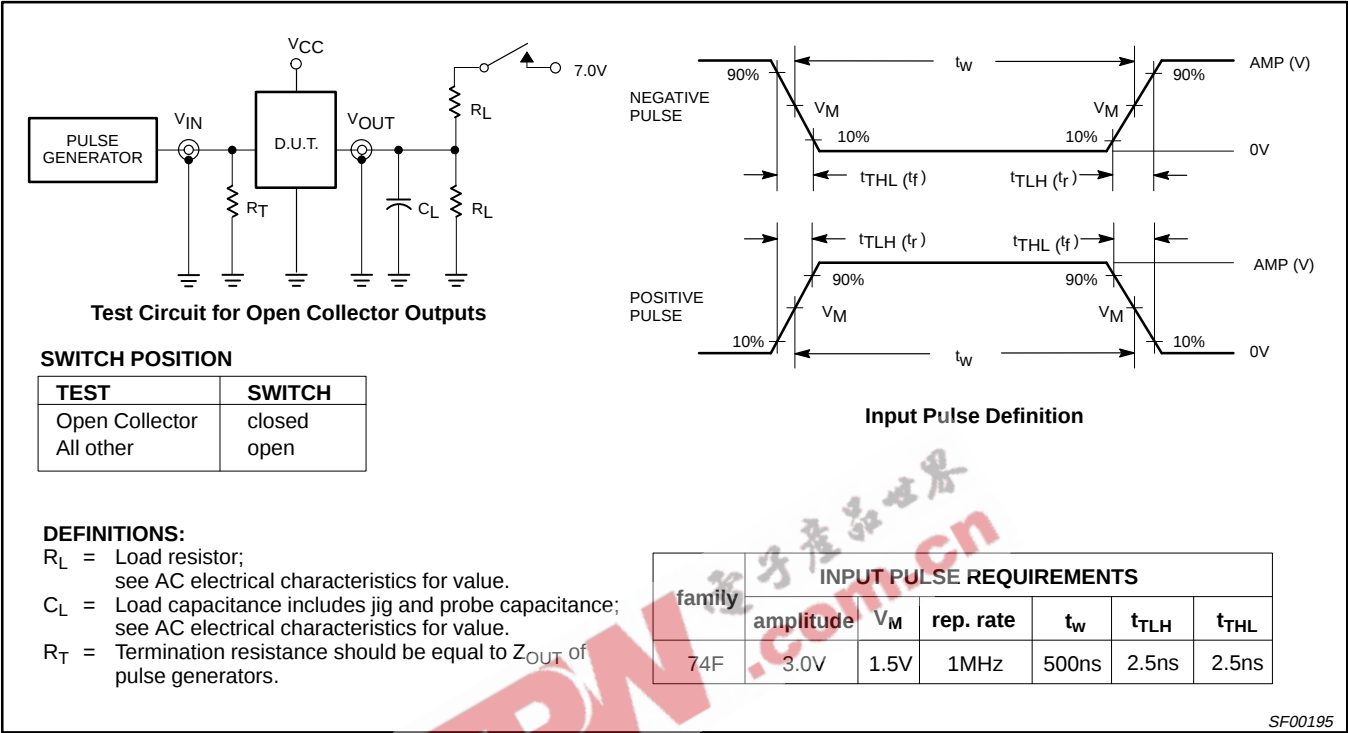


Waveform 2. Propagation Delay for Inverting Paths

Arithmetic logic unit

74F181

TEST CIRCUIT AND WAVEFORMS



SF00195